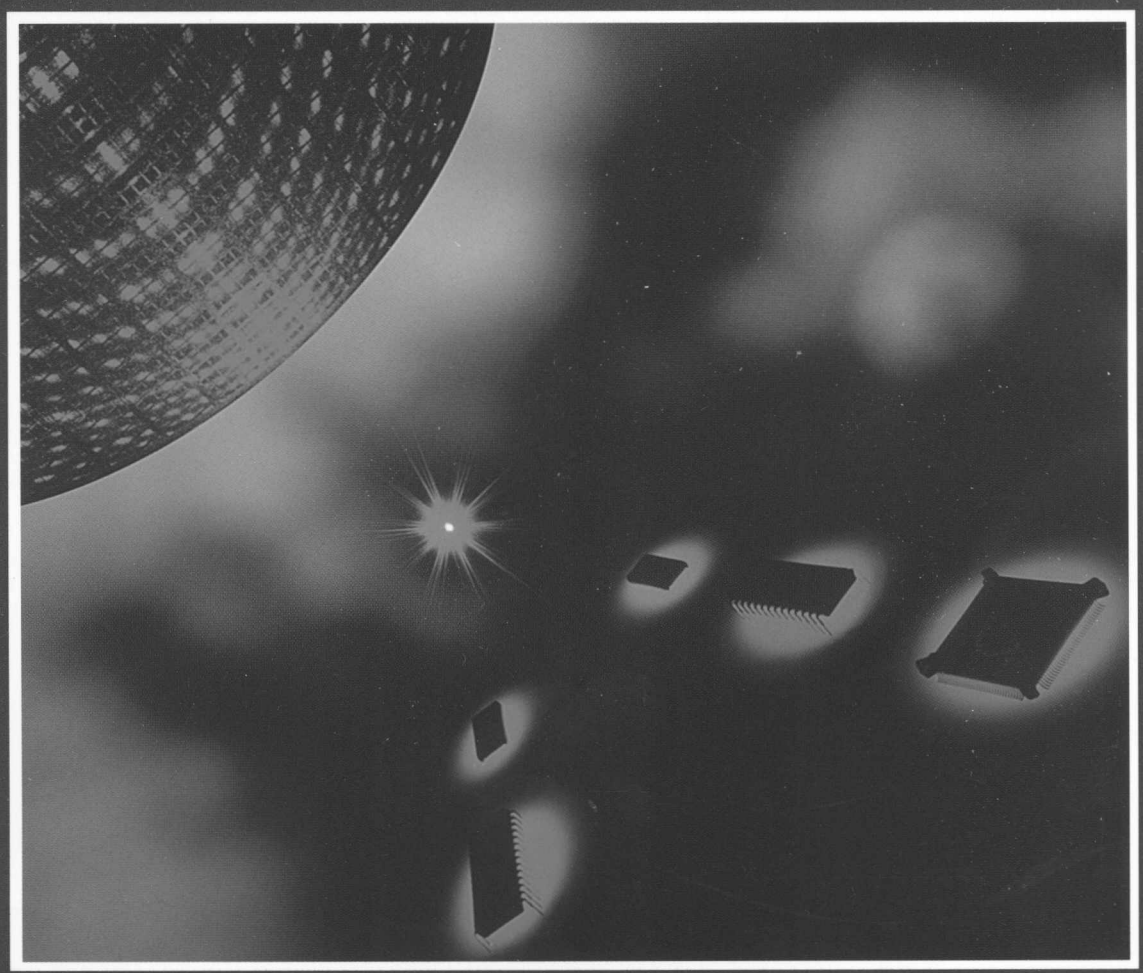
SHARP

Memory
Data Book
1992



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NOTICE

The specifications contained within this Sharp Memory Data Book are current as of the July, 1992 publication date.

The product data provided is classified and labeled as follows:

CLASSIFICATION *	DESCRIPTION
Product Preview	Contains information about a device that is in the planning stage or the soon to be in-development stage.
Advance Information	Contains information about a device that is in development. Includes design specifications for device development.
Preliminary	Contains information for device soon to be, or recently, released to production.
No label is used for this classification.	Contains information about a device that is in full production.

* Note: occasionally certain product data information may be classified and labeled differently than the main classification label. For example, a main label may be 'Preliminary,' but the 15 ns version of that part may be labeled 'Advance Information.'

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PREFACE

As we become more and more an information-oriented society, memory products have come to play a major role in both home and office equipment. On the one hand, computer-related services are growing ever more sophisticated and diverse; on the other, they are becoming much more accessible to each of us in our daily lives. Along with this increase in the importance of the information processing in our lives, we are faced with a growing demand for memory products using the most advanced technology.

To keep pace with this rapid progress, we at Sharp will continue to direct our efforts at understanding the crucial trends of the moment in this area and supply our customers with products that truly meet their needs. In short, to contribute to a better life for all of us in this age of expanding technology.

Sharp has developed a wide range of memory units including SRAMs, DRAMs, EPROMs, OTPROMs, Mask Programmable ROMs, and FIFO Memories for use in numerous areas of application. Sharp memory units are used extensively in personal computers, advanced office automation and measuring control equipment, video games, as well as in character processing and dictionary ROMs.

This data book has been especially compiled for the use of our customers. Listed here is the entire range of memory products developed and manufactured by Sharp, with detailed explanations of their many functions and outstanding features. We hope that you find this book useful in determining which Sharp products are best suited to your needs. Please contact us directly if you have any further questions.

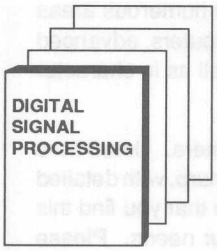
SHARP'S INTEGRATED CIRCUIT DOCUMENTATION

MICRO-COMPUTER

- 4-Bit Single-Chip Microcomputers
- 8-Bit Single-Chip Microcomputers
- 8-Bit Microprocessors/Peripherals
- 16-Bit Microprocessors/Peripherals
- Development Support Tools

MOS

- Gate Arrays/Standard Cells
- Display Drivers, Telecommunications
- MODEMs, CCDs/CCD Peripherals
- ICs for Audio/Visual Equipment
- Voice/Melody Generators, ICs for Clock, etc.



DIGITAL SIGNAL PROCESSING

24-Bit Real Time Digital Signal Processing

- Data Sheets
- User's Guides
- Simulator Guides
- Application Notes
- Evaluation Modules/Boards

BIPOLAR

- Operational Amplifiers/Comparators
- Transistor Arrays, Voltage Regulators
- A/D, D/A Converters, Bus Interfaces
- ICs for Audio/Visual Equipment
- CCD Peripherals, ICs for Telephone, etc.

MEMORY

- Pseudo-Static RAMs
- Static RAMs
- Mask-Programmable ROMs
- FIFO Memories
- Application Notes and Conference Papers

RELIABILITY HANDBOOK

- Quality and Reliability Assurance System
- How Sharp Views Semiconductor Device Reliability and Reliability Prediction
- Reliability Testing
- Failure Analysis
- Proper Handling of Semiconductor Devices

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PSEUDO-STATIC RAMs

	Density	Organization	
LH5P832	256K	32K × 8	2-1
LH5P8129	1M	128K × 8	2-8
LH5P8128	1M	128K × 8	2-20
LH5P8512	4M	512K × 8	2-32

STATIC RAMs

LH5116/H	16K	2K × 8	3-1
LH5116S	16K	2K × 8	3-9
LH5118/H	16K	2K × 8	3-16
LH5168/H	64K	8K × 8	3-24
LH5168SH	64K	8K × 8	3-33
LH51256L	256K	32K × 8	3-41
LH511000UL	1M	128K × 8	3-48
LH52250AL	256K	32K × 8	3-57
LH52256LL	256K	32K × 8	3-65
LH52252A	256K	64K × 4	3-72
LH52252B	256K	64K × 4	3-79
LH52253	256K	64K × 4	3-86
LH52258	256K	32K × 8	3-93
LH52258A	256K	32K × 8	3-101
LH52258B	256K	32K × 8	3-109
LH521002	1M	256K × 4	3-117
LH521007	1M	128K × 8	3-125
LH521008	1M	128K × 8	3-133
LH521028	1M	64K × 18	3-141

MASK-PROGRAMMABLE ROMs

LH53259	256K	32K × 8	4-1
LH53515	512K	64K × 8	4-7
LH53H1000	1M	64K × 16	4-13
LH53H0900	1M	128K × 8	4-18
LH530800A	1M	128K × 8	4-23
LH531000B	1M	128K × 8	4-29
LH532000B	2M	256K × 8/128K × 16	4-35
LH532100B	2M	256K × 8	4-40
LH534000B	4M	512K × 8/256K × 16	4-44
LH534100B	4M	512K × 8	4-49

MASK-PROGRAMMABLE ROMs (cont'd)

	Density	Organization	
LH534500A	4M	512K × 8/256K × 16	4-54
LH534600	4M	512K × 8/256K × 16	4-60
LH538000	8M	1M × 8/512K × 16	4-65
LH538100	8M	1M × 8	4-71
LH538500A	8M	1M × 8/512K × 16	4-76
LH5316000	16M	2M × 8/1M × 16	4-83
LH5316500	16M	2M × 8/1M × 16	4-89
LH5332000	32M	4M × 8/2M × 16	4-95

FIFO MEMORIES

LH5481/91	64 × 8/64 × 9	5-2
LH5496	512 × 9	5-16
LH5497	1K × 9	5-31
LH5498	2K × 9	5-46
LH5499	4K × 9	5-61
LH5492	4K × 9	5-76
LH5493	4K × 9	5-94
LH5494	4K × 9	5-110
LH5420	256 × 36 × 2	5-125
LH540201/02	512 × 9/1K × 9	5-160
LH540203	2K × 9	5-176
LH540204	4K × 9	5-192
LH540205	8K × 9	5-208
LH540206	16K × 9	5-224
LH540215/25	512 × 18/1K × 18	5-226
LH543620	1K × 36	5-253

APPLICATION NOTES AND CONFERENCE PAPERS

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PACKAGING

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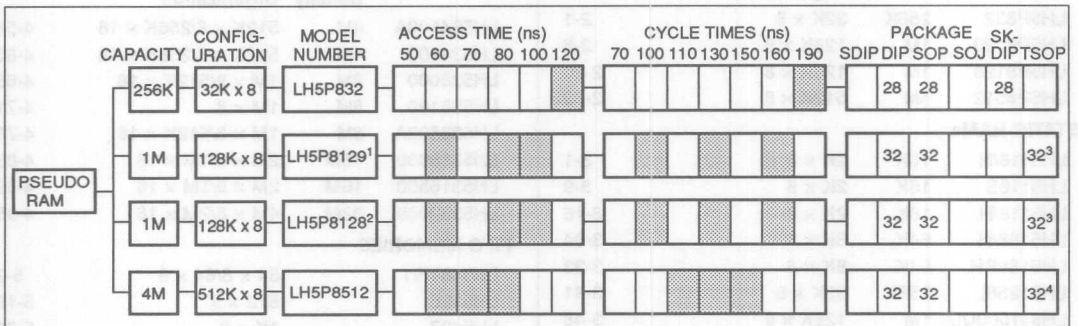
PSEUDO STATIC RAMs



CAPACITY	CONFIG-URATION (WORDS x BITS)	MODEL NO.	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION OPERATING/ STANDBY (mW) MAX.	OPERATING MODE	PACKAGE
256K	32,768 x 8	LH5P832	120	190	303/16.5	PSEUDO SRAM	28DIP/ 28SK-DIP/ 28SOP
1M	131,072 x 8	LH5P8129	60	100	572/5.5	PSEUDO SRAM	32DIP/ 32SOP/ 32TSOP[3]
			80	130	440/5.5		
			100	160	358/5.5		
		LH5P8128	60	100	572/5.5		
			80	130	440/5.5		
			100	160	358/5.5		
4M	524,288 x 8	LH5P8512	60	110	550/8.25	PSEUDO SRAM	32DIP/ 32SOP/ 32TSOP[4]
			70	130	550/8.25		
			80	150	550/8.25		

NOTES:

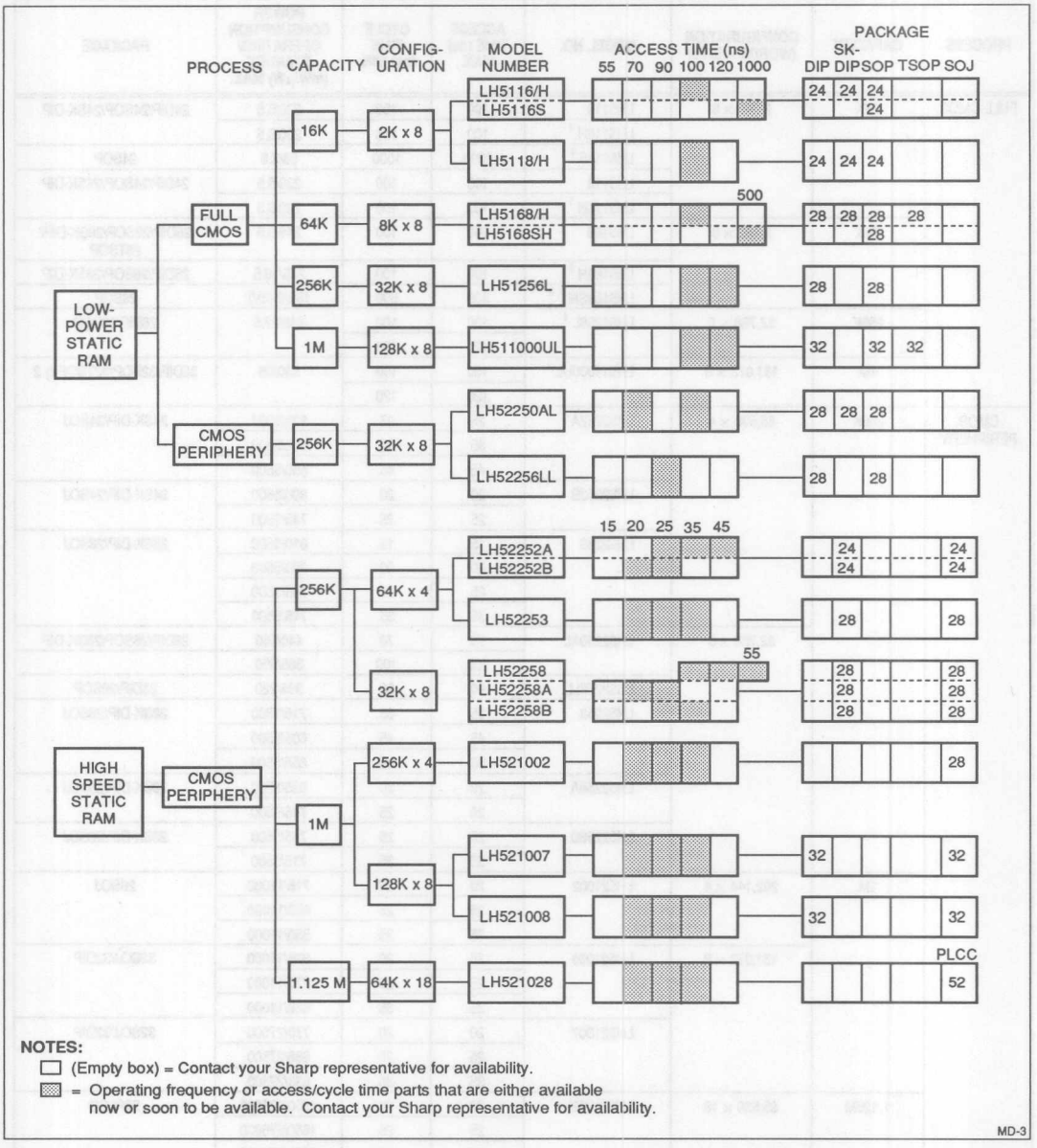
☐ (Empty box) = Contact your Sharp representative for availability.

▨ = Operating frequency or access/cycle time parts that are either available now or soon to be available. Contact your Sharp representative for availability.

1. $\overline{CS}$ Control
2. $\overline{CE}$ Control
3. TSOP(I)
4. TSOP(II) - Consult factory for availability.

MD-7A

STATIC RAMs



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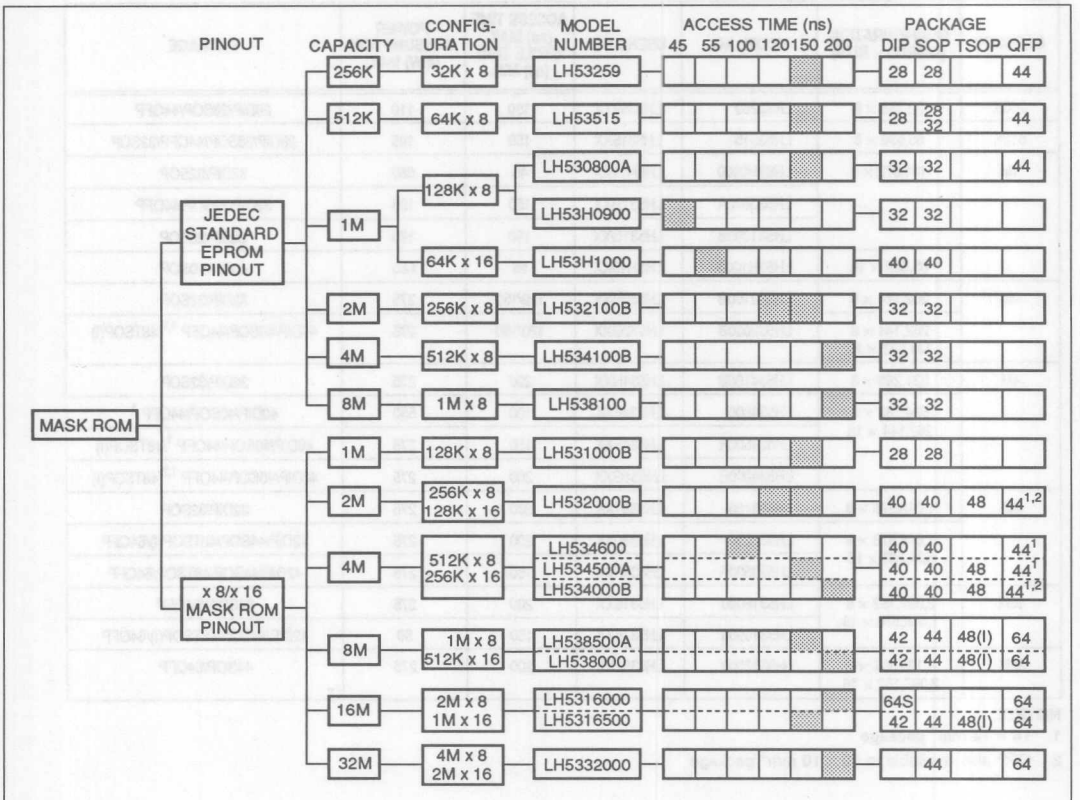
STATIC RAMs

PROCESS	CAPACITY	CONFIGURATION (WORDS × BITS)	MODEL NO.	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION OPERATING/ STANDBY (mW/μW) MAX.	PACKAGE
FULL CMOS	16K	2,048 × 8	LH5116	100	100	220/5.5	24DIP/24SOP/24SK-DIP
			LH5116H [1]	100	100	220/5.5	
			LH5116S [4]	1000	1000	33/3.3	24SOP
			LH5118	100	100	220/5.5	24DIP/24SOP/24SK-DIP
			LH5118H [1]	100	100	220/5.5	
	64K	8,192 × 8	LH5168	100	100	248/5.5	28DIP/28SOP/28SK-DIP/ 28TSOP
			LH5168H [1]	100	100	275/16.5	28DIP/28SOP/28SK-DIP
			LH5168SH [1, 4]	500	500	150/9 (3V)	28SOP
	256K	32,768 × 8	LH51256L [1]	100	100	248/27.5	28DIP/28SOP
				120	120		
	1M	131,072 × 8	LH511000UL [1]	100	100	330/66	32DIP/32SOP/32TSOP(I) 2
				120	120		
CMOS PERIPHERY	256K	65,536 × 4	LH52252A	25	25	825/5500	24SK-DIP/24SOJ
				35	35	660/5500	
				45	45	550/5500	
			LH52252B	20	20	800/5500	24SK-DIP/24SOJ
				25	25	745/5500	
			LH52253	15	15	910/5500	28SK-DIP/28SOJ
				20	20	800/5500	
				25	25	745/5500	
				35	35	745/5500	
		32,768 × 8	LH52250AL	70	70	440/550	28DIP/28SOP/28SK-DIP
				100	100	385/550	
			LH52256LL	90	90	385/220	28DIP/28SOP
			LH52258	35	35	715/5500	28SK-DIP/28SOJ
				45	45	605/5500	
				55	55	855/5500	
			LH52258A	20	20	825/5500	28SK-DIP/28SOJ
				25	25	745/5500	
			LH52258B	25	25	745/5500	28SK-DIP/28SOJ
				35	35	715/5500	
	1M	262,144 × 4	LH521002	20	20	715/11000	28SOJ
				25	25	660/11000	
				35	35	550/11000	
		131,072 × 8	LH521008	20	20	825/11000	32SOJ/32DIP
				25	25	770/11000	
				35	35	660/11000	
			LH521007	20	20	770/27500	32SOJ/32DIP
				25	25	688/27500	
				35	35	633/27500	
	1.125M	65,536 × 18	LH521028	20	20	1650/275000	52PLCC
				25	25	1650/275000	
				30	30	1650/275000	
				35	35	1650/275000	

NOTES:

1. T_{OPR} = -40 to +85°C
2. T TSOP (Type I) Forward bend
   TR TSOP (Type I) Reverse bend
3. Supply Voltage (V) = 3 ± 10%
4. Supply Voltage (V) = 2.5 to 5.5

MASK-PROGRAMMABLE ROMs



NOTES:

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- ▨ = Operating frequency or access/cycle time parts that are either available now or soon to be available. Contact your Sharp representative for availability.

LH5XXX: CMOS

1. 14 x 14 mm² package
2. QFP also available in 10 x 10 mm² package

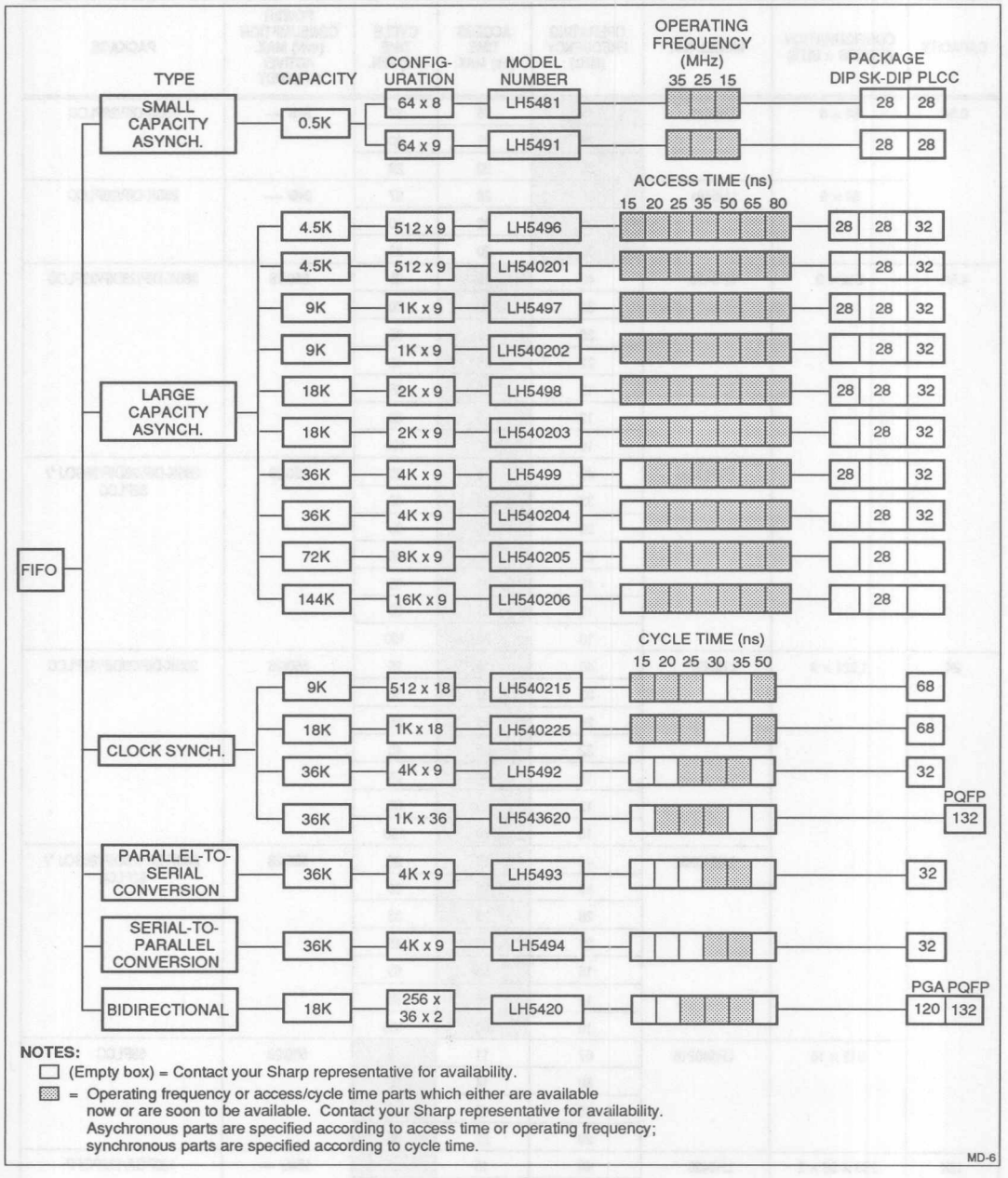
MD-5

MASK-PROGRAMMABLE ROMs

CAPACITY	CONFIGURATION (WORDS × BITS)	MODEL NO.	USERS NO.	ACCESS TIME (ns) MAX. CYCLE TIME (ns) MIN.	POWER CONSUMPTION (mW) MAX.	PACKAGE
256K	32,768 × 8	LH53259	LH5359XX	150	110	28DIP/28SOP/44QFP
512K	65,536 × 8	LH53515	LH5315XX	150	195	28DIP/28SOP/44QFP/32SOP
1M	131,072 × 8	LH53H0900	LH5H11XX	45	660	32DIP/32SOP
		LH530800A	LH531HXX	150	195	32DIP/32SOP/44QFP
		LH531000B	LH531GXX	150	195	28DIP/28SOP
	65,536 × 16	LH53H1000	LH5H10XX	55	660	40DIP/40SOP
2M	262,144 × 8	LH532100B	LH532HXX	120/150	275	32DIP/32SOP
	262,144 × 8 131,072 × 16	LH532000B	LH532GXX	120/150	275	40DIP/40SOP/44QFP [1,2]/48TSOP(I)
4M	524,288 × 8	LH534100B	LH534HXX	200	275	32DIP/32SOP
	524,288 × 8 262,144 × 16	LH534600	LH5346XX	100	550	40DIP/40SOP/44QFP [1]
		LH534500A	LH534FXX	150	275	40DIP/40SOP/44QFP [1]/48TSOP(I)
		LH534000B	LH534GXX	200	275	40DIP/40SOP/44QFP [1,2]/48TSOP(I)
8M	1,048,576 × 8	LH538100	LH5381XX	200	275	32DIP/32SOP
	1,048,576 × 8 524,288 × 16	LH538000	LH5380XX	200	275	42DIP/44SOP/48TSOP(I)/64QFP
		LH538500A	LH538FXX	150	275	42DIP/44SOP/48TSOP/64QFP
16M	2,097,152 × 8 1,048,576 × 16	LH5316000	LH5316XX	200	275	64SDIP/64QFP
		LH5316500	LH5375XX	150	50	42DIP/44SOP/48TSOP(I)/64QFP
32M	4,194,304 × 8 2,097,152 × 16	LH5332000	LH5332XX	200	275	44SOP/64QFP

NOTES:
1. 14 × 14 mm^2 package
2. QFP also available in 10 × 10 mm^2 package

FIFO MEMORIES



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- = Operating frequency or access/cycle time parts which either are available now or are soon to be available. Contact your Sharp representative for availability. Asychronous parts are specified according to access time or operating frequency; synchronous parts are specified according to cycle time.

FIFO MEMORIES

CAPACITY	CONFIGURATION (WORDS × BITS)	MODEL NO.	OPERATING FREQUENCY (MHz)	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION (mW) MAX. ACTIVE/ STANDBY	PACKAGE
0.5K	64 × 8	LH5481	15	26	67	248/ —	28SK-DIP/28PLCC
			25	22	40		
			35	20	28		
	64 × 9	LH5491	15	26	67	248/ —	28SK-DIP/28PLCC
			25	22	40		
			35	20	28		
4.5K	512 × 9	LH5496	40	15	25	550/28	28SK-DIP/28DIP/32PLCC
			33	20	30		
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
		LH540201	40	15	25	550/28	28SK-DIP/28DIP/28SOJ */ 32PLCC
			33	20	30		
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
9K	1,024 × 9	LH5497	40	15	25	550/28	28SK-DIP/28DIP/32PLCC
			33	20	30		
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
		LH540202	40	15	25	550/28	28SK-DIP/28DIP/28SOJ */ 32PLCC
			33	20	30		
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
	512 × 18	LH540215	67	11	15	550/28	68PLCC
			50	14	20		
			40	15	25		
			28	25	35		
18K	256 × 36 × 2	LH5420	40	15	25	1540/ —	120PGA/132PQFP
			33	20	30		
			28	25	35		

▨ Primary parameter for speed-grade specification.

* Contact your Sharp representative for availability.

FIFO MEMORIES (cont'd)

CAPACITY	CONFIGURATION (WORDS × BITS)	MODEL NO.	OPERATING FREQUENCY (MHz)	ACCESS TIME (ns) MAX.	CYCLE TIME (ns) MIN.	POWER CONSUMPTION (mW) MAX. ACTIVE/ STANDBY	PACKAGE
18K	2,048 × 9	LH5498	40	15	25	550/28	28SK-DIP/28DIP/32PLCC
			33	20	30		
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
		LH540203	40	15	25	550/28	28SK-DIP/28DIP/28SOJ */ 32PLCC
			33	20	30		
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
	1,024 × 18	LH540225	67	11	15	550/28	68PLCC
			50	14	20		
			40	15	25		
			28	25	35		
36K	4,096 × 9	LH5499	33	20	30	550/44	28DIP/32PLCC
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
		LH540204	33	20	30	605/44	28SK-DIP/28DIP/28SOJ */ 32PLCC
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
		LH5492	40	20	25	825/138	32PLCC
			33	22	30		
			28	25	35		
		LH5493	33	22	30	825/138	32PLCC
			28	25	35		
		LH5494	33	22	30	825/138	32PLCC
			28	25	35		
	1,024 × 36	LH543620	50	14	20	TBD	132PQFP
			40	15	25		
			33	21	30		
72K	8,192 × 9	LH540205	33	20	30	605/44	28SK-DIP/28DIP
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		
144K	16,384 × 9	LH540206	33	20	30	605/44	28DIP
			28	25	35		
			22	35	45		
			15	50	65		
			12	65	80		
			10	80	100		

▒ Primary parameter for speed-grade specification.

* Contact your Sharp representative for availability.

QUALITY ASSURANCE

Quality Assurance System

Sharp develops and produces a wide range of consumer and industrial-use semiconductor products.

In recent years, the applications of ICs have expanded significantly, into fields where extremely high levels of quality are critical.

In response, Sharp has implemented a total quality assurance system that encompasses the entire production process from planning to after-sales service. This system ensures that quality is a priority in the planning development and production and guarantees product reliability through rigorous reliability testing. We compiled the "Sharp Semiconductor Reliability Handbook, IC Edition" to introduce you to the results of some of our research and to our quality and reliability philosophy and programs. We hope that it is informative and that it will help Sharp customers develop and refine their quality and reliability assurance and control activities. We will introduce a part of this system here.

Sharp's quality and reliability assurance activities are based on the following guidelines:

- All personnel should participate in quality assurance by continually cultivating a higher level of quality awareness.
- In the design and development stages of new products, create reliable designs that consider reliability in every respect.
- Quality control in all production processes, all working environments, materials, equipment, and measuring devices should be carefully monitored to ensure quality and reliability from the very beginning of the production process.
- Confirm long-term reliability and obtain a thorough understanding of practical limits through reliability testing.
- Continually work to improve quality through application of data from process inspections, reliability testing, and market surveys.

Quality Assurance During New Product Development

New product development ***(Figure 1)*** begins with an accurate grasp of the purpose, environment, and manners in which customers will use the product as well as the required reliability. A development plan is then drafted, clarifying the price, quantity, sales period and target reliability of the product to be manufactured.

Quality and reliability are built into the product from the beginning of the product cycle by introducing design review (DR) and reliability planning in the development and design stage. The first tasks undertaken in this stage are process development and circuitry design, by which a prototype, or technical sample (TS), is made. An evaluation of the technical sample is conducted, centering on the function and performance of the sample under conditions in which the final product will be used (TS evaluation).

Next, an engineering sample (ES) is made, based on the results of the TS evaluation, and it is subjected to ES evaluation. The ES evaluation consists of determining, under mass production conditions, whether the product functions and performs as intended during development and design. Reliability testing is also used to decide whether the engineering sample has the required degree of reliability.

In the final stage, the transfer of the product to mass production is discussed - based on the results of the TS and ES evaluations. Once TS and ES are accepted, preproduction begins. At this time, it is determined whether the quality and reliability obtained during development and design can be maintained, whether there are any discrepancies in the production process and what yields will be. The manufacturability of the product is determined, based on these results.

DR (Design Review) is performed to prevent faulty operation and to enhance the functions, usability, quality and reliability, upon completion of structural design, logic design, software design, circuit design, TS/ES evaluation and reliability tests.

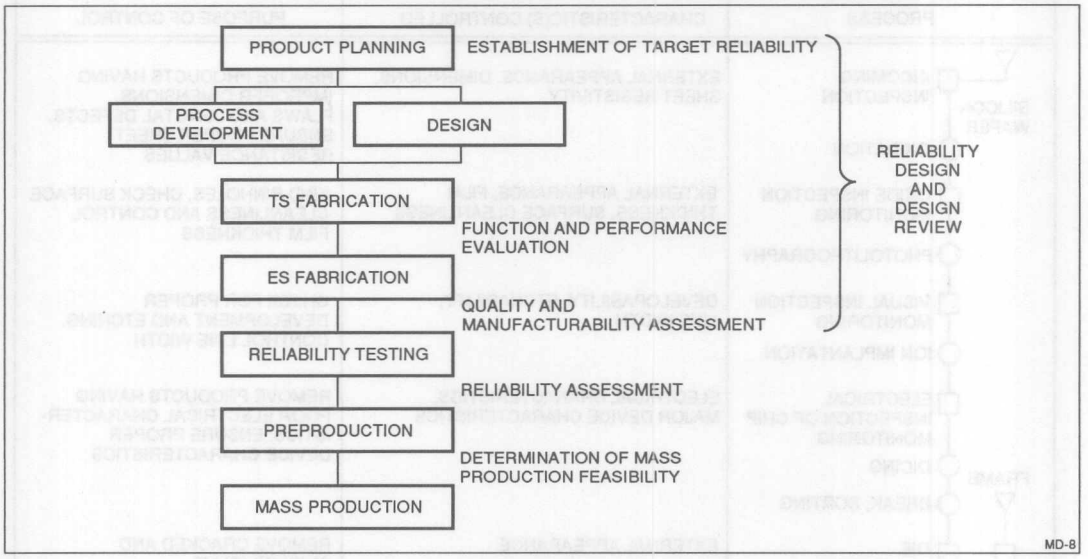


Figure 1. New Product Development Steps

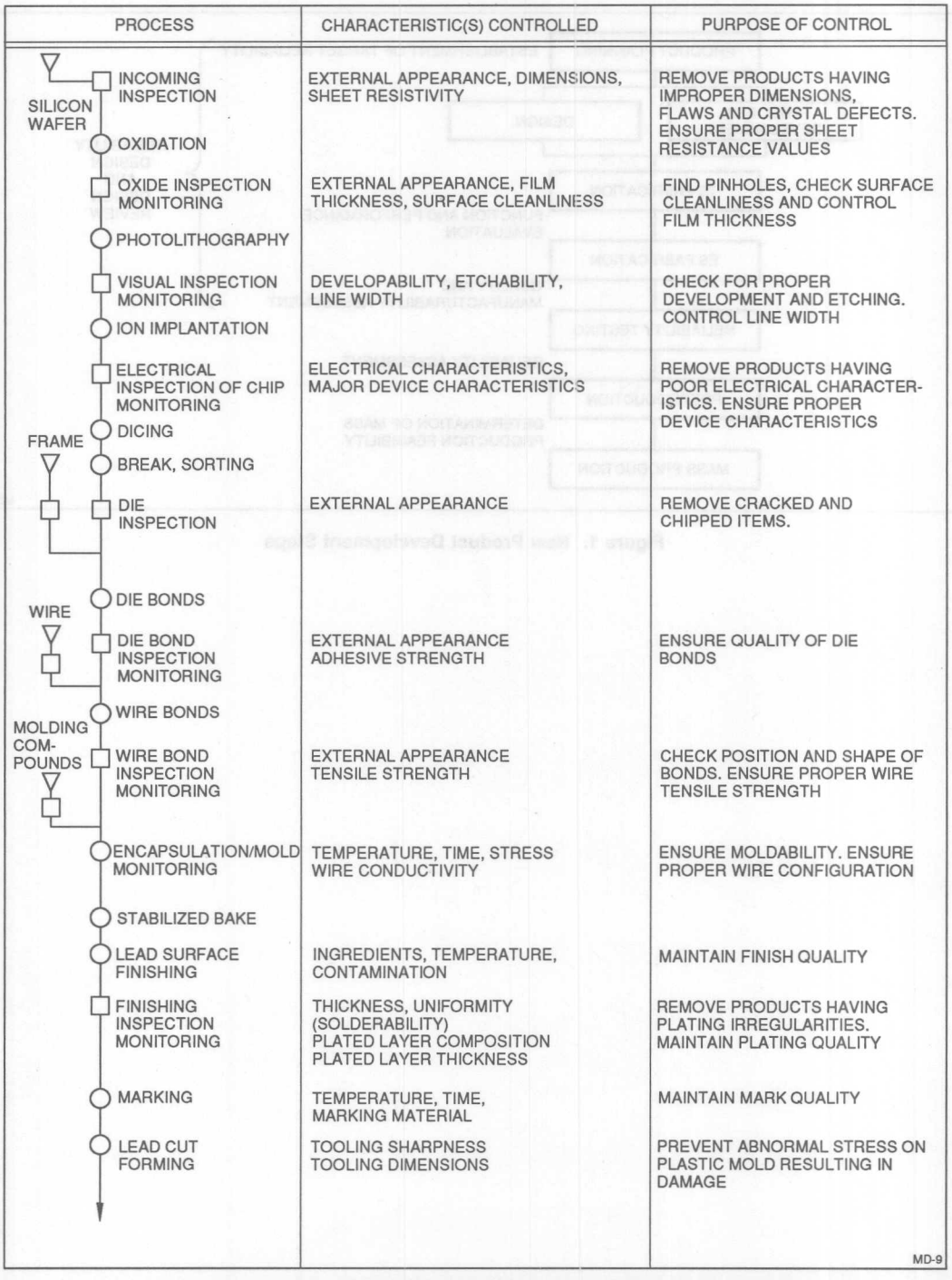


Figure 2. Example of the Quality Control Process

Raw Materials Control

The level of product quality and reliability is largely governed by the quality of the materials originally making up the production process and environment.

It is the responsibility of the vendor to execute the quality assurance of basic materials purchased by Sharp. Raw material quality assurance is conducted according to the following system:

- Initial selections of a raw material manufacturer.
- Quality qualification for each new material put into use (quality and reliability assessments of devices in which such new materials are used).
- Periodic quality consultations based on quality information obtained during mass production.

Acceptance inspections are carried out as necessary based on acceptance criteria derived from product specifications and approved drawings.

Control of the Manufacturing Environment

Integrated circuit devices are manufactured in a clean room where there is minimal air-born particulates. The use of ultrapure water also aids cleanliness. Such conditions are necessary due to the adhesion of even small bits of foreign particles (0.1 μm or less), no more than 1/5 - 1/10 the size of the smallest IC pattern, can result in defects later in the process.

Particulates not only affects chip yields, but can also have a lethal affect on the quality and reliablity of a device. Therefore, the cleanliness of every piece of equipment and facility in the plant as well as that of work clothes and work articles are controlled. Degree of cleanliness is usually expressed numerically as the number of particles over 0.5 μm per cubic foot of air.

The degree of cleanliness maintained in Sharp clean rooms, where wafers come in direct contact with air, is Class 1. Temperature and humidity are maintained at constant levels by continuous computer-controlled monitoring ***(Table 1).***

The ultrapure de-ionized (DI) water used in the wafer process is manufactured with an ultrapurification equipment, employing ion-exchange treatment, ultraviolet irradiation and ultrafiltration systems.

Table 1.
Clean Room Temperature & Humidity Standards

Temperature	24 ± 0.5°C
Humidity	45 ± 5% RH

Control of Facilities and Instrumentation

Intregrated circuit device technology is experiencing rapid revolutionary change, and advances in IC production facilities and equipment are equally impressive.

Process automation is promoted by using the latest CIM (Computer Intregrated Manufacturing) system to create devices having stable quality and to reduce variance of characteristics. In addition, production facilities maintenance control, and precision control for various instrumentation devices are implemented by both daily and periodic spot inspections.

Facilities' control is conceptually based on Total Productive Maintenance (TPM), in which all concerned employees systematically participate in facilities maintenance activities. Sharp's goal is to create a highly skilled human resource through activities such as:

- operator-initiated maintenance;
- scheduled maintenance;
- corrective maintenance.

Control of instrumentation devices is in accordance with Japanese national standards. Regular calibration by overseeing public agencies also helps maintain a high level of accuracy in these devices.

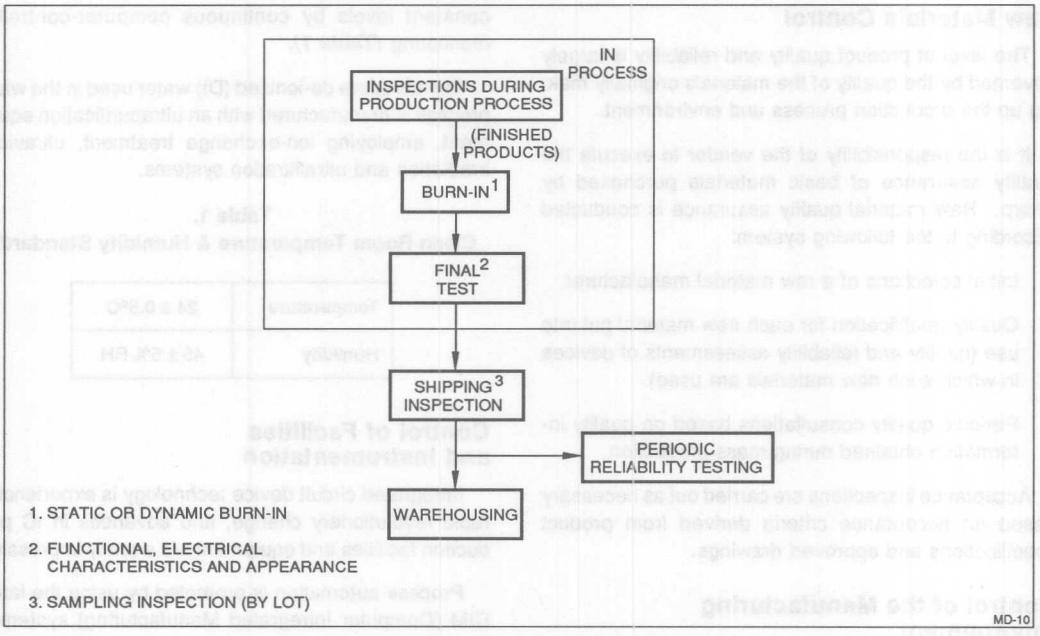


Figure 3. Product Inspection System

Quality Control During the Production Process

Designed-in quality and reliability must be faithfully built into a device during production to manufacture consistently high-quality and high-reliability products.

Production Operations are therefore based on specific, established operational standards. Checks are performed at each process step to decide whether specific characteristics have been obtained and quality has been built in. Each process is monitored to ensure that defectives are not sent to the next process. This is done by rigorously carrying out various standardized controls, appropriate to each process, such as monitoring, visual inspections and sampling inspections.

Sharp strongly promotes the automation of production facilities and equipment. Sharp works to prevent quality problems before they occur and to stabilize quality. Operations that required human skills in the past are now automated. Computer Integrated Manufacturing (CIM) is being introduced into the wafer process. CIM is used to implement comprehensive production control, including conveyance within a process, equipment monitoring and progress control. CIM enables several types of process data to be processed together. Control charts and process capacity index (Cpk) are computed in real time for individual pieces of equipment. Even minute fluctuations in characteristics are fed back to improve control.

Reliability is also being assessed by periodic sampling. This test is a long-term reliability assessment, and the results are fed back to the related divisions.

While quality assurance tests and inspections are conducted for improving and maintaining quality, they also are used to predict the probable reliability a product will have in the marketplace. They provide a multi-faceted approach to ensuring product quality.

Table 2.
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE &CONDITIONS	REFERENCE STANDARDS
Thermal Environment Tests	Soldering Heat	To determine soldering heat resistance. Standard test conditions: Solder bath temperature: 260 ± 5°C Time: 10 ± 1 sec. Solder composition: Pb:Sn = 4:6	JIS C 7022: A-1 MIL-STD-750 C 2031 IEC Pub. 68 Test Tb
	Temperature Cycling	To determine resistance to high and low temperatures and to temperature changes between these extremes. Standard test conditions: $T_a = T_{stg\ MIN} \sim T_{stg\ MAX}$ [gas environment]	JIS C 7022: A-4 MIL-STD-883 C 1010 IEC Pub. 68 Test Na, Nb
	Thermal Shock	To determine resistance to sudden changes in temperature. Standard test conditions: $T_a = T_{stg\ MIN} \sim T_{stg\ MAX}$ [liquid environment]	JIS C 7022: A-3 MIL-STD-883 C 1011 IEC Pub. 68 Test Nc
	Temperature & Humidity Cycling	To determine resistance to conditions of high temperature and high humidity. Standard test conditions: -10 ~ 65°C, 90 ~ 95% RH, one (1) cycle every 24 hours	JIS C 7022: A-5 MIL-STD-883 C 1004 IEC Pub. 68 Test Z/AD
Mechanical Environment Tests	Variable Frequency Vibration	To determine resistance to vibration during transportation and use. Standard test conditions: Cycle: 100 ~ 2000 H_z in 4 min. Peak acceleration: 20 G Orientation: four (4) times in each of the orientations of ± X, ± Y and ± Z	JIS C 7022: A-10 MIL-STD-883 C 2007 IEC Pub. 68 Test Fc
	Mechanical Shock	To determine resistance to shocks during transportation & use. Standard test conditions: Peak acceleration: 1500 G Pulse duration: 0.5 ms Orientation: three (3) pulses in each of the orientations ± X, ± Y and ± Z	JIS C 7022: A-7 MIL-STD-883 C 2002 IEC Pub. 68 Test Ea
	Constant Acceleration	To determine resistance to constant acceleration. Standard test conditions: Stress level: 20,000 G, Orientation: applied for one (1) min. in each of the orientations ± X, ± Y and ± Z	JIS C 7022: A-9 MIL-STD-883 C 2001 IEC Pub. 68 Test Ga
	Lead Integrity	To determine resistance to installation and handling such as wiring. (1) Tensile strength. Standard test conditions: A specified load is applied in a direction parallel to the lead axis for 10 ± 1 sec. (2) Bending strength. Standard test conditions: A specified load is applied to the tip of each lead and the lead is bent once each through a + and - 90° arc and back. (The specified load is determined by nominal cross section or nominal section modulus.) *TCP (tape carrier package): N/A	JIS C 7002: A-11 IEC Pub. 68 Test U

Table 2. (cont'd)
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE &CONDITIONS	REFERENCE STANDARDS
Mechanical Environment Tests	Solderability	To determine the solderability of leads which are connected by soldering. Standard test conditions: Solder bath temperature: 230 ± 5°C, Dip time: 5 ± 0.5 sec. Solder composition: Pb:Sn = 4:6, used with rosin flux.	JIS C 7022: A-2 MIL-STD-883 C 2003
	Seal (Hermeticity)	To determine the effectiveness of the seal of hermetically sealed devices. (1) Fine leak detection (helium): measured with a helium detector after storage in an He atmosphere at a prescribed pressure for a designated time period. (2) Gross leak observation (bubbles): observation of bubbles formed by a fluorocarbon or silicone oil.	JIS C 7022: A-6 MIL-STD-883 C 1014 IEC Pub. 68 Test Q
	Salt Atmosphere (Corrosion)	To determine resistance to corrosion in a salt fog. Standard test conditions: Exposure to salt spraying conditions of salt concentration, 5 ± 1%. Spray rate: 0.5 ~ 3 ml/80 cm^3/h Salt fog temperature: 35 ± 2°C for a designated period of time.	JIS C 7022: A-12 MIL-STD-883 C 1009 IEC Pub. 68 Test Ka
Life Tests	High Temperature Operation	To determine resistance to prolonged operating stress, electrical and thermal. Standard test conditions: $T_a = T_{op\ MAX}$ Operating source voltage = Max. operating voltage	JIS C 7022: B-1 MIL-STD-883 C 1005
	High Temperature Storage	To determine resistance to prolonged high temperature storage. Standard test conditions: $T_a = T_{stg\ MAX}$	JIS C 7022: B-3 MIL-STD-883 C 1008
	Low Temperature Storage	To determine resistance to prolonged low temperature storage. Standard test conditions: $T_a = T_{stg\ MIN}$	JIS C 7022: B-4 IEC Pub. 68 Test A
	High Temperature/ High Humidity Bias	To determine resistance to prolonged temperature, humidity and electrical stress. Standard test conditions: 85°C, 85% RH Applied voltage = $V_{TYPICAL}$	JIS C 7022: B-5 IEC Pub. 68 Test C
	High Temperature/ High Humidity Storage	To determine resistance to prolonged storage at high temperature and humidity. Standard test conditions: (1) 60°C, 90% RH (2) 85°C, 85% RH	JIS C 7022: B-5 IEC Pub. 68 Test C

Table 2. (cont'd)
Reliability Test Items

CLASSIFICATION	TEST	PURPOSE &CONDITIONS	REFERENCE STANDARDS
Miscellaneous	Pressure Cooker (PCT)	To evaluate moisture resistance in a short period of time. Standard test conditions: 121°C, 2atm, no electrical load. 100% RH	EIAJ IC-121: 18
	Composite Test	Several tests (selected from those listed above) performed in series to effectively evaluate product. Example: for a surface mount device: High-Temperature/High-Humidity Storage→Soldering Heat Resistance→Pressure cooker (PCT)	
	Electrostatic Discharge Strength	To determine resistance to electrostatic stress. Standard test conditions: (1) Human body model: Earth capacity C = 100 pF, equivalent Resistance R = 1.5 kΩ (2) Machine model: Earth capacity C = 200 pF, equivalent Resistance R = 0Ω	MIL-STD-883 C 3015 EIAJ IC-121:20
	Latch-Up Strength	To determine resistance to latch-up. Standard test conditions: (1) Condenser charge (2) Current application (3) V_{CC} overvoltage application	

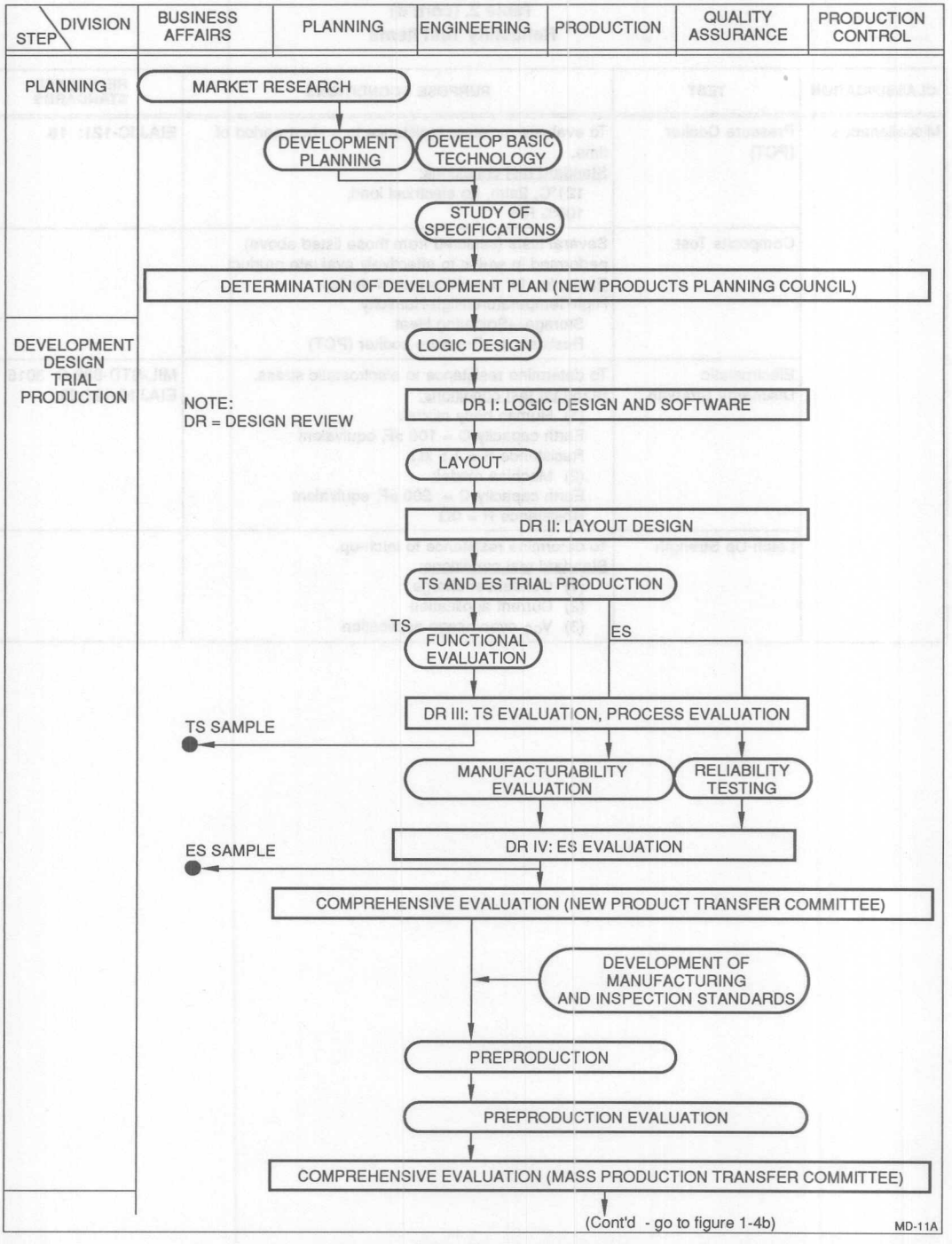


Figure 4a. Quality Assurance System

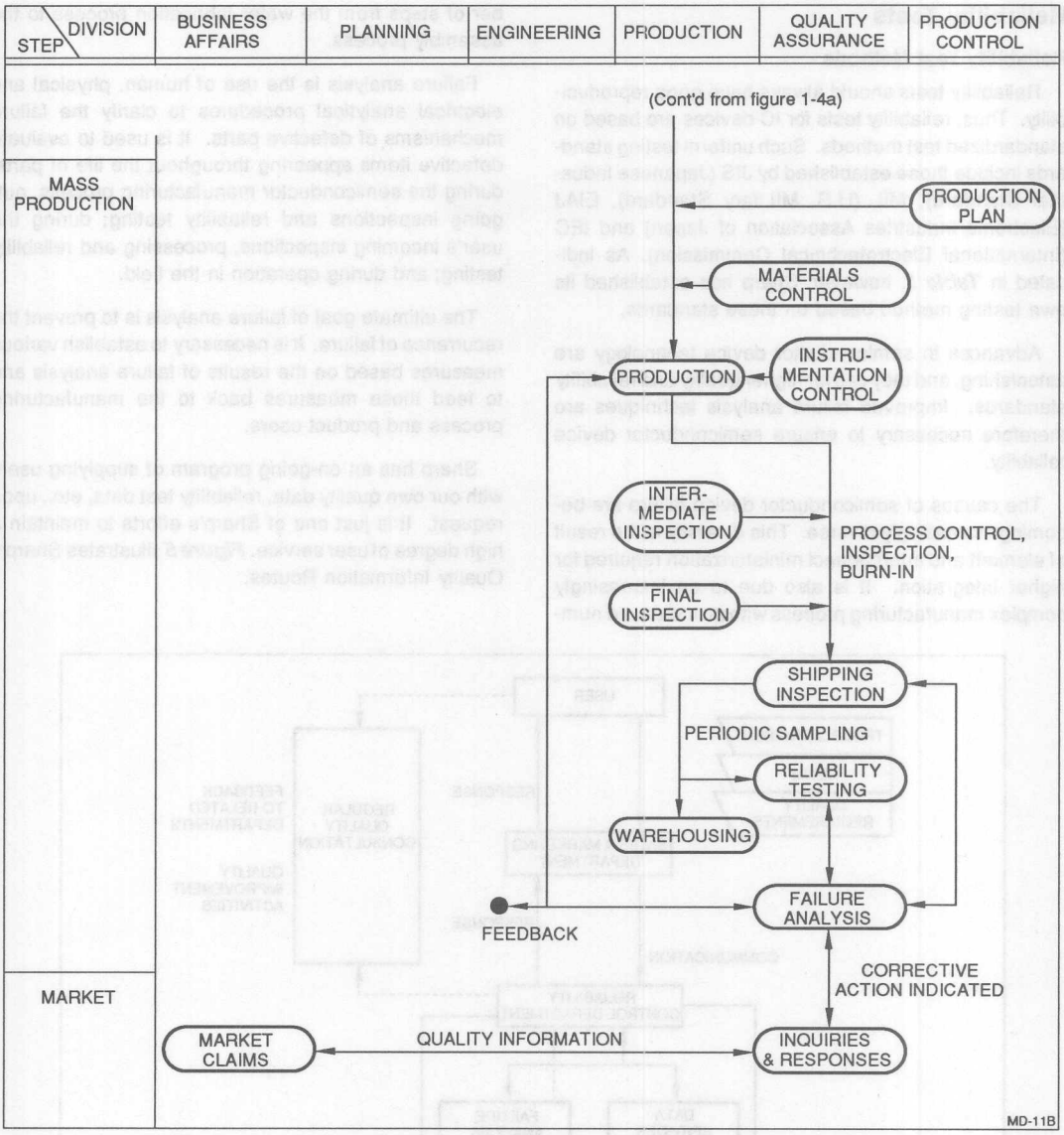


Figure 4b. Quality Assurance System

Reliability Tests

Reliability Test Methods

Reliability tests should always have good reproducibility. Thus, reliability tests for IC devices are based on standardized test methods. Such uniform testing standards include those established by JIS (Japanese Industrial Standard), MIL (U.S. MILitary Standard), EIAJ (Electronic Industries Association of Japan) and IEC (International Electrotechnical Commission). As indicated in ***Table 2***, however, Sharp has established its own testing method based on these standards.

Advances in semiconductor device technology are astonishing, and they call for higher quality and reliability standards. Improved failure analysis techniques are therefore necessary to ensure semiconductor device reliablity.

The causes of semiconductor device failure are becoming increasingly diverse. This diversity is the result of element and interconnect miniaturization required for higher integration. It is also due to an increasingly complex manufacturing process with an increased number of steps from the wafer fabrication process to the assembly process.

Failure analysis is the use of human, physical and electrical analytical procedures to clarify the failure mechanisms of defective parts. It is used to evaluate defective items appearing throughout the life of parts: during the semiconductor manufacturing process, outgoing inspections and reliability testing; during the user's incoming inspections, processing and reliability testing; and during operation in the field.

The ultimate goal of failure analysis is to prevent the recurrence of failure. It is necessary to establish various measures based on the results of failure analysis and to feed those measures back to the manufacturing process and product users.

Sharp has an on-going program of supplying users with our own quality data, reliability test data, etc., upon request. It is just one of Sharp's efforts to maintain a high degree of user service. ***Figure 5*** illustrates Sharp's Quality Information Routes.

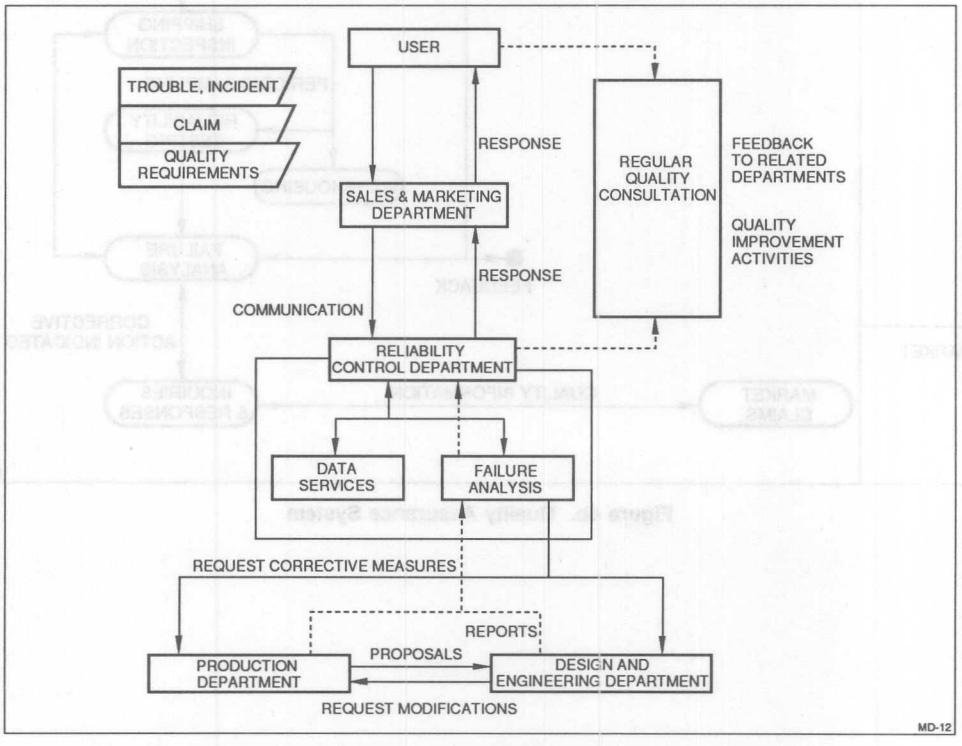


Figure 5. Routes through which malfunctions outside the company are handled.

Handling Precautions

All the semiconductor products listed in this data book are manufactured based on exacting designs and under comprehensive quality control. However, to take full advantage of the features offered and to assure each products' long-life service, please refer to the following items.

Maximum Ratings

It is generally known that the failure rate of semiconductor products increases as the temperature increases. It is therefore necessary that the ambient temperature be within the maximum rated temperature. Further, it is desirable from the stand-point of reliability that the ambient temperature be lowered as much as possible. The voltage, current, and electric power used are also factors that significantly influence the life of semiconductor products. Voltage or current that exceeds the rated level may damage the semiconductor product; even if applied only momentarily and the unit continues to operate properly, excessive voltage or current will likely increase the failure rate.

Therefore, in actual circuit design, it is important that the semiconductor products have an allowance with respect to the voltage, current and temperature conditions under which they will be used. The greater this allowance, the fewer the failures that will occur.

To keep failures to a minimum, the circuit should be designed so that under all conditions to absolute maximum, the ratings are not exceeded even momentarily and so that the maximum values for any two or more items are not achieved simultaneously. In addition, remember that the circuit functions of semiconductor products are guaranteed within the operating temperature range (Topr) or the absolute maximum ratings, but that storage temperature (Tstg) is the range in a non-operating condition.

Storage Precautions

General Storage Precautions

a. Storing product in the packing in which it is shipped is recommended. If transferred to a different container, use one that will not readily carry an electrostatic charge.

b. Store at conditions of normal temperature (5 - 35°C) and normal humidity (45 - 75% RH).

c. Avoid storing product in the presence of corrosive gases or dusty areas.

d. Avoid storing product in areas of direct sunlight or where sudden temperature changes will occur.

e. Avoid stacking product or otherwise applying heavy loads.

f. In the case of extended storage, take particular care against corrosion and deterioration in lead solderability. Inspecting such product before use is recommended.

Basic Electrostatic Discharge Countermeasures

Semiconductor device mounting requires exacting precautions to avoid applying excessive static electricity to the semiconductor. Item (a) - (c) below are basic electrostatic discharge countermeasures.

a. Use humidifiers and the like to ensure against excessively low relative humidity in the work environment. (Maintaining relative humidity consistently above 50% is ideal).

b. To prevent sudden electrostatic discharge, spread high-resistance electroconductive mats (about $10^6\Omega$) over workbenches and have workers wear wrist (ground) straps.

Have workers wear clothing made of charge-resistant cotton, noncharging materials (10^9 - $10^{14}\Omega$) or static electricity dissipating materials (10^5 - $10^9\Omega$). Antistatic foot apparel is also effective.

c. Ionizers (ionized air blowers) are effective when it is difficult to discharge static electricity from mounting equipment, contacting dielectrics and semiconductors.

Sharp recommends using static electricity measuring devices to quantify electrostatic charges and develop effective countermeasures.

When forming the lead wires of semiconductor products to be mounted, forceps or a similar tool that will prevent stress from being applied to the base of the wires should be used.

To prevent the input terminals of semiconductor products on completed printed circuit boards from becoming open during storage or transport, the terminals of the circuit board should be shortcircuited or the entire circuit board itself should be wrapped in aluminium foil.

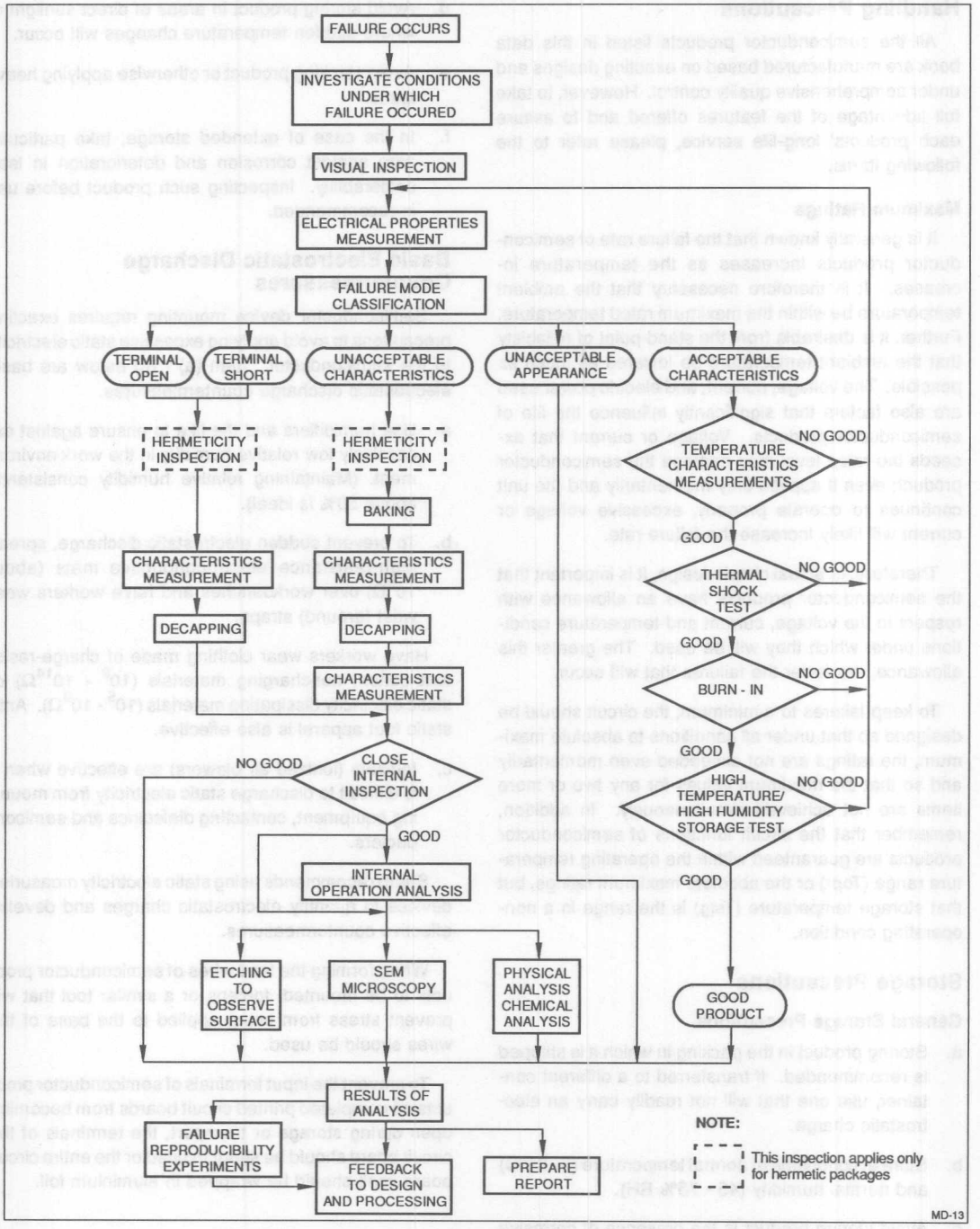


Figure 6. Failure Analysis Procedure

Soldering and Cleaning

When a semiconductor product is solder-bonded, specify the best conditions according to ***Table 4.*** If using a soldering iron, use one that doesn't leak from the soldering tip. An 'A Class' soldering iron with an insulation resistance of less than 10 MΩ is recommended. When using a solder bath, it should be grounded to prevent an unstable electric potential.

Using a strongly acidic or alkaline flux for soldering can cause corrosion of the lead wires. A rosin flux is ideal for this type of soldering.

To assure the reliability of a system, removal of the solder flux is generally required.

To prevent stress of semiconductor products and circuit boards when using ultrasonic cleaning, a cleaning method must be used that will shadow the main unit from the vibrator and specify the best conditions according to the following:

Table 3.
Recommended Conditions for PC Board Cleaning

Ultrasonic Power	less than 25 W/l
Cleaning Conditions	less than one minute total
Cleaning Solution Temperature	15 to 40°C

Adjustment and Tests

When the set is to be adjusted and tested upon completion of the printed circuit board, the printed circuit board must be checked to ensure that there are no solder bridges or cracks before the power is turned on. Also, if the market-rated voltage and current are to be used, it is wise to use a current limiter.

Whenever a printed circuit board is to be removed or mounted, or mounted on a socket, the power must be turned off.

When testing with a probe, care must be taken to assure that the probe does not come in contact with other signals or the power supply. If the test location has been decided beforehand, it is wise to set up a specially designed test-pin for testing.

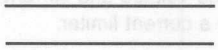
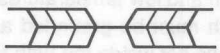
When testing in high and low temperatures, the constant-temperature bath must be grounded and measures taken to protect the set inside the bath from static electricity.

Table 4 outlines the semiconductor bonding and testing methods.

Table 4.
Semiconductor Bonding and Testing Methods

BONDING METHOD	TEMPERATURE AND TIME	TEST POSITION
Infrared reflow	Peak temp. 240°C or less 230°C or more within 15 sec. Heating speed: 1 to 4°C/sec.	Surface IC package
Flow dipping	245°C or less Within 3 sec./cycle Within 5 sec. in total	Solder bath
VPS	215°C or less 250°C or less, within 40 sec.	Steam
Hand soldering	260°C or less, within 10 sec.	IC outer lead

TIMING DIAGRAM CONVENTIONS

TIMING DIAGRAM	INPUT FUNCTIONS	OUTPUT FUNCTIONS
	HIGH or LOW	HIGH or LOW
	HIGH-to-LOW transitions allowed	HIGH-to-LOW transitions during designated interval
	LOW-to-HIGH transitions allowed	LOW-to-HIGH transitions during designated interval
	Don't care	State unknown or changing
	(Does not apply)	Centerline is high-impedance

MD-14

GENERAL INFORMATION – 1

PSEUDO-STATIC RAMs – 2

STATIC RAMs – 3

MASK-PROGRAMMABLE ROMS – 4

FIFO MEMORIES – 5

APPLICATION NOTES AND CONFERENCE PAPERS – 6

PACKAGING – 7

PSEUDO-STATIC RAMs

	Density	Organization	Page
LH5P832	256K	32K × 8	2-1
LH5P8129	1M	128K × 8	2-8
LH5P8128	1M	128K × 8	2-20
LH5P8128	4M	512K × 8	2-32

LH5P832

CMOS 256K (32K × 8) Pseudo-Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time: 120 ns (MAX.)
- Cycle time: 190 ns (MIN.)
- Power consumption:
  Operating: 303 mW
  Standby: 16.5 mW
- TTL compatible I/O
- 256 refresh cycle/4 ms
- Auto refresh is executed by internal counter (controlled by $\overline{OE}$/RFSH pin)
- Self refresh is executed by internal timer
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 300-mil SK-DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH5P832 is a 256K bit Pseudo Static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5P832 uses convenient on-chip refresh circuitry with a DRAM memory cell for pseudo static operation. This simplifies external clock inputs, while providing the same simple, non-multiplexed pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, many 32K × 8 SRAM sockets can be filled with the LH5P832 with little or no changes. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P832 PSRAM has the ability to fill the gap between DRAM and SRAM by offering low cost, low standby power, and a simple interface.

Three methods of refresh control are provided for maximum versatility. A 'CE-Only' refresh cycle refreshes the addressed row of memory cells transparently. All 256 rows must be refreshed or accessed every four milliseconds. 'Auto Refresh' automatically cycles through a different row on every OE/RFSH clock pulse, accomplishing the row refreshes without the need to supply row addresses externally. 'Self Refresh' further simplifies the refresh requirements by eliminating the need for address inputs and clock pulses entirely. An automatic timer senses time periods when memory accesses have ceased, and provides full refresh of all rows of memory without any external assistance.

PIN CONNECTIONS

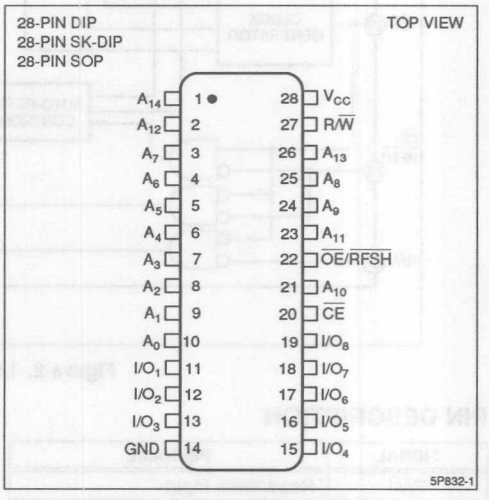


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

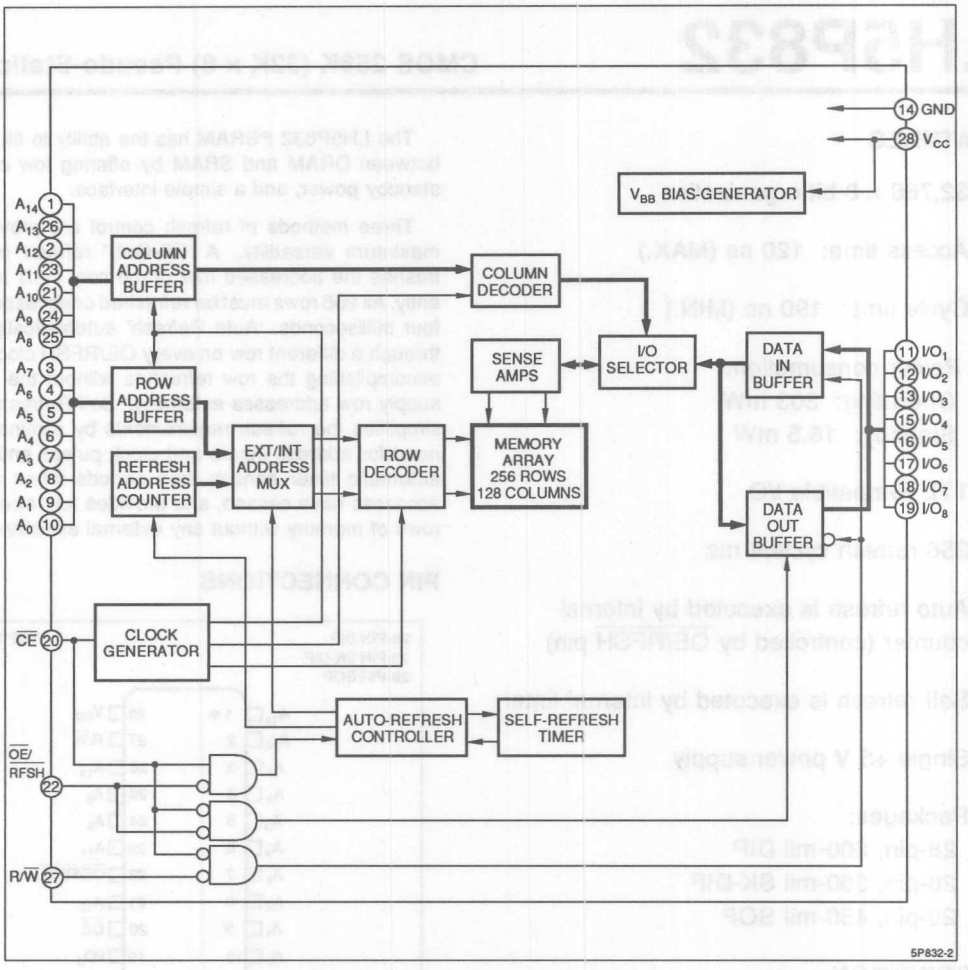


Figure 2. LH5P832 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
R/$\overline{W}$	Read/Write input
$\overline{OE}$/$\overline{RFSH}$	Output Enable/Refresh input
I/O_1 - I/O_8	Data inputs and outputs
A_0 - A_7	Row address inputs

SIGNAL	PIN NAME
A_8 - A_{14}	Column Address inputs
$\overline{CE}$	Chip Enable input
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$/$\overline{RFSH}$	MODE	I/O_1 - I/O_8	I_{CC}	NOTE
L	L	X	Write	Data in	Operating (I_{CC})	1
L	H	L	Read	Data out	Operating (I_{CC})	
L	H	H	$\overline{CE}$-Only Refresh	High-Z	Operating (I_{CC})	
H	X	L	Auto Refresh	High-Z	Operating	1, 2
H	X	L	Self Refresh	High-Z	Standby	1, 3

NOTES:
1. X = H or L 2. $\overline{OE}$ Pulsewidth < 8 µs 3. $\overline{OE}$ Pulsewidth ≥ 8 µs

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pin	V_T	-1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Power consumption	P_D	600	mW	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. Referenced to GND

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		+0.8	V

CAPACITANCE (V_{CC} = 5.0 V ± 10%, T_A = 0 to +70°C, f = 1MHz)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{14}, R/$\overline{W}$	C_{IN1}		8	pF
	$\overline{CE}$, $\overline{OE}$/$\overline{RFSH}$	C_{IN2}		5	pF
Input/output capacitance	I/O_1 - I/O_8	C_{OUT1}		12	pF

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	I_{CC1}	t_{RC} = 190 ns		55	mA	1
Standby current	I_{CC2}	$\overline{CE}$ = V_{IH}, $\overline{OE}$/$\overline{RFSH}$ = V_{IH}		3	mA	1
Self refresh average current	I_{CC3}	$\overline{CE}$ = V_{IH}, $\overline{OE}$/$\overline{RFSH}$ = V_{IL}		3	mA	
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V	-10	10	µA	
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V	-10	10	µA	1
Output High voltage	V_{OH}	I_{OUT} = -1 mA	2.4		V	
Output Low voltage	V_{OL}	I_{OUT} = 4 mA		0.4	V	

NOTES:
1. The output pins are in high-impedance state.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	5 ns
Timing reference level	1.5 V
Output load conditions	1TTL gate, C_L = 100 pF (Includes scope and jig capacitance)

AC CHARACTERISTICS

READ AND WRITE CYCLES [1,2] (V_{CC} = 5.0 V ± 10%, T_A = 0 to 70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Random read, write cycle time	t_{RC}	190		ns	
Read modify write cycle time	t_{RMW}	280		ns	
$\overline{CE}$ pulse width	t_{CE}	120	10,000	ns	
$\overline{CE}$ precharge time	t_P	60		ns	
Address setup time	t_{AS}	0		ns	
Address hold time	t_{AH}	30		ns	
Read command hold time	t_{RCH}	0		ns	
Read command setup time	t_{RCS}	0		ns	
$\overline{CE}$ access time	t_{CEA}		120	ns	
$\overline{OE}$ access time	t_{OEA}		50	ns	
$\overline{CE}$ to output in Low-Z	t_{CLZ}	10		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		ns	
Output enable from end of write	t_{WLZ}	0		ns	
Chip disable to output in High-Z	t_{CHZ}	0	35	ns	2
Output disable to output in High-Z	t_{OHZ}	0	35	ns	2
Write enable to output in High-Z	t_{WHZ}	0	35	ns	2
$\overline{OE}$ setup time	t_{OES}	10		ns	
$\overline{OE}$ hold time	t_{OEH}	0		ns	
$\overline{OE}$ lead time	t_{OEL}	10		ns	
Write command pulse width	t_{WCP}	85		ns	
Write command setup time	t_{WCS}	85		ns	
Write command hold time	t_{WCH}	85		ns	
Data setup time from write	t_{DSW}	50		ns	
Data setup time from $\overline{CE}$	t_{DSC}	50		ns	
Data hold time from write	t_{DHW}	0		ns	
Data hold time from $\overline{CE}$	t_{DHC}	0		ns	
Transition time (rise and fall)	t_T	3	35	ns	
Refresh time interval	t_{REF}		4	ms	

REFRESH CYCLE

Auto refresh cycle time	t_{FC}	190		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	60		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	80	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		ns	
$\overline{CE}$ delay time from refresh active (Auto refresh)	t_{FCE}	225		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	225		ns	

NOTES:

1. At least 1 ms of pause time after power on should be given for proper device operation. $\overline{CE}$ and $\overline{OE}$/RFSH must be fixed at V_{IH} for 1 ms from the V_{DD} reached to the specified voltage level.
2. Active output to high-Z and high-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

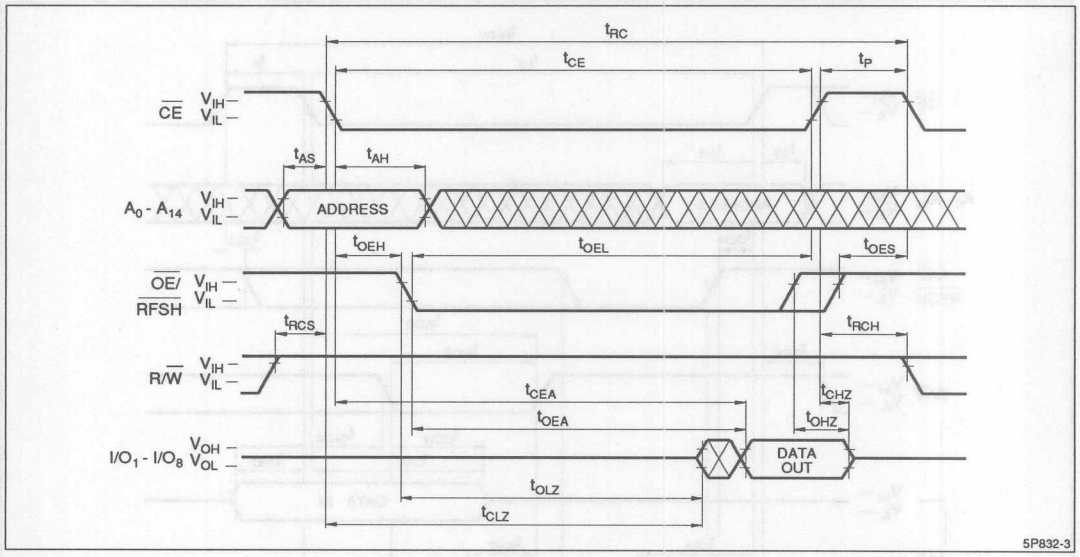


Figure 3. Read Cycle

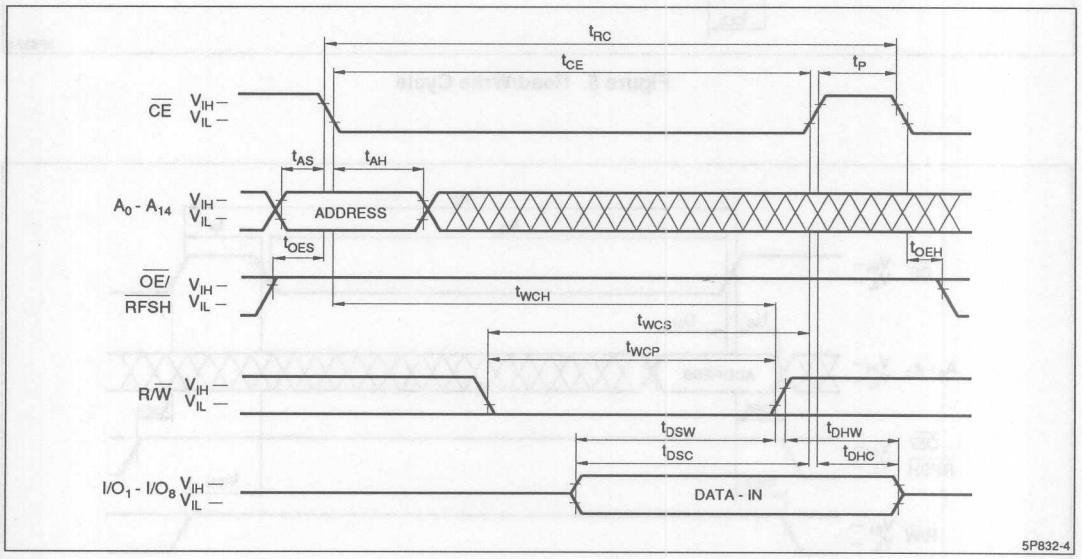


Figure 4. Write Cycle

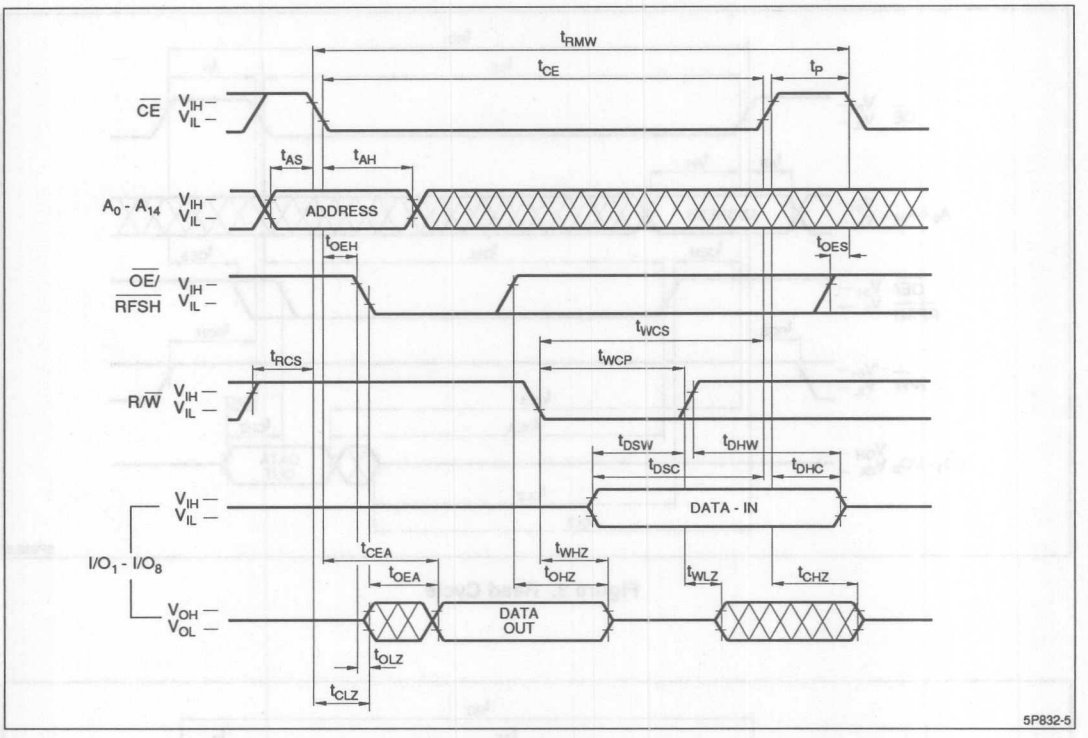


Figure 5. Read/Write Cycle

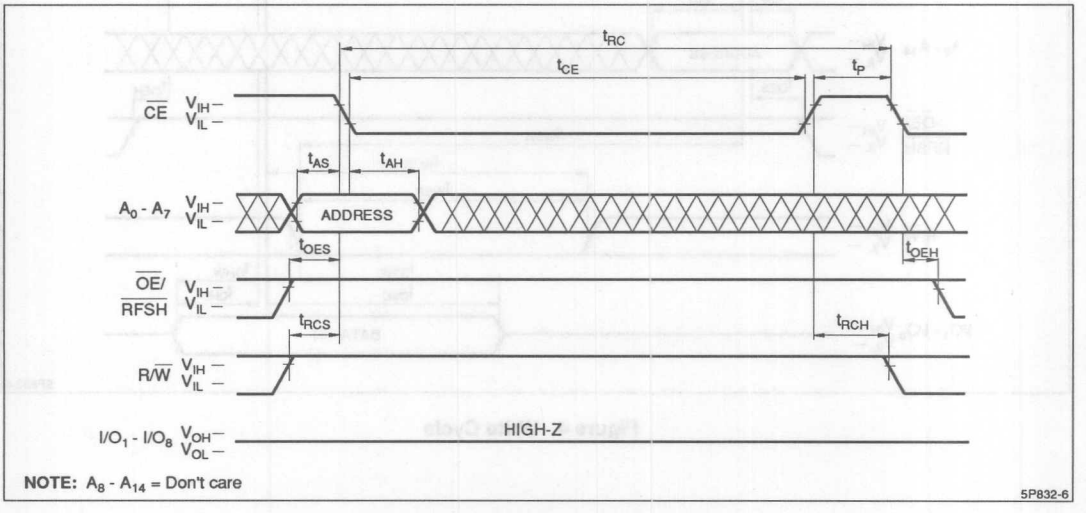


Figure 6. $\overline{CE}$ Only Refresh Cycle

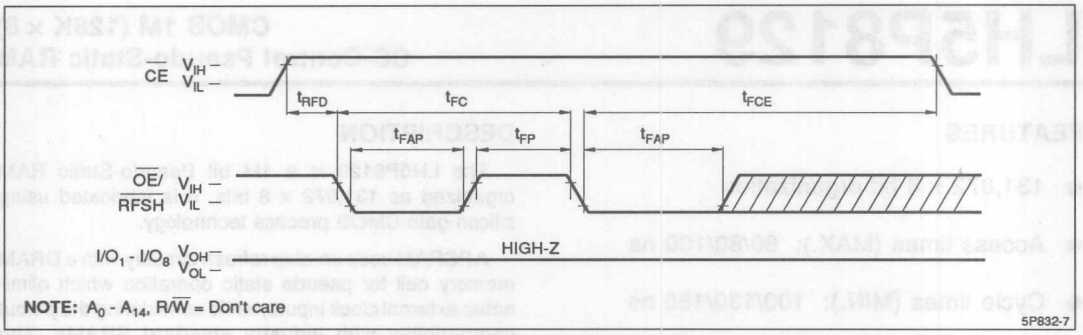


Figure 7. Auto Refresh Cycle

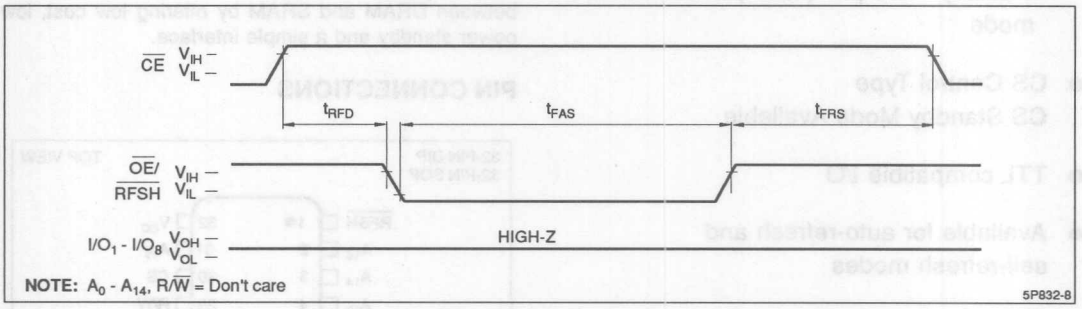
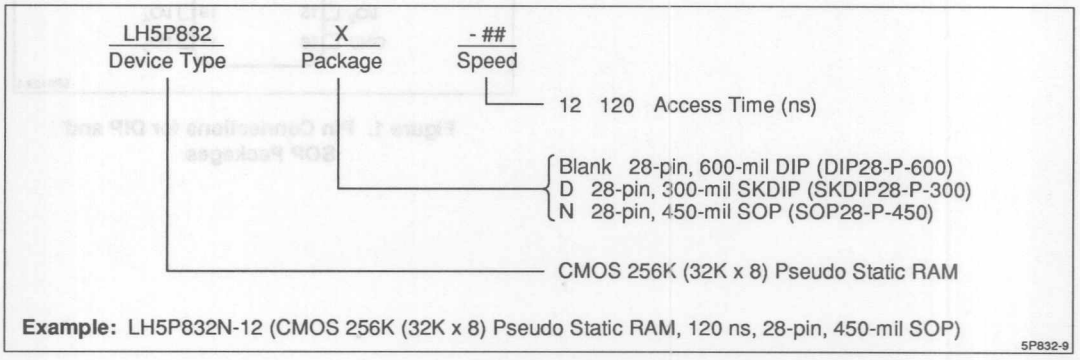


Figure 8. Self Refresh Cycle

ORDERING INFORMATION



PRELIMINARY

LH5P8129

CMOS 1M (128K × 8)
CS-Control Pseudo-Static RAM

FEATURES

- 131,072 × 8 bit organization
- Access times (MAX.): 60/80/100 ns
- Cycle times (MIN.): 100/130/160 ns
- Power consumption:
  Operating: 572/440/358 mW (MAX.)
  Standby: 275 µW (MAX.) in self-refresh mode
- CS Control Type
  CS Standby Mode Available
- TTL compatible I/O
- Available for auto-refresh and self-refresh modes
- 512 refresh cycles/8 ms
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type I)
  (normal and reverse bend pins)

DESCRIPTION

The LH5P8129 is a 1M bit Pseudo-Static RAM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

A PSRAM uses on-chip refresh circuitry with a DRAM memory cell for pseudo static operation which eliminates external clock inputs, while considering the pinout compatibility with industry standard SRAMs. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P8129 PSRAM has the ability to fill the gap between DRAM and SRAM by offering low cost, low power standby and a simple interface.

PIN CONNECTIONS

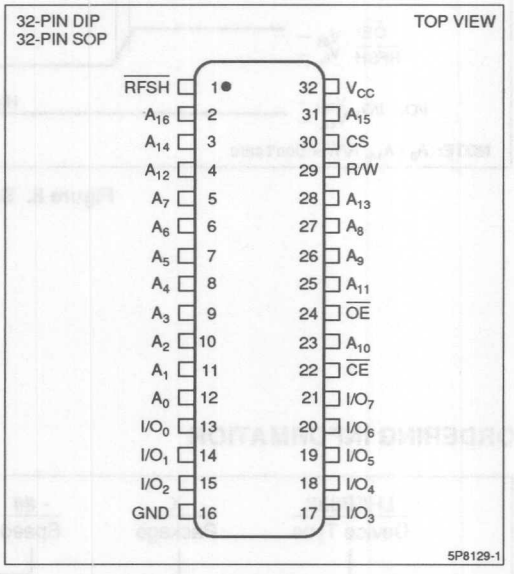


Figure 1. Pin Connections for DIP and SOP Packages

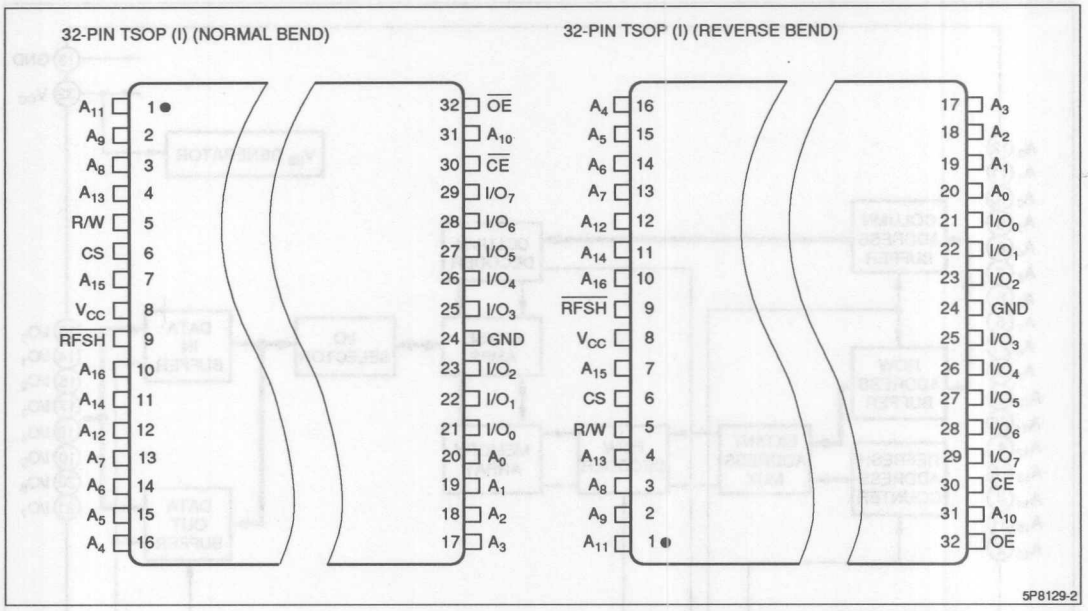


Figure 2. Pin Connections for TSOP Packages

TRUTH TABLE

$\overline{CE}$	CS	$\overline{OE}$	R/W	$\overline{RFSH}$	A_0 - A_{16}	I/O_1 - I/O_8	MODE
L	H	L	H	H	VX	D_{OUT}	Read
L	H	X	L	H	VX	D_{IN}	Write
L	H	H	H	H	VX	High-Z	$\overline{CE}$ only refresh
L	L	X	X	X	X	High-Z	CS standby
H	X	X	X	L	X	High-Z	Auto/Self refresh
H	X	X	X	H	X	High-Z	Standby

NOTES:

H = High at V_{IN} = VCC + 0.3 V to V_{IH} (MIN.)
L = Low at V_{IN} = V_{IL} (MAX.) to -1.0 V
X = Don't care at V_{CC} + 0.3 V to -1.0 V
VX = Input when $\overline{CE}$ = L, then Don't Care

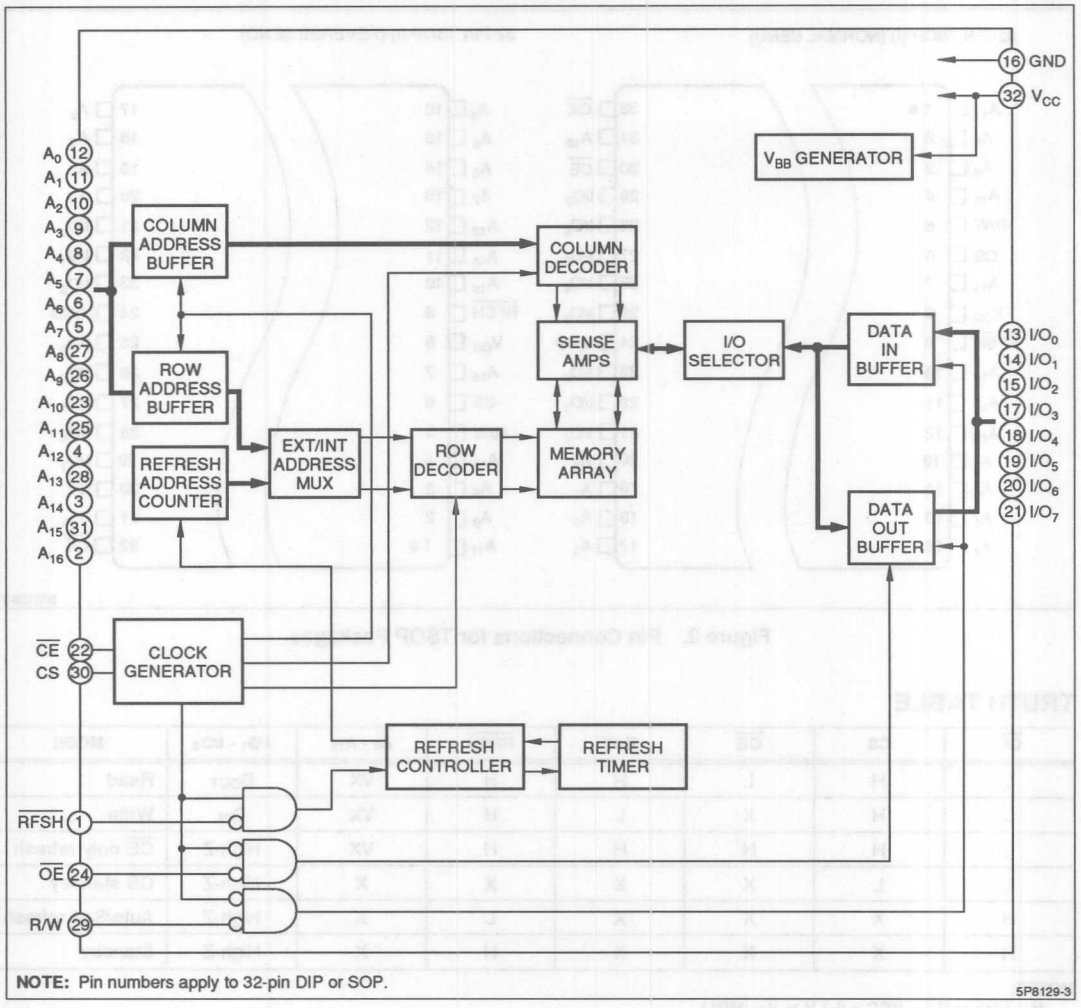


Figure 3. LH5P8129 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
R/W	Read/Write input
$\overline{OE}$	Output Enable input
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
CS	Chip Select input
$\overline{RFSH}$	Refresh input
I/O_0 - I/O_7	Data input/output

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pins	V_T	-1.0 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	
Output short circuit current	I_O	50	mA	
Power consumption	P_D	600	mW	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		0.8	V

CAPACITANCE (T_A = 0 to +70°C, f = 1MHz, V_{CC} = 5.0 V ± 10%)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{16}	C_{IN1}		8	pF
	R/W, $\overline{OE}$	C_{IN2}		5	pF
	$\overline{CE}$, CS	C_{IN3}		5	pF
	$\overline{RFSH}$	C_{IN4}		5	pF
Input/output capacitance	I/O_0 - I/O_7	C_{OUT1}		10	pF

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

PARAMETER		SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	LH5P8129-60	I_{CC1}	tRC = t_{RC} (MIN)		104	mA	1, 2
	LH5P8129-80				80		
	LH5P8129-10				65		
Standby current	TTL Input	I_{CC2}			1	mA	1, 3
	CMOS Input				0.05		1, 4
Self-refresh average current	TTL Input	I_{CC3}			1	mA	1, 5
	CMOS Input				0.05		1, 6
CPU internal cycle average current	LH5P8129-60	I_{CC4}	(R/W = $\overline{OE}$ = V_{IH})		104	mA	1, 2
	LH5P8129-80				80		
	LH5P8129-10				65		
Input leakage current		I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other test pins	-10	10	µA	
I/O leakage current		I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V Output in high-impedance state	-10	10	µA	
Output HIGH voltage		V_{OH}	I_{OUT} = 1 mA	2.4		V	
Output LOW voltage		V_{OL}	I_{OUT} = 4 mA		0.4	V	

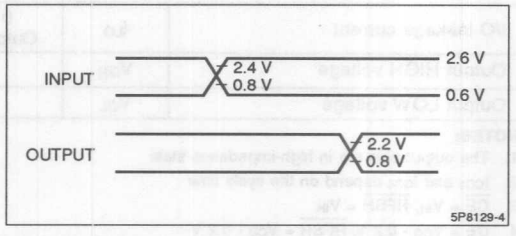
NOTES:
1. The output pins are in high-impedance state
2. I_{CC1} and I_{CC4} depend on the cycle time
3. $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IH}
4. $\overline{CE}$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = V_{CC} - 0.2 V
5. $\overline{CE}$ = V_{IH}, $\overline{RFSH}$ = V_{IL}
6. $\overline{CE}$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = 0.2 V

AC ELECTRICAL CHARACTERISTICS [1,2,3] (T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

PARAMETER	SYMBOL	LH5P8129-60		LH5P8129-80		LH5P8129-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read, write cycle time	t_{RC}	100		130		160		ns	
Read modify write cycle time	t_{RMW}	155		195		235		ns	
$\overline{CE}$ pulse width	t_{CE}	60	10,000	80	10,000	100	10,000	ns	
$\overline{CE}$ precharge time	t_P	30		40		50		ns	
Address setup time	t_{AS}	0		0		0		ns	4
Address hold time	t_{AH}	15		20		25		ns	4
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
$\overline{CE}$ access time	t_{CEA}		60		80		100	ns	5
$\overline{OE}$ access time	t_{OEA}		25		30		35	ns	5
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20		20		20		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		0		0		ns	
Output enable from end of write	t_{WLZ}	0		0		0		ns	
Chip disable to output in High-Z	t_{CHZ}		20		25		30	ns	
Output disable to output in High-Z	t_{OHZ}		20		25		30	ns	
Write enable to output in High-Z	t_{WHZ}		20		25		30	ns	
$\overline{OE}$ setup time	t_{OES}	0		0		0		ns	
$\overline{OE}$ hold time	t_{OEH}	10		10		10		ns	
CS setup time	t_{CSS}	0		0		0		ns	
CS hold time	t_{CSH}	15		20		25		ns	
Write command pulse width	t_{WP}	30		30		30		ns	
Write command setup time	t_{WCS}	30		30		30		ns	
Write command hold time	t_{WCH}	40		50		60		ns	
Data setup time from write	t_{DSW}	25		30		35		ns	6
Data setup time from $\overline{CE}$	t_{DSC}	25		30		35		ns	6
Data hold time from write	t_{DHW}	0		0		0		ns	6
Data hold time from $\overline{CE}$	t_{DHC}	0		0		0		ns	6
Transition time (rise and fall)	t_T	3	35	3	35	3	35	ns	
Refresh time interval	t_{REF}		8		8		8	ms	
Refresh command hold time	t_{RHC}	15		15		15		ns	
Auto refresh cycle time	t_{FC}	100		130		160		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	30		40		50		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	30	8,000	30	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		30		30		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		8,000		8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	140		160		190		ns	

NOTES:

1. In order to initialize the circuit, $\overline{CE}$ should be kept in V_{IH} for 100 µs after power-up.
2. AC characteristics are measured at t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right).
4. Address is latched at the negative edge of $\overline{CE}$.
5. Measured with a load equivalent to 2TTL + 100 pF.
6. Data is latched at the positive edge of W/R or at the positive edge of $\overline{CE}$.



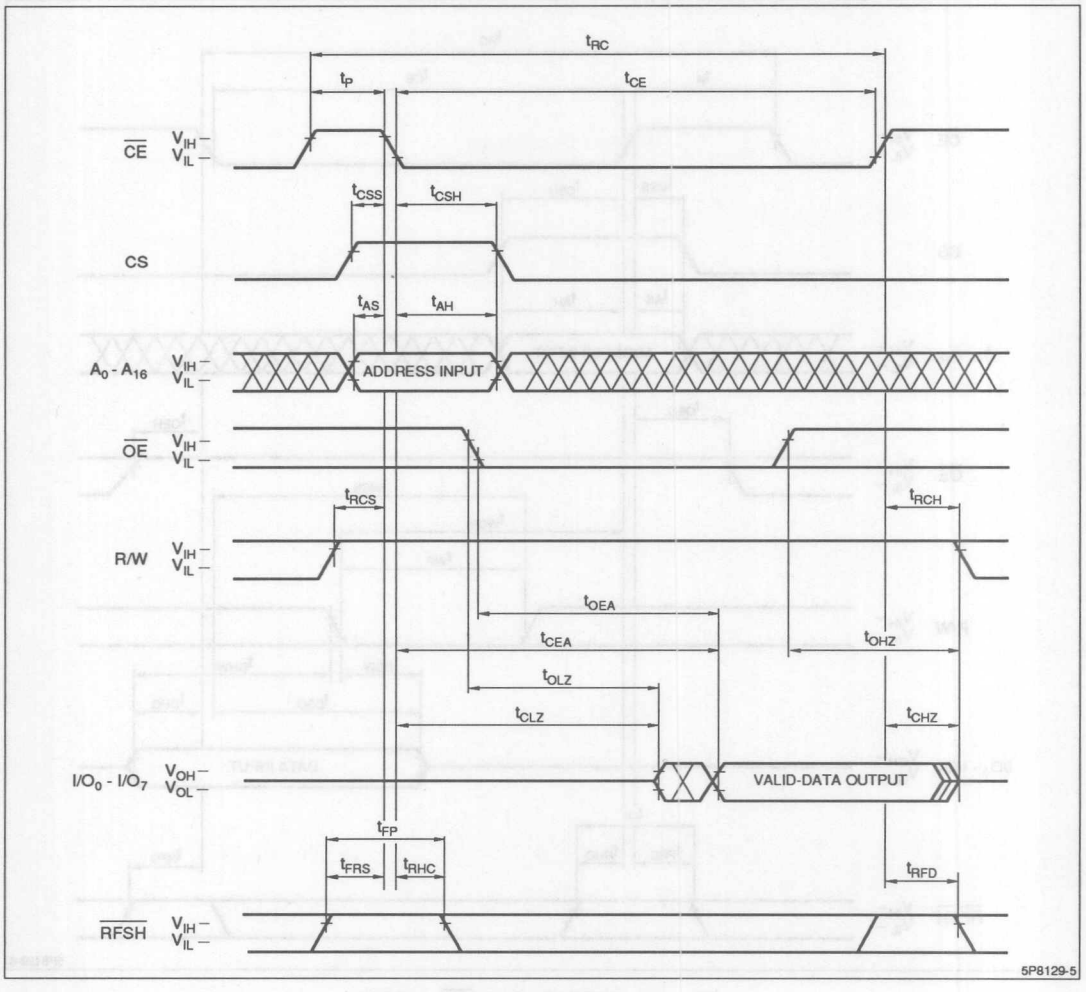


Figure 4. Read Cycle

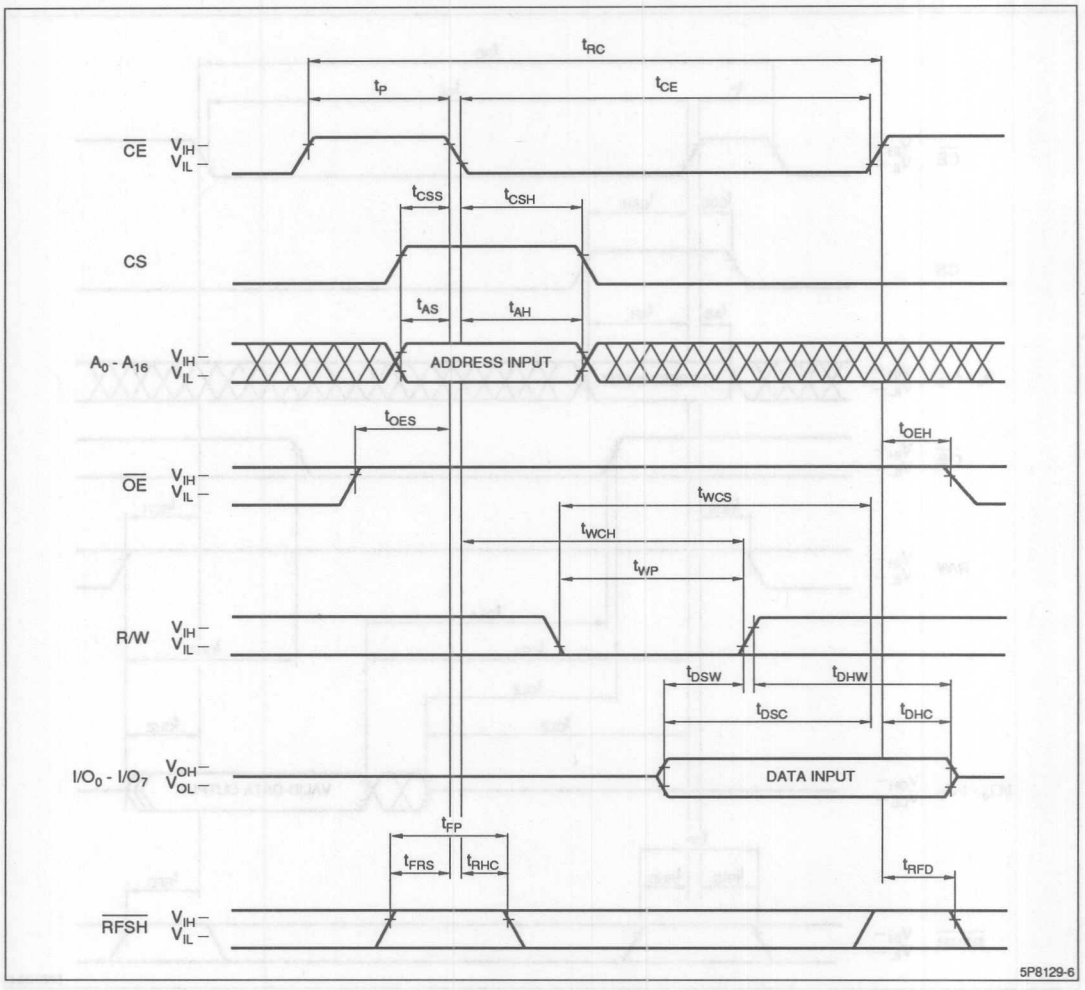


Figure 5. Write Cycle 1 ($\overline{OE}$ = HIGH)

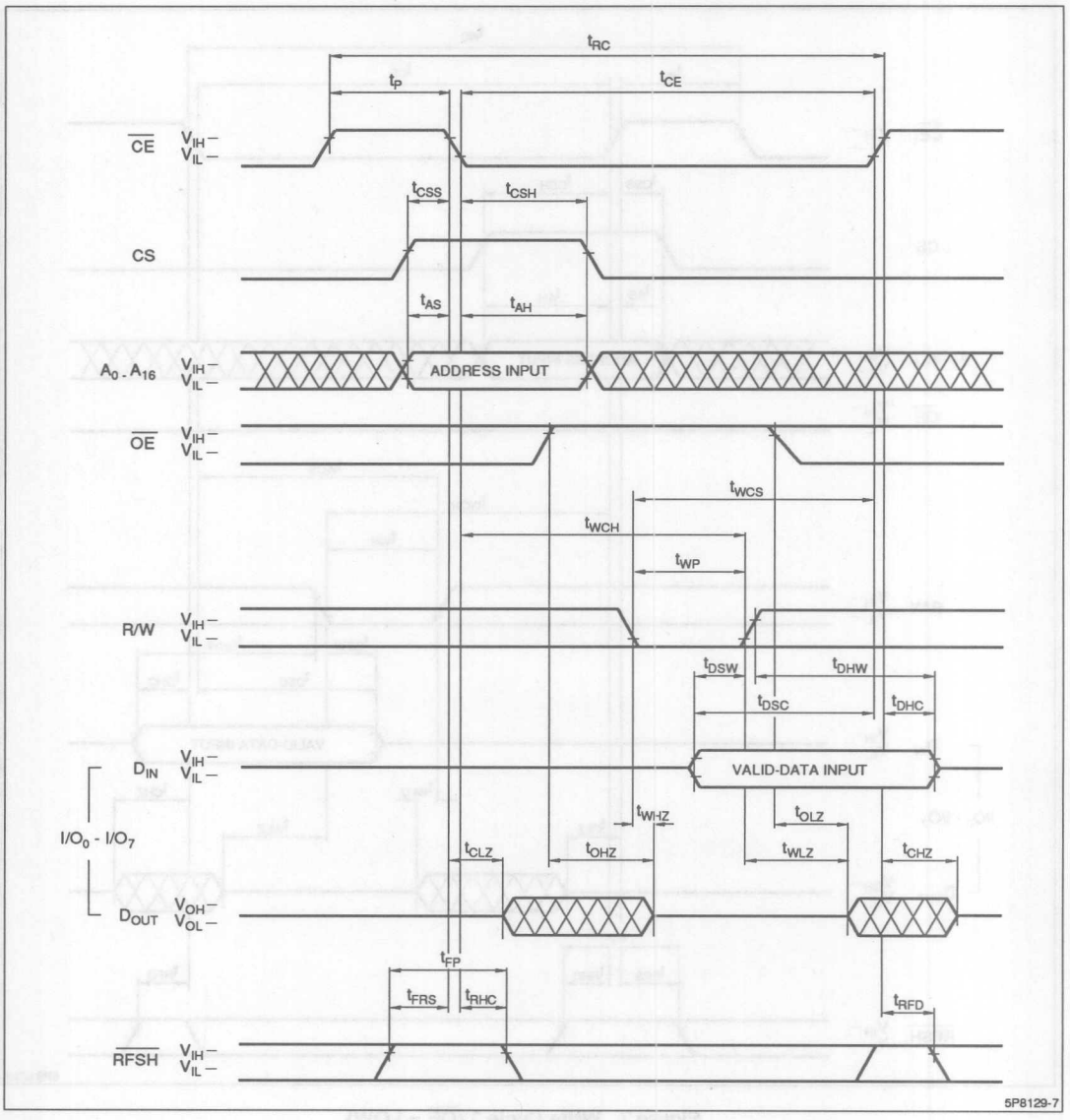


Figure 6. Write Cycle 2 ($\overline{OE}$ Clock)

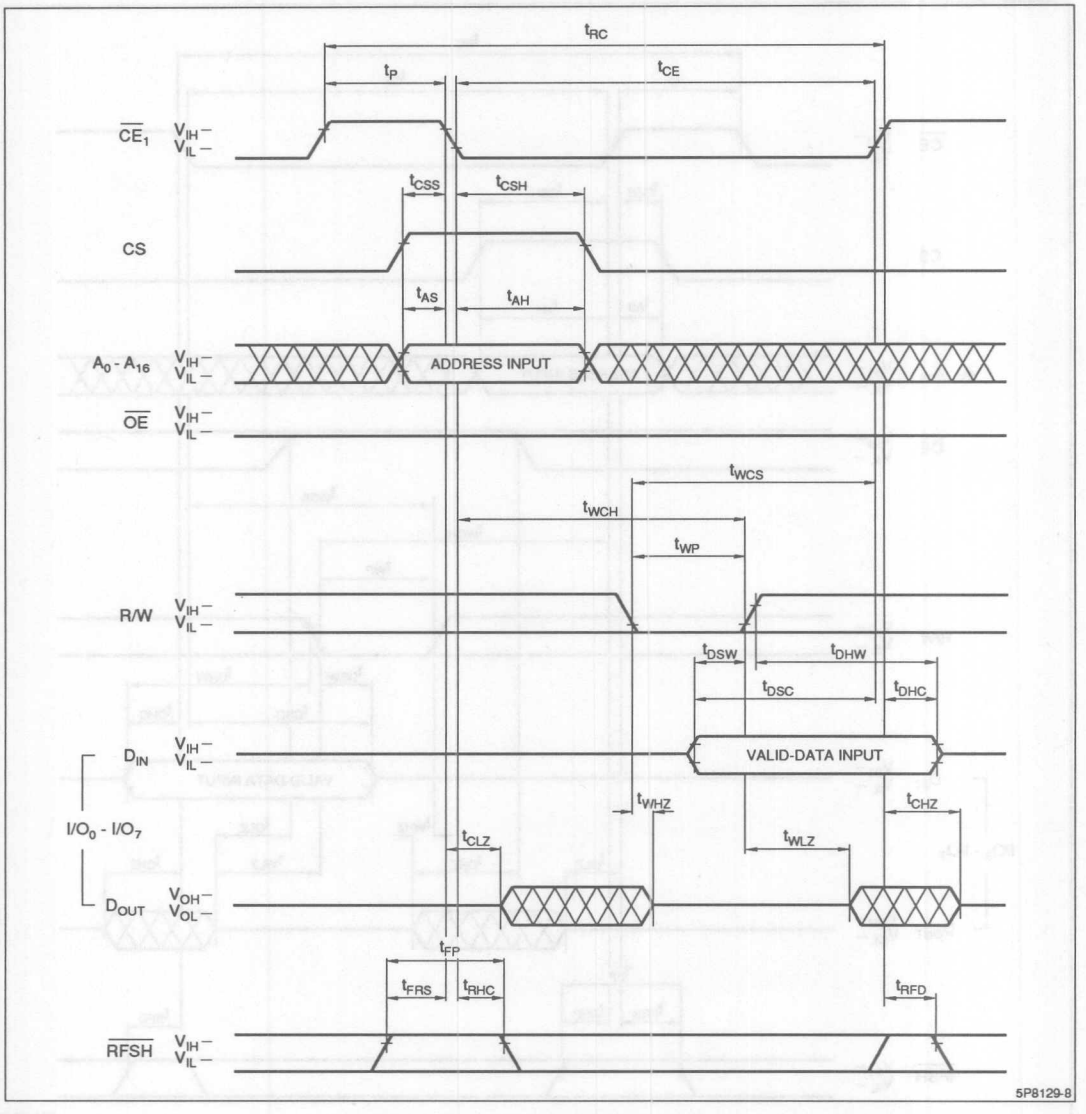


Figure 7. Write Cycle 3 ($\overline{OE}$ = LOW)

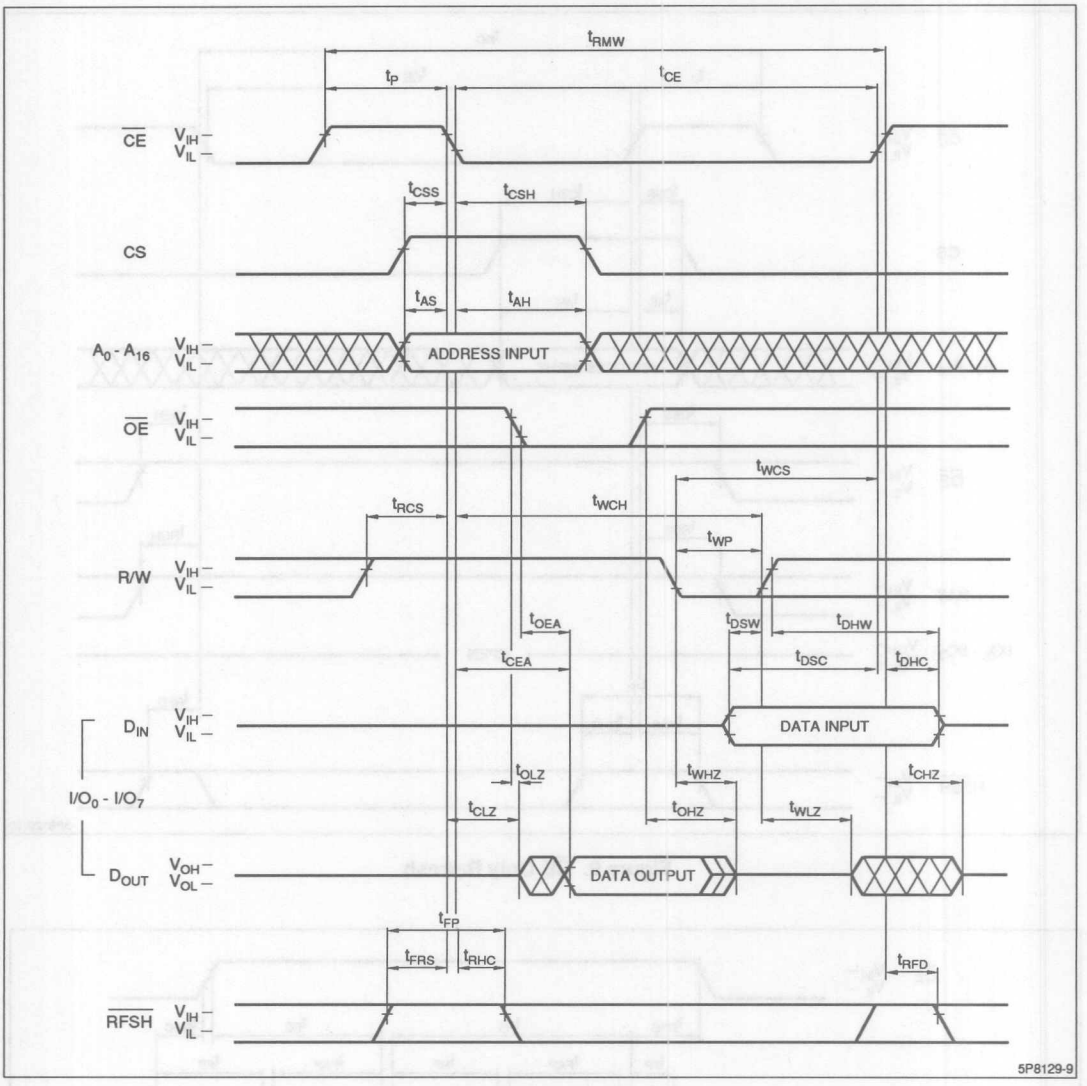


Figure 8. Read-Modify-Write Cycle

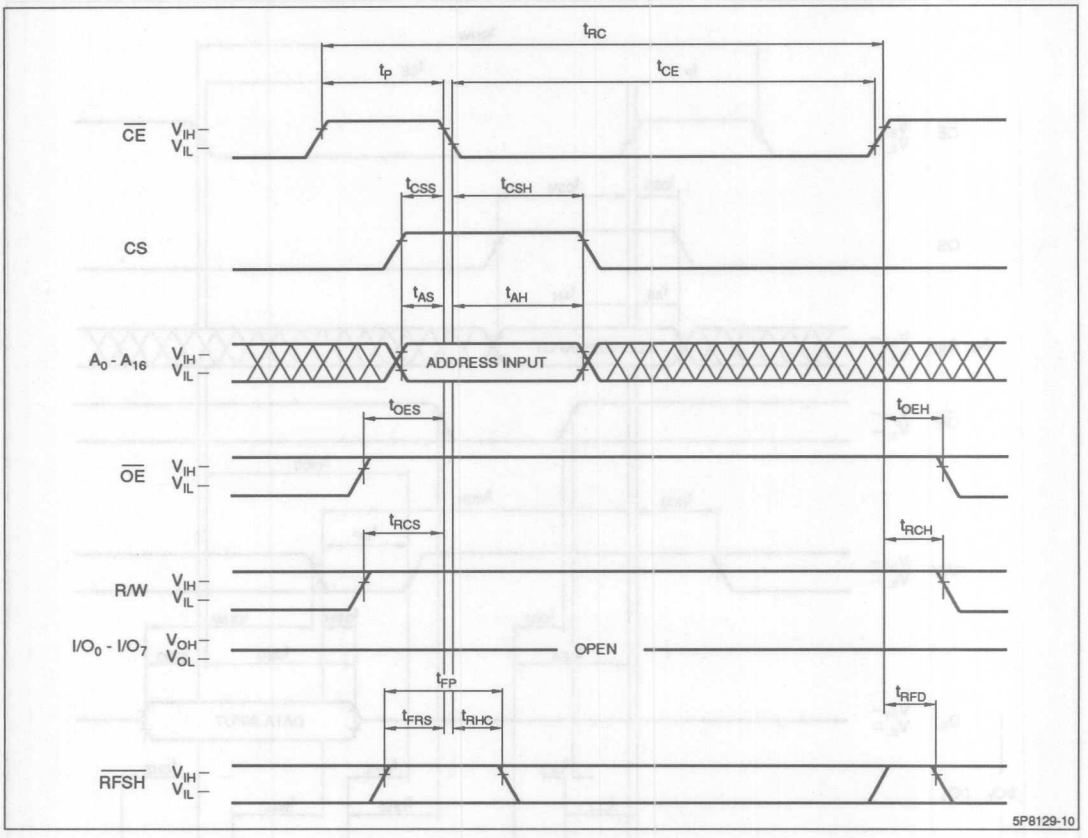


Figure 9. $\overline{CE}$ Only Refresh

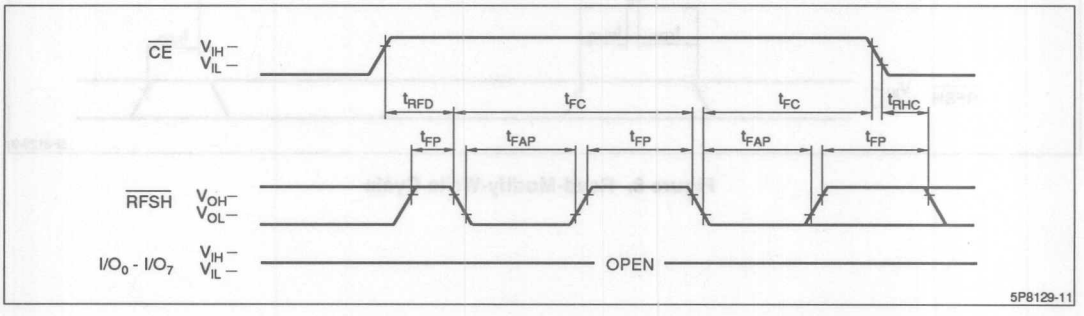


Figure 10. Auto Refresh Cycle

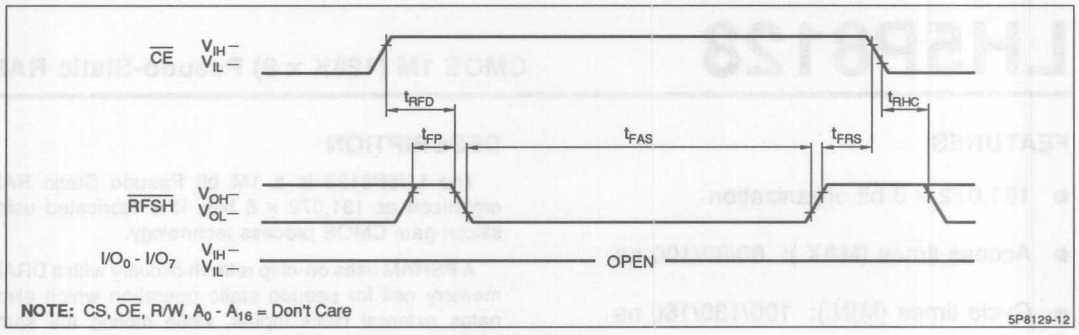


Figure 11. Self Refresh Cycle

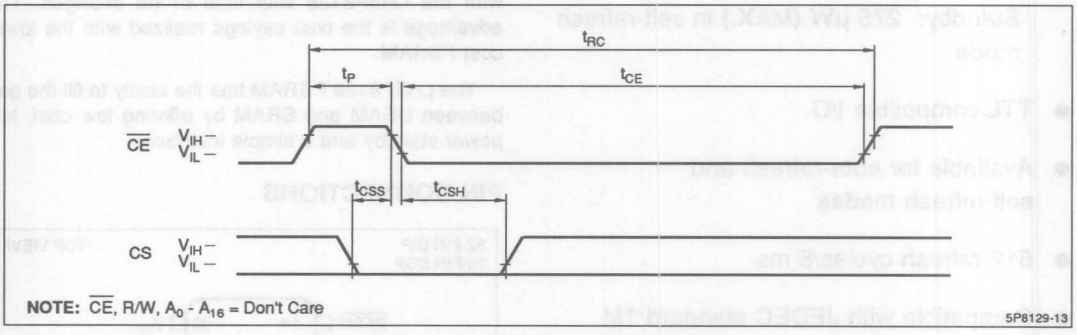


Figure 12. CS Standby Mode

ORDERING INFORMATION

LH5P8129 — Device Type
X — Package
- ## — Speed

Speed:
- 60L 60
- 80L 80 Access Time (ns)
- 10L 100

Package:
- Blank 32-pin, 600-mil DIP (DIP32-P-600)
- N 32-pin, 525-mil SOP (SOP32-P-525)
- T 32-pin, 8 x 20 mm² TSOP(I) (TSOP32-P-0820)
- TR 32-pin, 8 x 20 mm² TSOP(I) Reverse bend (TSOP32-P-0820)

Device Type:
- CMOS 1M (128K x 8) CS Control Pseudo-Static RAM

Example: LH5P8129N-60L (CMOS 1M (128K x 8) Pseudo-Static RAM, 60 ns, 32-pin, 525-mil SOP)

5P8129-14

LH5P8128

CMOS 1M (128K × 8) Pseudo-Static RAM

FEATURES

- 131,072 × 8 bit organization
- Access times (MAX.): 60/80/100 ns
- Cycle times (MIN.): 100/130/160 ns
- Power consumption:
  Operating: 572/440/358 mW (MAX.)
  Standby: 275 µW (MAX.) in self-refresh mode
- TTL compatible I/O
- Available for auto-refresh and self-refresh modes
- 512 refresh cycles/8 ms
- Compatible with JEDEC standard 1M SRAM pinout
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type I)
  (normal and reverse bend pins)

DESCRIPTION

The LH5P8128 is a 1M bit Pseudo Static RAM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

A PSRAM uses on-chip refresh circuitry with a DRAM memory cell for pseudo static operation which eliminates external clock inputs, while having the same pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, existing 128K × 8 SRAM sockets can be filled with the LH5P8128 with little or no changes. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P8128 PSRAM has the ability to fill the gap between DRAM and SRAM by offering low cost, low power standby and a simple interface.

PIN CONNECTIONS

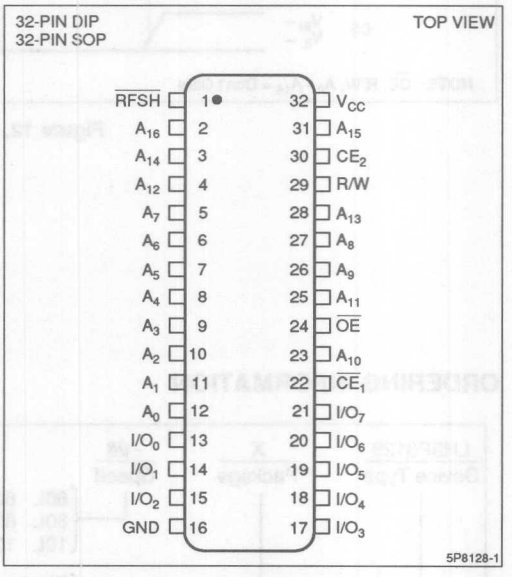


Figure 1. Pin Connections for DIP and SOP Packages

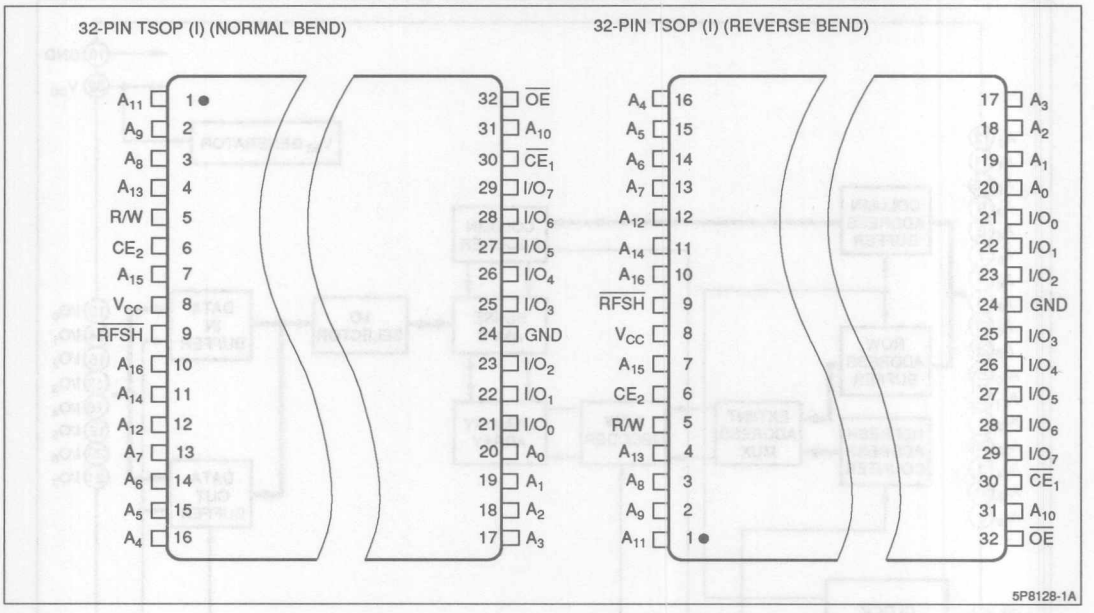


Figure 2. Pin Connections for TSOP Packages

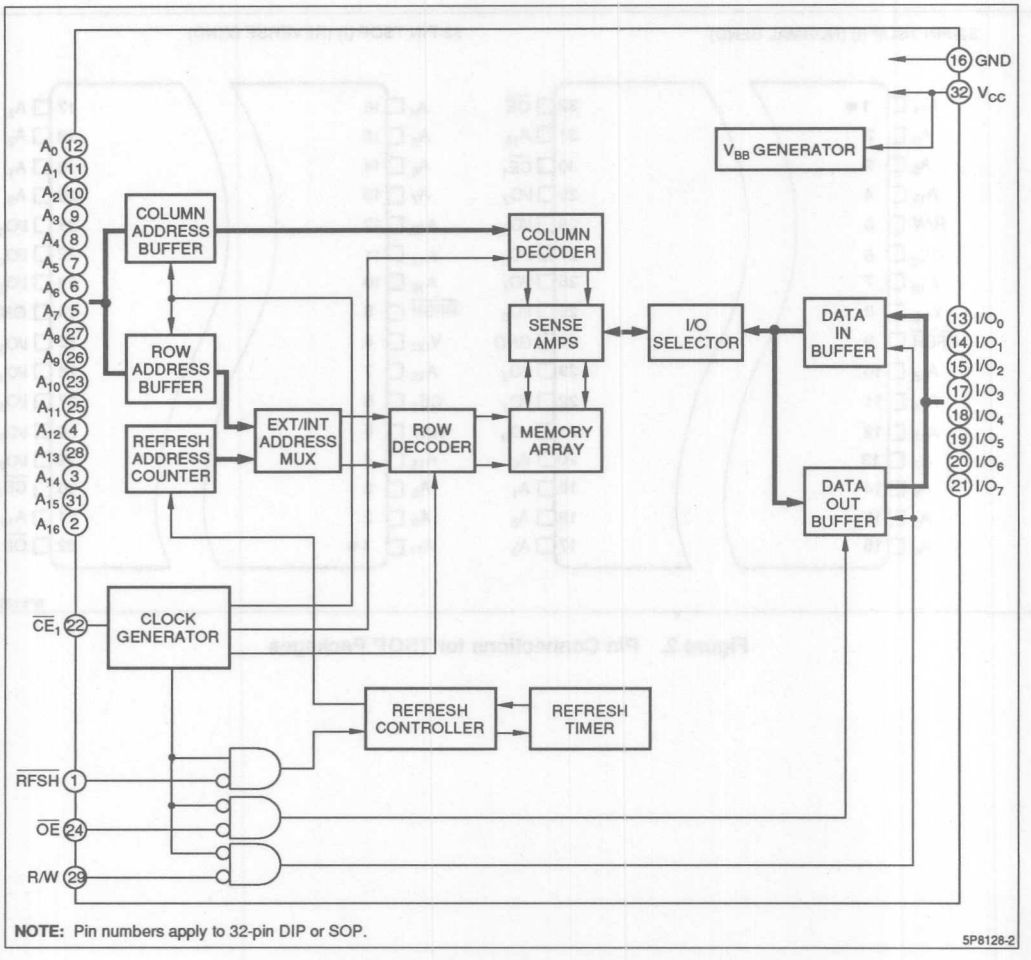


Figure 3. LH5P8128 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
R/W	Read/Write input
$\overline{OE}$	Output Enable Input

SIGNAL	PIN NAME
$\overline{CE_1}$, CE_2	Chip Enable input
$\overline{RFSH}$	Refresh input
I/O_0 - I/O_7	Data input/output

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pins	V_T	-1.0 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	
Output short circuit current	I_O	50	mA	
Power consumption	P_D	600	mW	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		V_{CC} + 0.3	V
	V_{IL}	-1.0		0.8	V

CAPACITANCE (T_A = 0 to +70°C, f = 1MHz, V_{CC} = 5.0 V ± 10%)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT
Input capacitance	A_0 - A_{16}	C_{IN1}		8	pF
	R/W, $\overline{OE}$	C_{IN2}		5	pF
	$\overline{CE_1}$, CE_2	C_{IN3}		5	pF
	$\overline{RFSH}$	C_{IN4}		5	pF
Input/output capacitance	I/O_0 - I/O_7	C_{OUT1}		10	pF

DC CHARACTERISTICS (T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

PARAMETER		SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Operating current	LH5P8128-60	I_{CC1}	tRC = t_{RC} (MIN)		104	mA	1, 2
	LH5P8128-80				80		
	LH5P8128-10				65		
Standby current	TTL Input	I_{CC2}			1	mA	1, 3
	CMOS Input				0.05		1, 4
Self-refresh average current	TTL Input	I_{CC3}			1	mA	1, 5
	CMOS Input				0.05		1, 6
CPU internal cycle average current	LH5P8128-60	I_{CC4}	(R/W = $\overline{OE}$ = V_{IH})		104	mA	1, 2
	LH5P8128-80				80		
	LH5P8128-10				65		
Input leakage current		I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V 0 V on all other test pins	-10	10	µA	
I/O leakage current		I_{LO}	0 V ≤ V_{OUT} ≤ V_{CC} + 0.3 V Output in high-impedance state	-10	10	µA	
Output HIGH voltage		V_{OH}	I_{OUT} = 1 mA	2.4		V	
Output LOW voltage		V_{OL}	I_{OUT} = 4 mA		0.4	V	

NOTES:

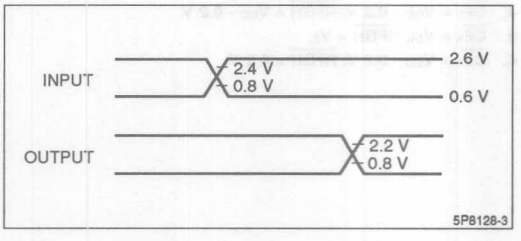
1. The output pins are in high-impedance state
2. I_{CC1} and I_{CC4} depend on the cycle time
3. $\overline{CE_1}$ = V_{IH}, $\overline{RFSH}$ = V_{IH}
4. $\overline{CE_1}$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = V_{CC} - 0.2 V
5. $\overline{CE_1}$ = V_{IH}, $\overline{RFSH}$ = V_{IL}
6. $\overline{CE_1}$ = V_{CC} - 0.2 V, $\overline{RFSH}$ = 0.2 V

AC ELECTRICAL CHARACTERISTICS [1,2,3] (T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

PARAMETER	SYMBOL	LH5P8128-60		LH5P8128-80		LH5P8128-10		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Random read, write cycle time	t_{RC}	100		130		160		ns	
Read modify write cycle time	t_{RMW}	155		195		235		ns	
$\overline{CE}$ pulse width	t_{CE}	60	10,000	80	10,000	100	10,000	ns	
$\overline{CE}$ precharge time	t_P	30		40		50		ns	
Address setup time	t_{AS}	0		0		0		ns	4
Address hold time	t_{AH}	15		20		25		ns	4
Read command setup time	t_{RCS}	0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		ns	
$\overline{CE}$ access time	t_{CEA}		60		80		100	ns	5
$\overline{OE}$ access time	t_{OEA}		25		30		35	ns	5
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20		20		20		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		0		0		ns	
Output enable from end of write	t_{WLZ}	0		0		0		ns	
Chip disable to output in High-Z	t_{CHZ}		20		25		30	ns	
Output disable to output in High-Z	t_{OHZ}		20		25		30	ns	
Write enable to output in High-Z	t_{WHZ}		20		25		30	ns	
$\overline{OE}$ setup time	t_{OES}	0		0		0		ns	
$\overline{OE}$ hold time	t_{OEH}	10		10		10		ns	
Write command pulse width	t_{WP}	30		30		30		ns	
Write command setup time	t_{WCS}	30		30		30		ns	
Write command hold time	t_{WCH}	40		50		60		ns	
Data setup time from write	t_{DSW}	25		30		35		ns	6
Data setup time from $\overline{CE}$	t_{DSC}	25		30		35		ns	6
Data hold time from write	t_{DHW}	0		0		0		ns	6
Data hold time from $\overline{CE}$	t_{DHC}	0		0		0		ns	6
Transition time (rise and fall)	t_T	3	35	3	35	3	35	ns	
Refresh time interval	t_{REF}		8		8		8	ms	
Refresh command hold time	t_{RHC}	15		15		15		ns	
Auto refresh cycle time	t_{FC}	100		130		160		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	30		40		50		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	30	8,000	30	8,000	ns	
Refresh precharge time (Auto refresh)	t_{FP}	30		30		30		ns	
Refresh pulse width (Self refresh)	t_{FAS}	8,000		8,000		8,000		ns	
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	140		160		190		ns	

NOTES:

1. In order to initialize the circuit, $\overline{CE_1}$ should be kept at V_{IH} or CE_2 should be kept at V_{IL} for 100 µs after power-up.
2. AC characteristics are measured at t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right).
4. Address is latched at the negative edge of $\overline{CE_1}$ or at the positive edge of CE_2.
5. Measured with a load equivalent to 2TTL + 100 pF.
6. Data is latched at the positive edge of W/R or at the positive edge of $\overline{CE_1}$ or at the negative edge of CE_2.



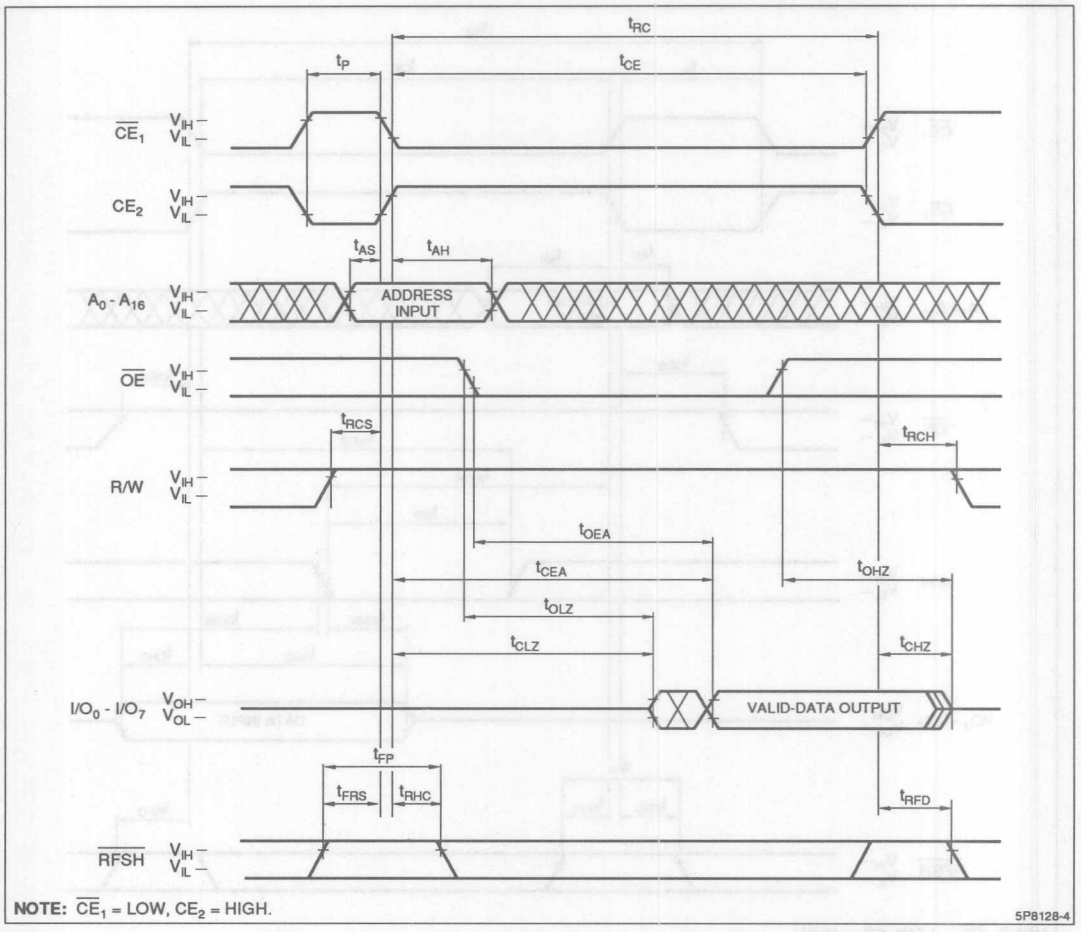
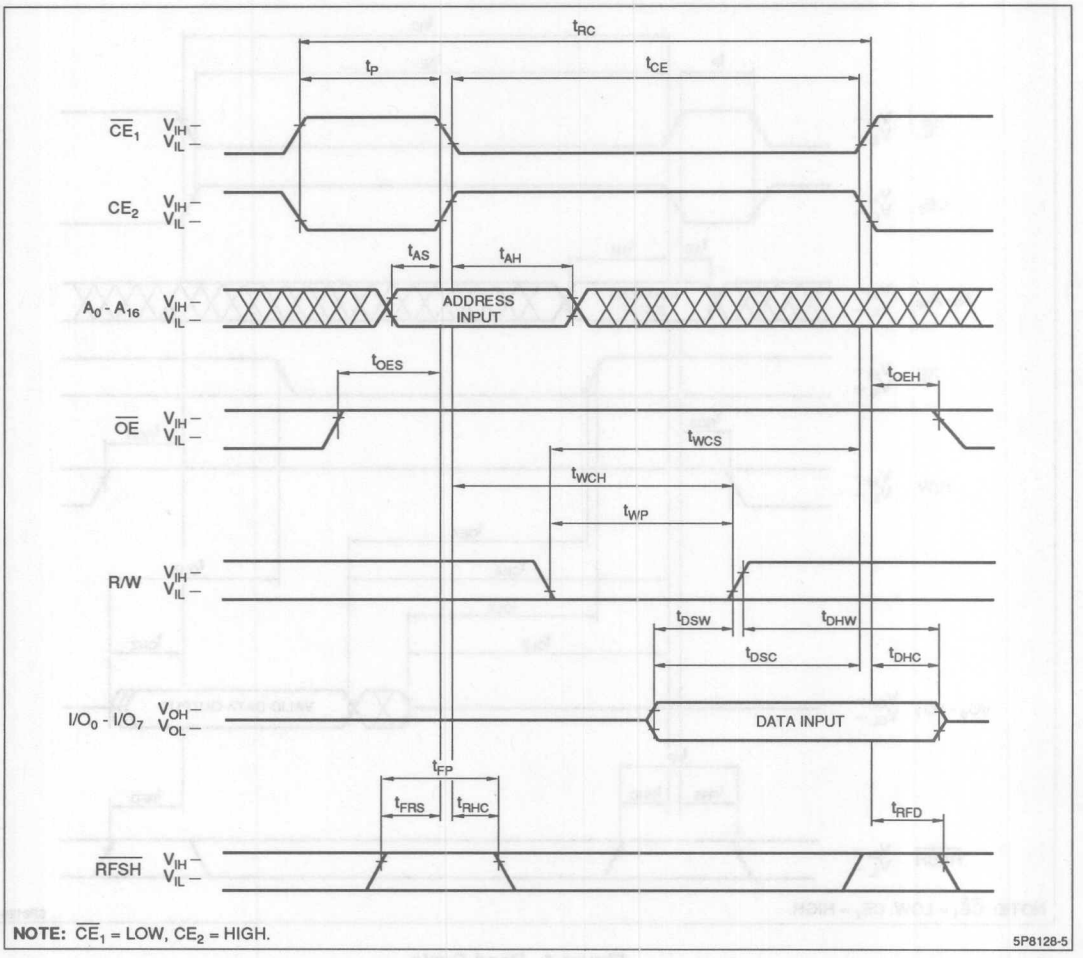


Figure 4. Read Cycle



NOTE: $\overline{CE_1}$ = LOW, CE_2 = HIGH.

5P8128-5

Figure 5. Write Cycle 1 ($\overline{OE}$ = HIGH)

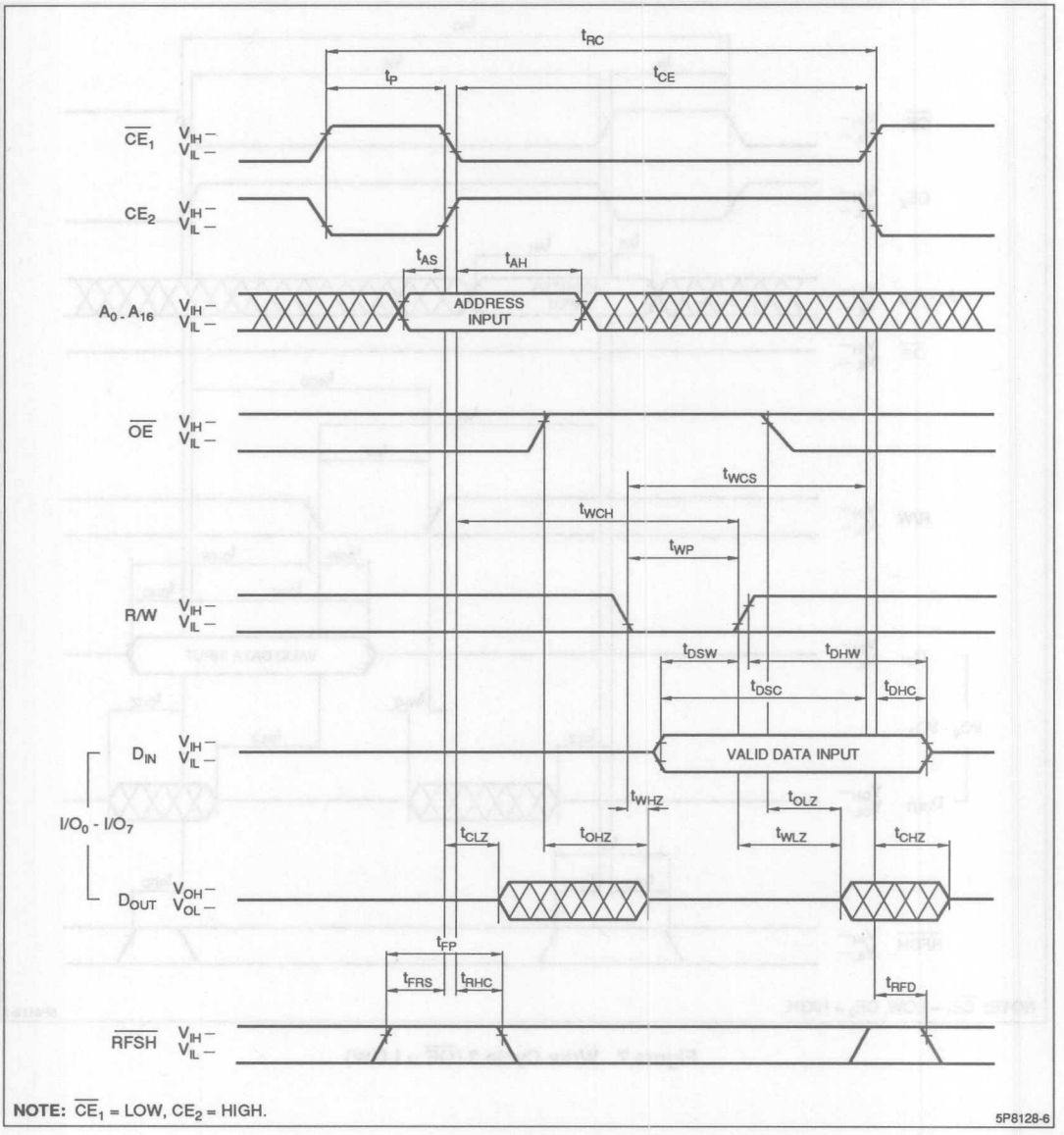


Figure 6. Write Cycle 2 ($\overline{OE}$ Clock)

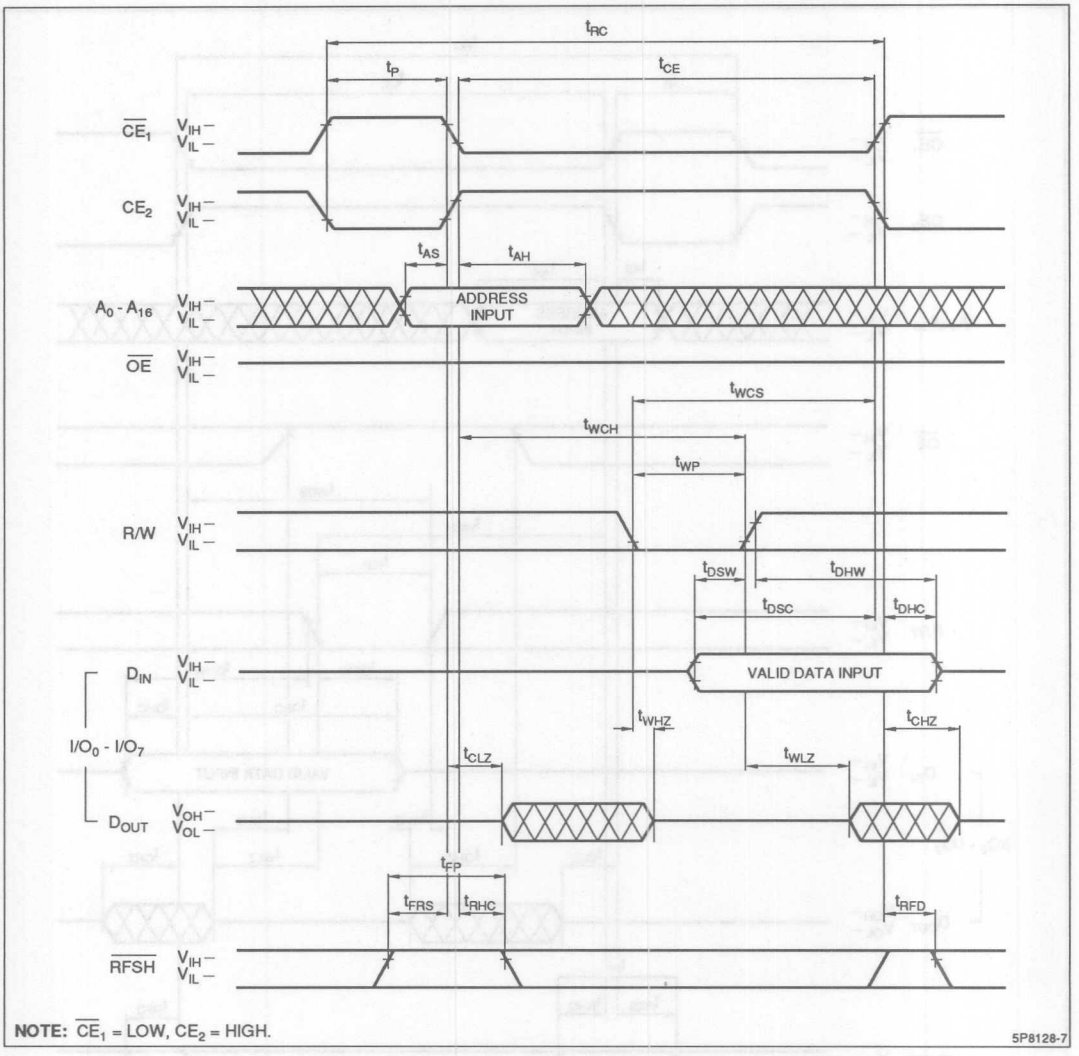


Figure 7. Write Cycle 3 ($\overline{OE}$ = LOW)

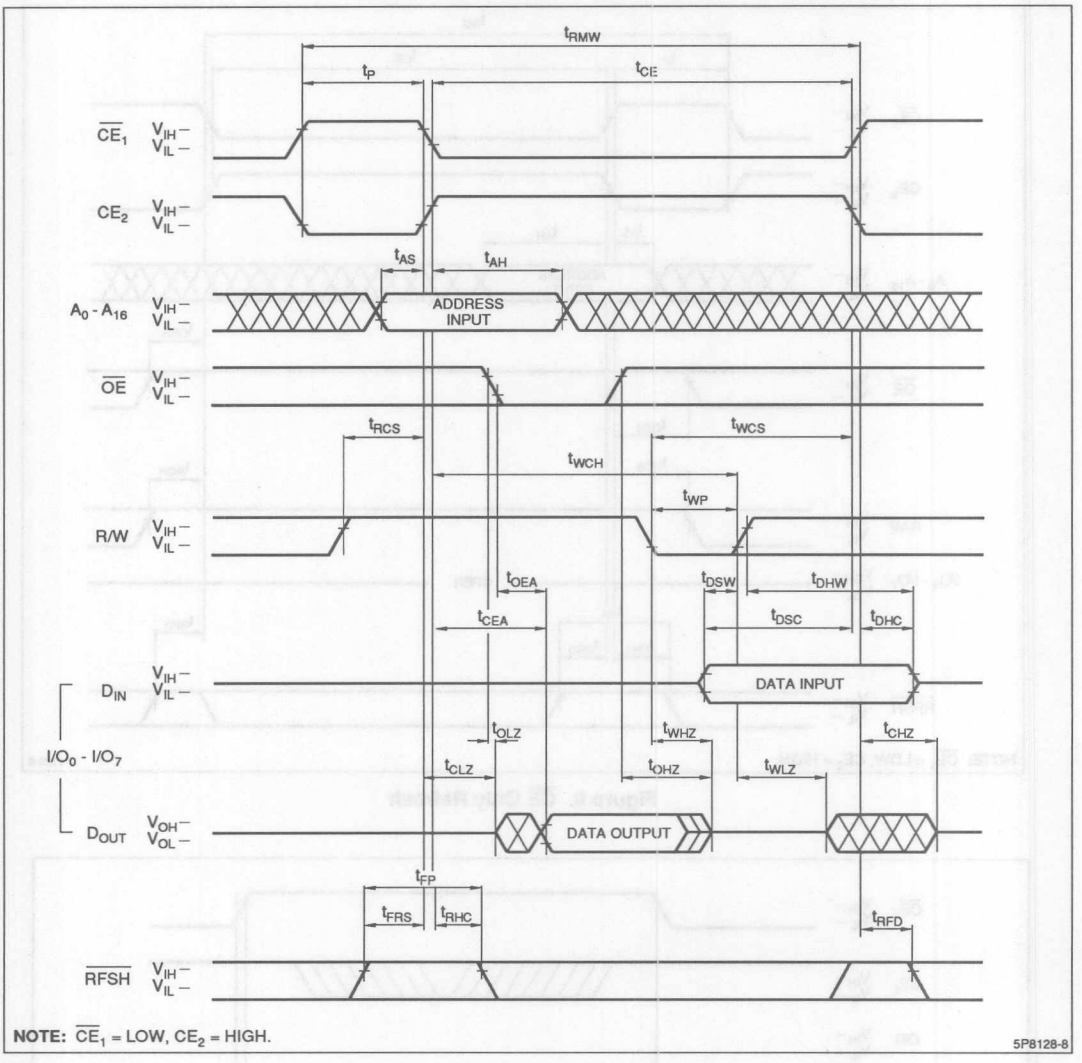


Figure 8. Read-Modify-Write Cycle

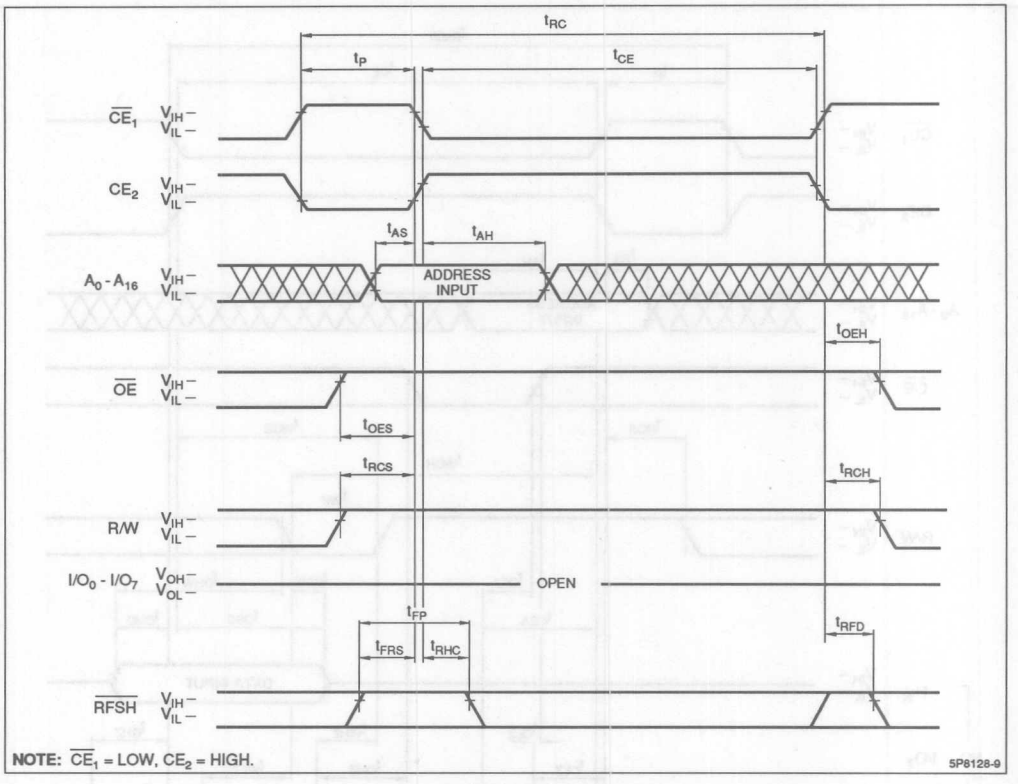


Figure 9. $\overline{CE}$ Only Refresh

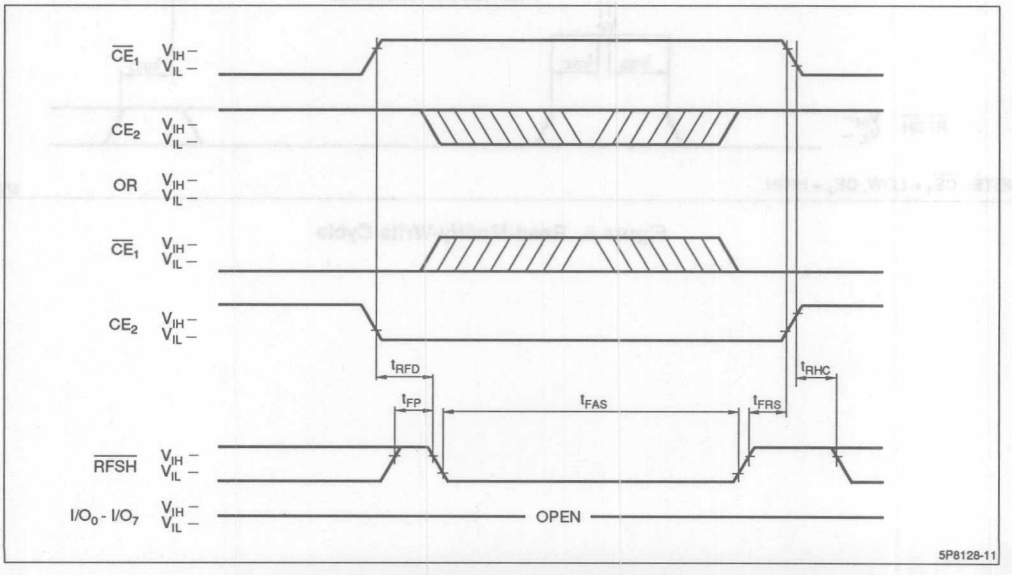


Figure 10. Auto Refresh Cycle

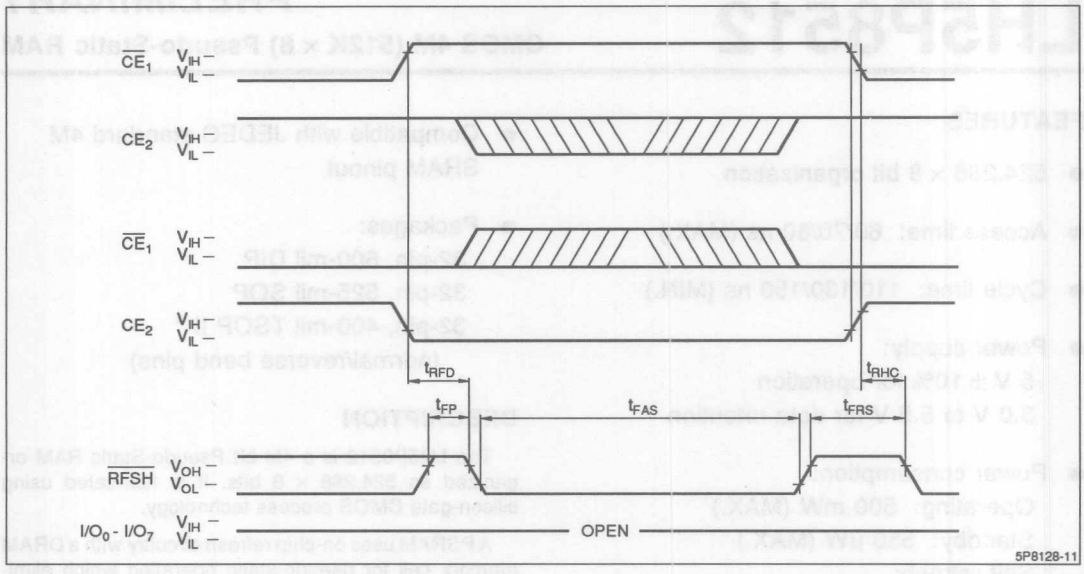
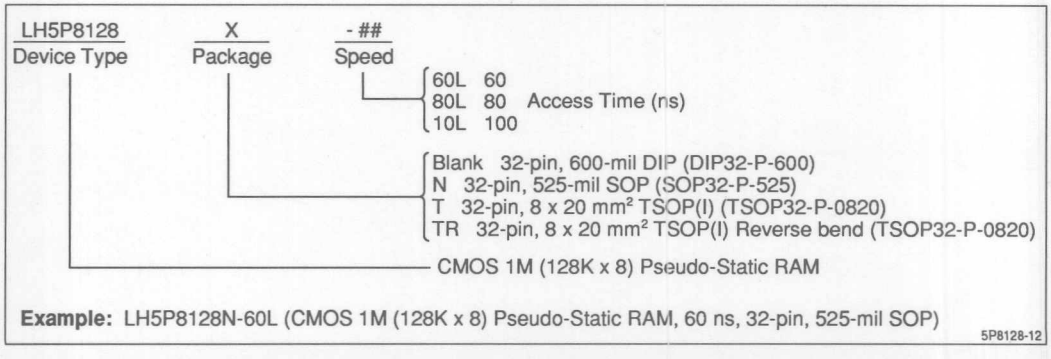


Figure 11. Self Refresh Cycle

ORDERING INFORMATION



LH5P8512

PRELIMINARY

CMOS 4M (512K × 8) Pseudo-Static RAM

FEATURES

- 524,288 × 8 bit organization
- Access time: 60/70/80 ns (MAX.)
- Cycle time: 110/130/150 ns (MIN.)
- Power supply:
  5 V ± 10% for operation
  3.0 V to 5.5 V for data retention
- Power consumption:
  Operating: 500 mW (MAX.)
  Standby: 550 µW (MAX.)
  Self refresh:
  550 µW (MAX.) V_{CC} = 5.5 V
  275 µW (MAX.) V_{CC} = 3.0 V
- TTL compatible I/O
- Available for address refresh, auto-refresh and self-refresh modes
- 2,048 refresh cycles/32 ms
- Non-multiplexed address input
- Read-Modify-Write capability
- Compatible with JEDEC standard 4M SRAM pinout
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 400-mil TSOP II *
  (normal/reverse bend pins)

DESCRIPTION

The LH5P8512 is a 4M bit Pseudo-Static RAM organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

A PSRAM uses on-chip refresh circuitry with a DRAM memory cell for pseudo-static operation which eliminates external clock inputs, while having the same pinout as industry standard SRAMs. Moreover, due to the functional similarities between PSRAMs and SRAMs, existing 512K × 8 SRAM sockets can be filled with the LH5P8512 with little changes. The advantage is the cost savings realized with the lower cost PSRAM.

The LH5P8512 PSRAM can be used for data memory of compact systems such as palm-top terminal equipment, electronic organizers and notebook personal computers, in place of a low power SRAM, or a slow-refresh DRAM, by offering low cost, low power standby, high density and simple interface.

* Consult factory for availability.

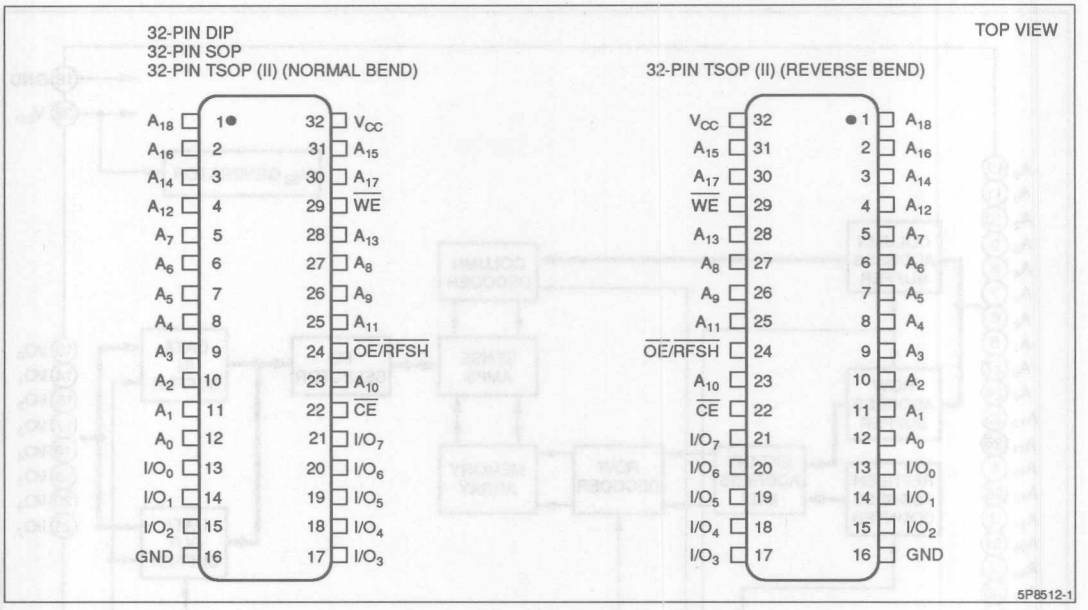


Figure 1. Pin Connections for DIP, SOP and TSOP II Packages

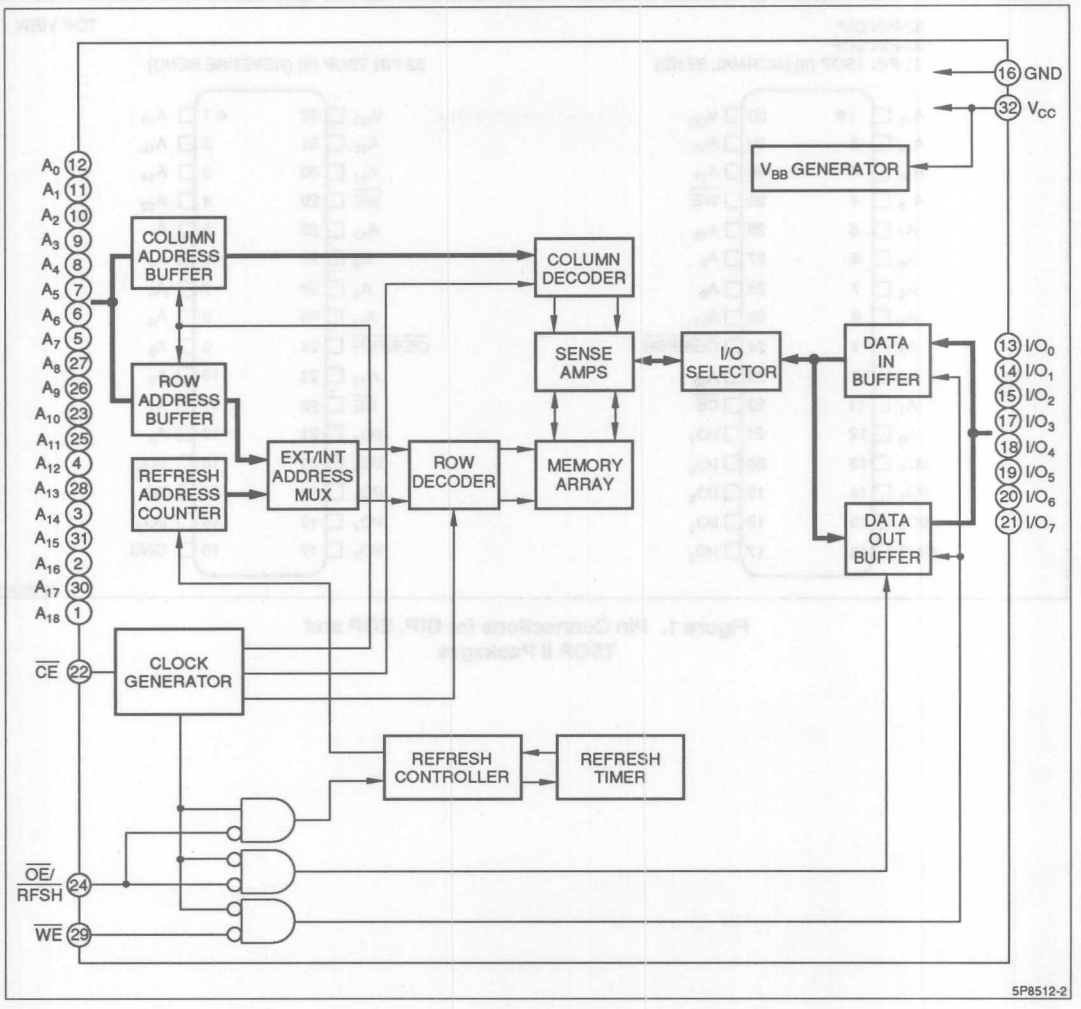


Figure 2. LH5P8512 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{18}	Address input
$\overline{WE}$	Write Enable input
$\overline{OE}/\overline{RFSH}$	Output Enable input/Refresh input

SIGNAL	PIN NAME
$\overline{CE}$	Chip Enable input
I/O_0 - I/O_7	Data input/output

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Applied voltage on any pin	V_T	1.0 to +7.0	V	1
Output short circuit current	I_O	50	mA	
Power consumption	P_D	1	W	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	55 to +150	°C	

NOTE:

1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input voltage	V_{IH}	2.4		6.5	V
	V_{IL}	1.0		0.8	V

DC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	LH5P8512-60L		UNIT	NOTE
			MIN.	MAX.		
Operating current	I_{CC1}	tRC = t_{RC} (MIN.)		100	mA	1,2
Standby current	I_{CC2}	$\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{IH} (MIN.)		1.0	mA	1,2
		$\overline{CE}$ = $\overline{OE}$/$\overline{RFSH}$ = V_{CC} - 0.2 V		100	µA	1
Address refresh average current	I_{CC3}	VIH (MIN.)/V_{IL} (MAX.) on all inputs, t_{RC} = 15.625 µs		1.5	mA	1
		V_{CC} - 0.2 V/0.2 V on all inputs, t_{RC} = 15.625 µs		600	µA	1,2
Auto refresh average current	I_{CC4}	VIH (MIN.)/V_{IL} (MAX.) on all inputs, t_{FC} = 15.625 µs		1.5	mA	1,2
		V_{CC} - 0.2 V/0.2 V on all inputs, t_{FC} = 15.625 µs		600	µA	1,2
Self refresh average current	I_{CC5}	$\overline{CE}$ = V_{IH} (MIN.), $\overline{OE}$/$\overline{RFSH}$ = V_{IL} (MAX.), V_{CC} = 5.5 V		1.0	mA	1,2
		$\overline{CE}$ = V_{CC} - 0.2 V, $\overline{OE}$/$\overline{RFSH}$ = 0.2 V, V_{CC} = 5.5 V		100	µA	1
		$\overline{CE}$ = V_{CC} - 0.2 V, $\overline{OE}$/$\overline{RFSH}$ = 0.2 V, V_{CC} = 3.0 V		50	µA	1
Input leakage current	I_{LI}	0 V ≤ V_{IN} ≤ 6.5 V, 0 V on all other test pins	-10	10	µA	
Output leakage current	I_{LO}	0 V ≤ V_{OUT} ≤ 6.5 V, Outputs in High-Z state	-10	10	µA	
Output HIGH voltage	V_{OH}	I_{OH} = -1.0 mA	2.4		V	
Output LOW voltage	V_{OL}	I_{OL} = 2.1 mA		0.4	V	
Data retention voltage	V_R		3.0	5.5	V	

NOTES:

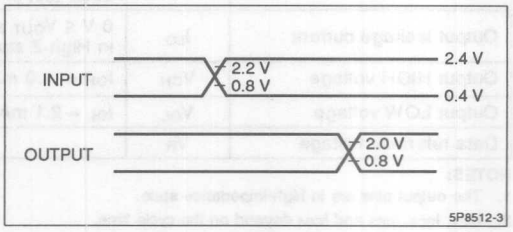
1. The output pins are in high-impedance state.
2. I_{CC1}, I_{CC2}, I_{CC3} and I_{CC4} depend on the cycle time.

AC CHARACTERISTICS [1,2,3,4] (T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10%)

PARAMETER	SYMBOL	LH5P8512-60L		UNIT	NOTE
		MIN.	MAX.		
Random read, write cycle time	t_{RC}	110		ns	
Read modify write cycle time	t_{RMW}	165		ns	
$\overline{CE}$ pulse width	t_{CE}	60	10,000	ns	
$\overline{CE}$ precharge time	t_P	40		ns	
Address setup time	t_{AS}	0		ns	
Address hold time	t_{AH}	15		ns	
Read command setup time	t_{RCS}	0		ns	
Read command hold time	t_{RCH}	0		ns	
$\overline{CE}$ access time	t_{CEA}		60	ns	
$\overline{OE}$ access time	t_{OEA}		30	ns	
$\overline{CE}$ to output in Low-Z	t_{CLZ}	20		ns	
$\overline{OE}$ to output in Low-Z	t_{OLZ}	0		ns	
Chip disable to output in High-Z	t_{CHZ}	0	20	ns	5
Output disable to output in High-Z	t_{OHZ}	0	20	ns	5
Write enable to output in High-Z	t_{WHZ}	0	20	ns	5
$\overline{OE}$ setup time	t_{OES}	0		ns	
$\overline{OE}$ hold time	t_{OEH}	15		ns	
Write command pulse width	t_{WP}	20		ns	
Write command setup time	t_{WCS}	20	10,000	ns	
Write command hold time	t_{WCH}	60	10,000	ns	
Data setup time from write	t_{DSW}	20		ns	
Data setup time from $\overline{CE}$	t_{DSC}	20		ns	
Data hold time from write	t_{DHW}	0		ns	
Data hold time from $\overline{CE}$	t_{DHC}	0		ns	
Transition time (rise and fall)	t_T	3	50	ns	
Refresh time interval	t_{REF}		32	ms	
Auto refresh cycle time	t_{FC}	110		ns	
Refresh delay time from $\overline{CE}$	t_{RFD}	15		ns	
Refresh pulse width (Auto refresh)	t_{FAP}	30	8,000	ns	6
Refresh precharge time (Auto refresh)	t_{FP}	30		ns	6
Refresh pulse width (Self refresh)	t_{FAS}	8,000		ns	6
$\overline{CE}$ delay time from refresh precharge (Self refresh)	t_{FRS}	140		ns	6
V_{CC} recovery time after data retention	t_R	5		ms	

NOTES:

1. In order to initialize the circuit, $\overline{CE}$ should be kept in V_{IH} for 100 µs after power-up.
2. AC characteristics are measured at t_T = 5 ns.
3. AC characteristics are measured at the following condition (see figure at right):
4. Measured with a load equivalent to 1TTL + 100 pF.
5. t_{CHZ}, t_{OHZ}, and t_{WHZ} define the time at which the output achieve the open circuit condition and are not referenced to output voltage levels.
6. Auto refresh and self refresh are defined by $\overline{RFSH}$ pulse width during $\overline{CE}$ = V_{IH}. If $\overline{RFSH}$ pulse width is less than t_{FAP} (MAX.), the cycle is an auto refresh cycle and memory cells are refreshed by the internal counter. If $\overline{RFSH}$ pulse width is more than t_{FAS} (MIN.), the cycle is a self refresh cycle and memory cells are refreshed by the internal clock automatically.



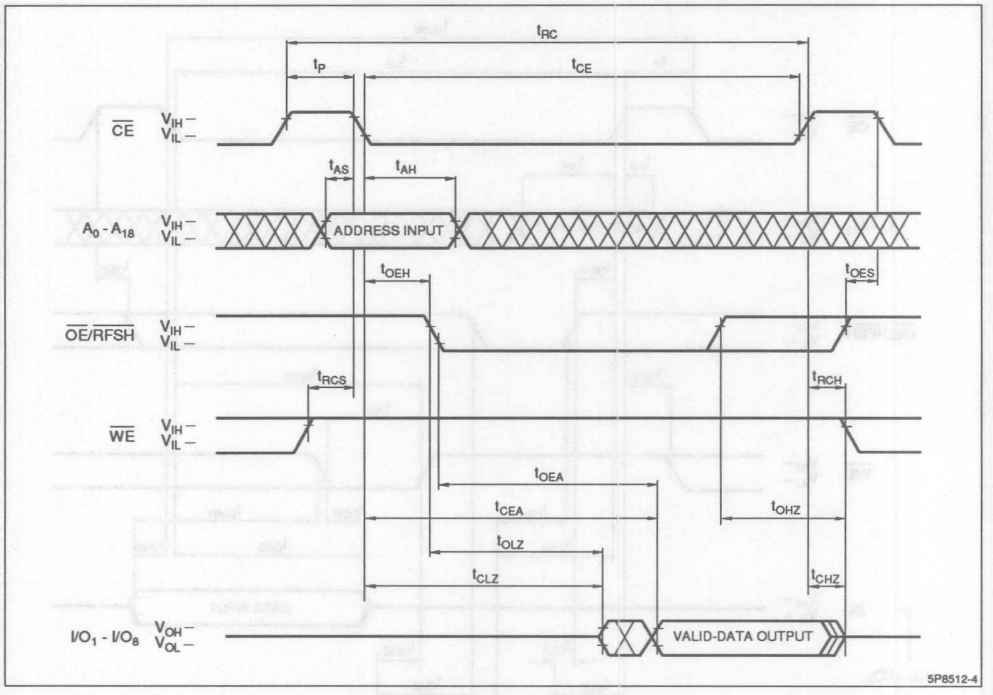


Figure 3. Read Cycle

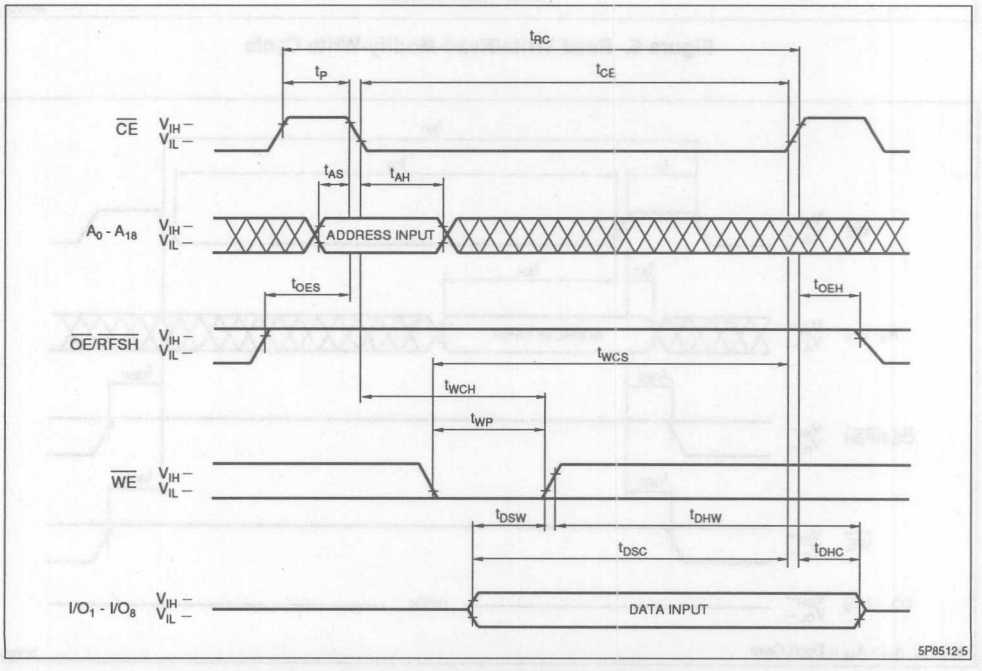


Figure 4. Write Cycle

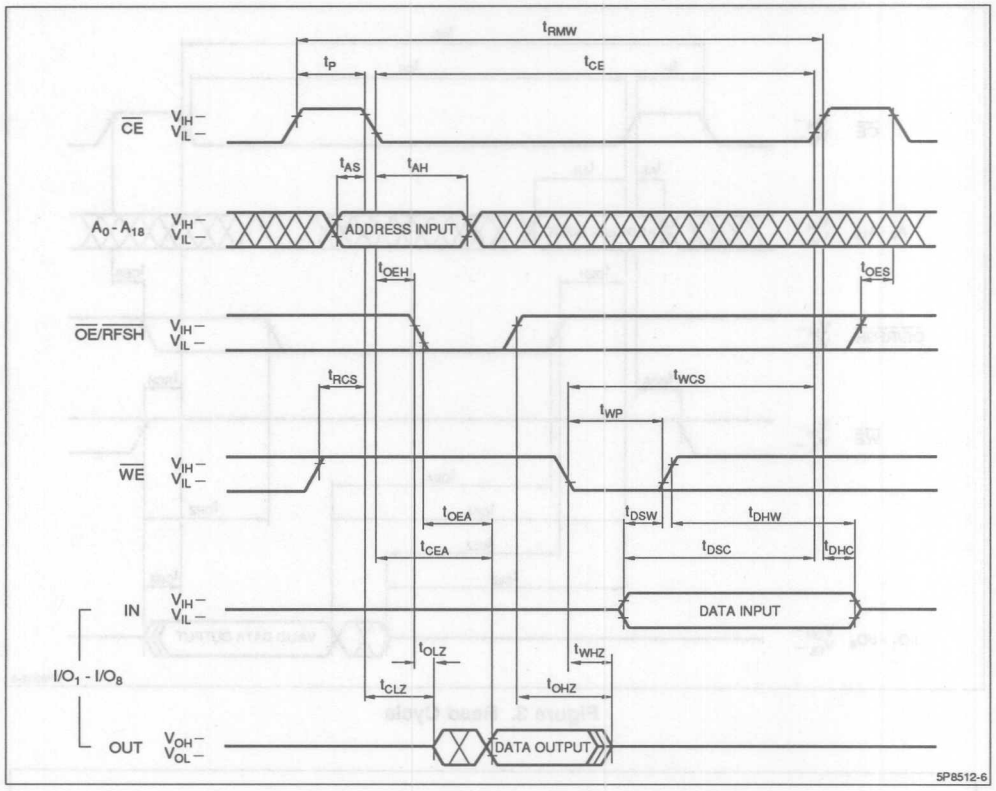


Figure 5. Read Write/Read-Modify-Write Cycle

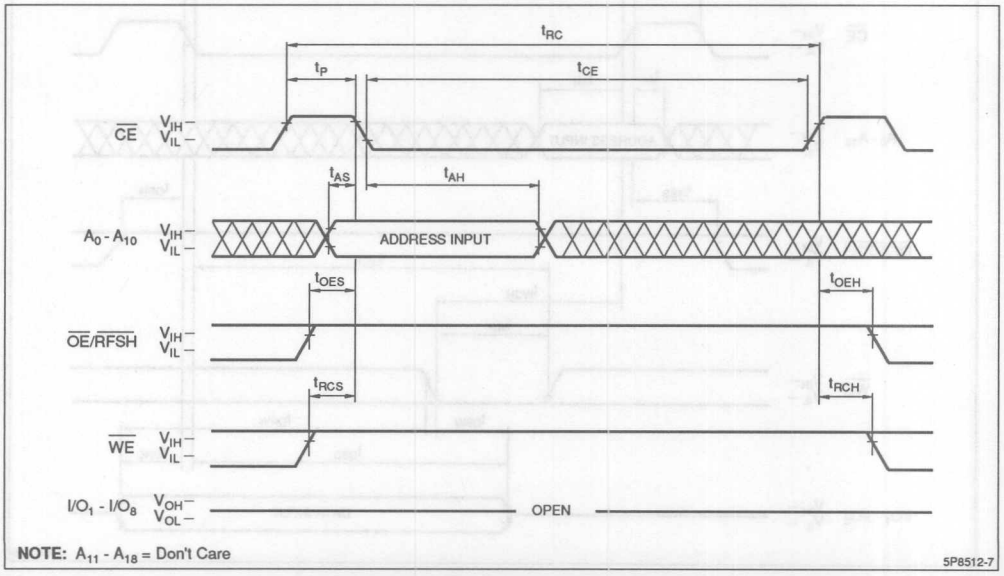


Figure 6. Address Refresh Cycle

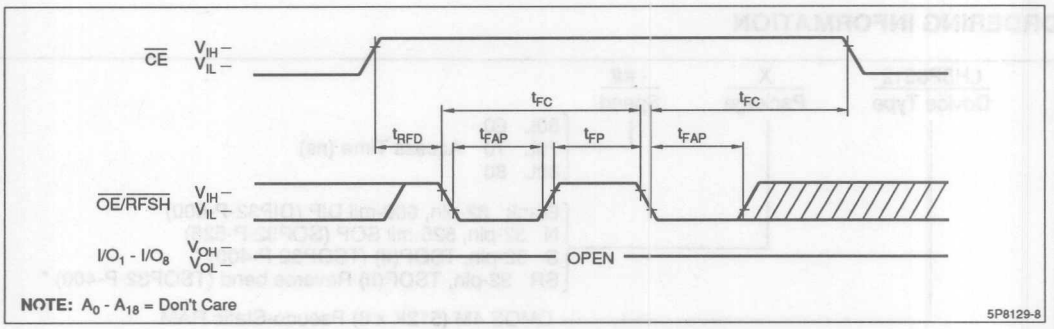


Figure 7. Auto Refresh Cycle

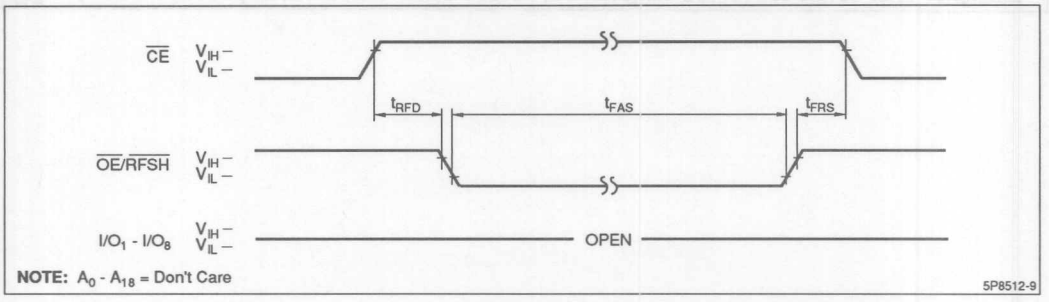


Figure 8. Self Refresh Cycle

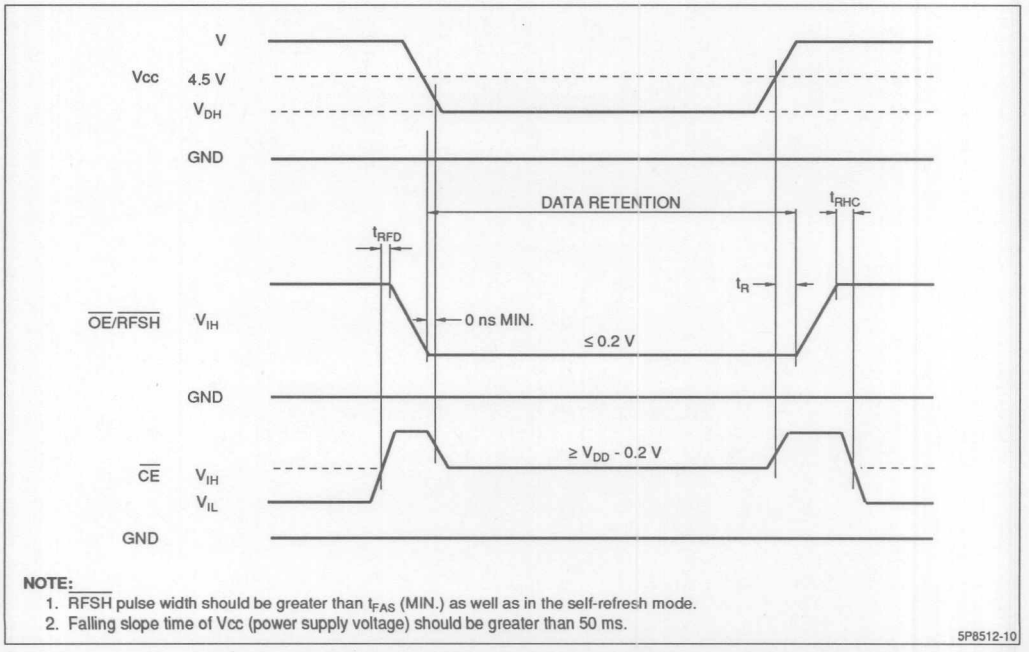
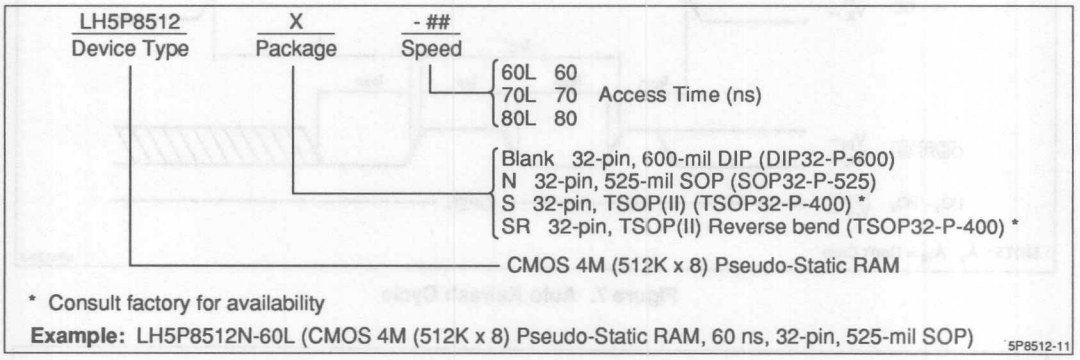


Figure 9. Data Retention Mode

ORDERING INFORMATION



GENERAL INFORMATION – 1

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FIFO MEMORIES – 5

APPLICATION NOTES AND CONFERENCE PAPERS – 6

PACKAGING – 7

STATIC RAMs

	Density	Organization	Page
LH5116/H	16K	2K × 8	3-1
LH5116S	16K	2K × 8	3-9
LH5118/H	16K	2K × 8	3-16
LH5168/H	64K	8K × 8	3-24
LH5168SH	64K	8K × 8	3-33
LH51256L	256K	32K × 8	3-41
LH511000UL	1M	128K × 8	3-48
LH52250AL	256K	32K × 8	3-57
LH52256LL	256K	32K × 8	3-65
LH52252A	256K	64K × 4	3-72
LH52252B	256K	64K × 4	3-79
LH52253	256K	64K × 4	3-86
LH52258	256K	32K × 8	3-93
LH52258A	256K	32K × 8	3-101
LH52258B	256K	32K × 8	3-109
LH521002	1M	256K × 4	3-117
LH521007	1M	128K × 8	3-125
LH521008	1M	128K × 8	3-133
LH521028	1M	64K × 18	3-141

LH5116

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time:
  100 ns (MAX.)
- Power consumption:
  Operating: 220 mW (MAX.)
  Standby: 5.5 µW (MAX.)
- Single +5 V power supply
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available
  LH5116H: -40 to +85°C
- Packages:
  24-pin, 600-mil DIP
  24-pin, 300-mil SK-DIP
  24-pin, 450-mil, SOP
- Compatible with 16K EPROM and mask ROM pinout

DESCRIPTION

The LH5116 is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology. It features high speed access in read mode using output enable (t_{OE}).

PIN CONNECTIONS

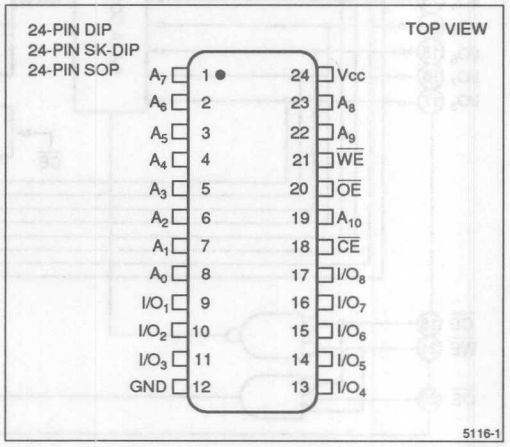


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

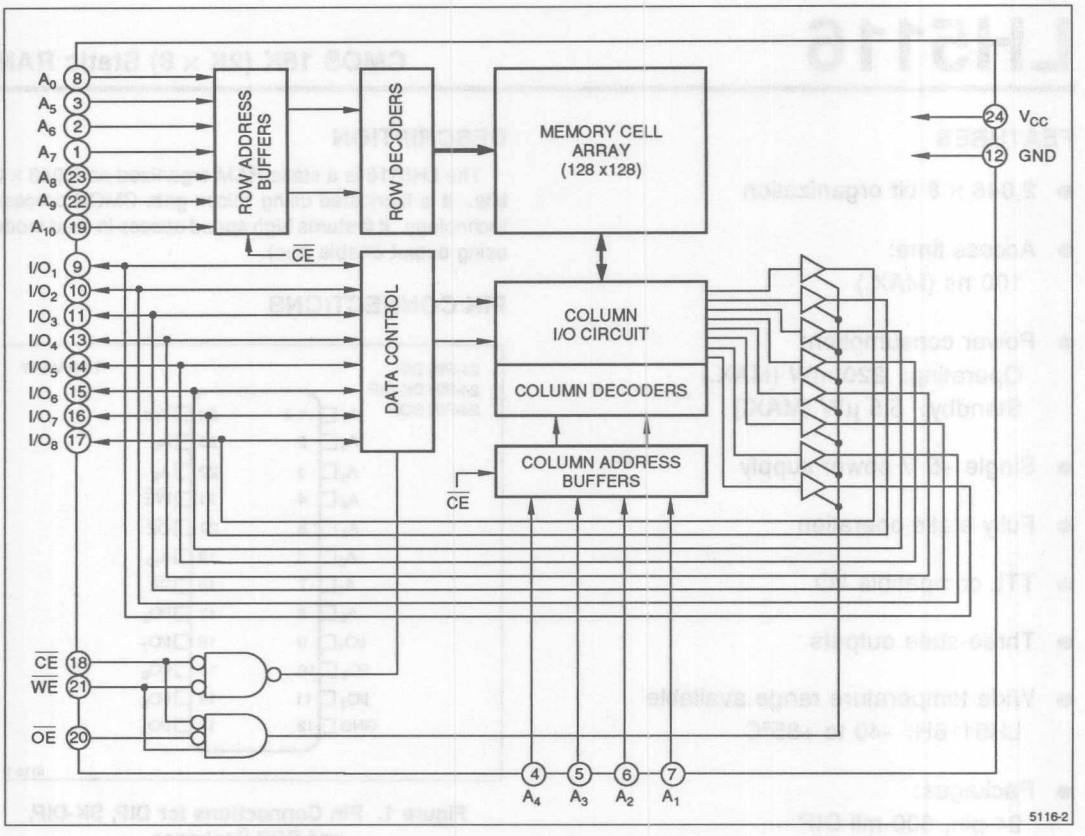


Figure 2. LH5116 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data input/output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
L	X	L	Write	D_{IN}	Operating (I_{CC})	1
L	L	H	Read	D_{OUT}	Operating (I_{CC})	
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	X	Outputs disable	High-Z	Operating (I_{CC})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	0 to +70	°C	2
		-40 to +85		3
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5116/D/NA
3. Applied to the LH5116H/HD/HN

RECOMMENDED OPERATING CONDITIONS [1]

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

NOTE:
1. T_A = 0 to 70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)

DC CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output "LOW" voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
Output "HIGH" voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}			1.0	µA	
Operating current	I_{CC1}	Outputs open ($\overline{OE}$ = V_{CC})		25	30	mA	2
	I_{CC2}	Outputs open ($\overline{OE}$ = V_{IH})		30	40	mA	3
Standby current	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V All other input pins = 0 V to V_{CC}			1.0	µA	
					0.2		4

NOTES:
1. T_A = 0 to 70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)
2. $\overline{CE}$ = 0 V; all other input pins = 0 V to V_{CC}
3. $\overline{CE}$ = V_{IL}; all other input pins = V_{IL} to V_{IH}
4. T_A = 25°C

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
Chip enable access time	t_{ACE}			100	ns	
$\overline{CE}$ Low to output in Low-Z	t_{CLZ}	10			ns	1
Output enable access time	t_{OE}			40	ns	
Output enable Low to output in Low-Z	t_{OLZ}	10			ns	1
Chip disable to output in High-Z	t_{CHZ}	0		40	ns	1
Output disable to output in High-Z	t_{OHZ}	0		40	ns	1
Output hold time	t_{OH}	10			ns	

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

(2) WRITE CYCLE [1] (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100			ns	
Chip enable to end of write	t_{CW}	80			ns	
Address valid time	t_{AW}	80			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	60			ns	
Write recovery time	t_{WR}	10			ns	
Output active from end of write	t_{OW}	10			ns	2
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	2
Data valid to end of write	t_{DW}	30			ns	
Data hold time	t_{DH}	10			ns	
Output enable to output in High-Z	t_{OHZ}			40	ns	2
Output active from end of write	t_{OW}	10			ns	2

NOTE:

1. T_A = 0 to +70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load condition	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCRC}$ - 0.2V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2V, V_{CCDR} = 3.0 V			1.0	µA	
					0.2		2
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	3

NOTES:

1. T_A = 0 to +70°C (LH5116/D/NA), T_A = -40 to +85°C (LH5116H/HD/HN)
2. T_A = 25°C
3. t_{RC} = Read cycle time

CAPACITANCE [1] (f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:

1. This parameter is sampled and not production tested.

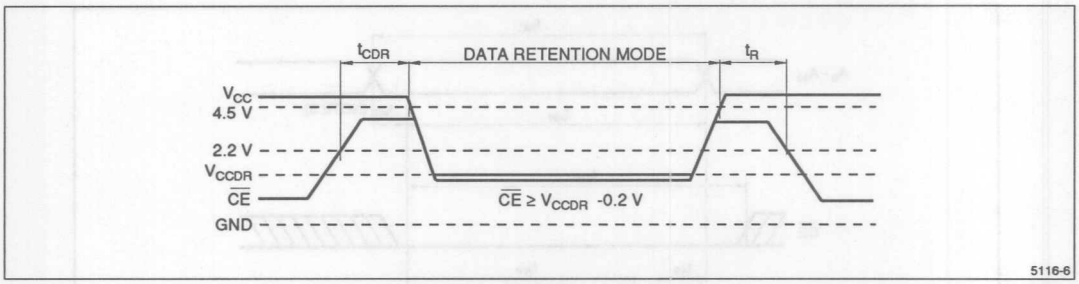


Figure 3. Low Voltage Data Retention

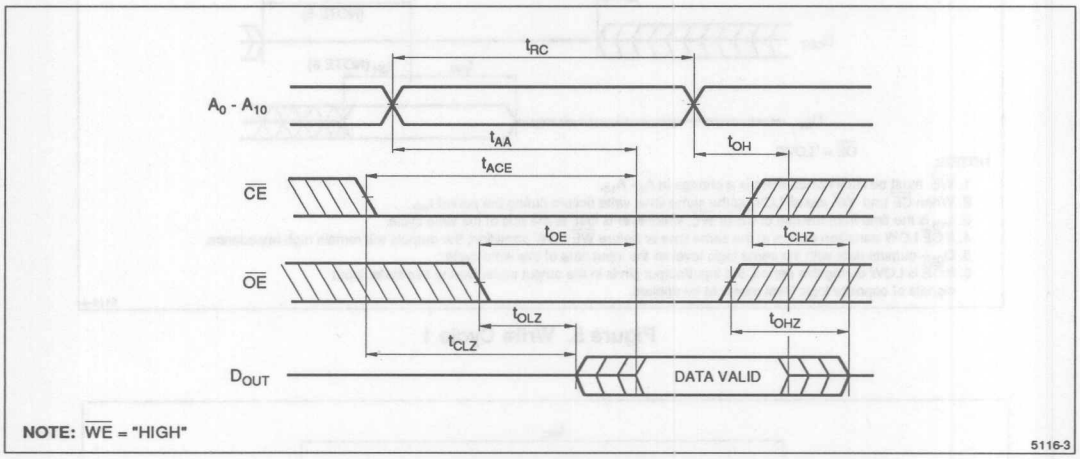
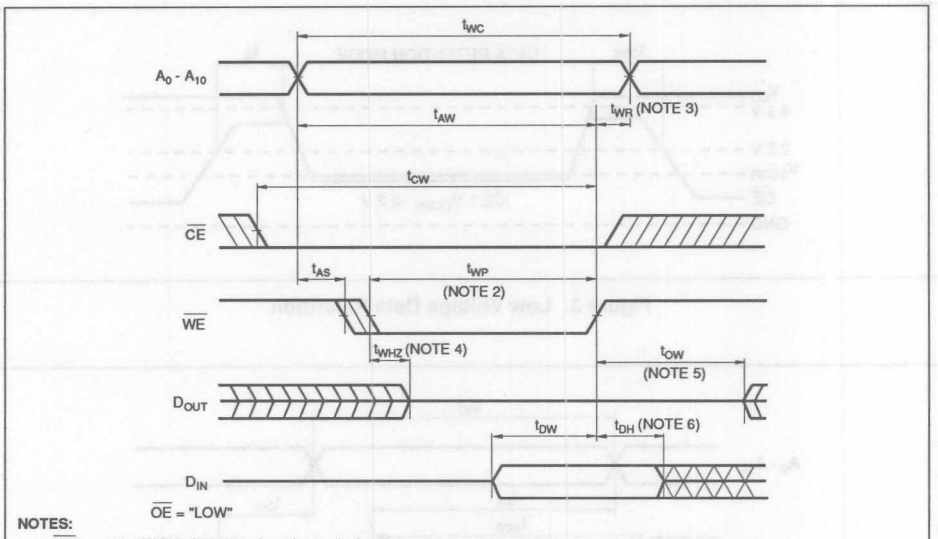


Figure 4. Read Cycle



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are all LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pin is in the output state. During this state, input signals of opposite logic level must not be applied.

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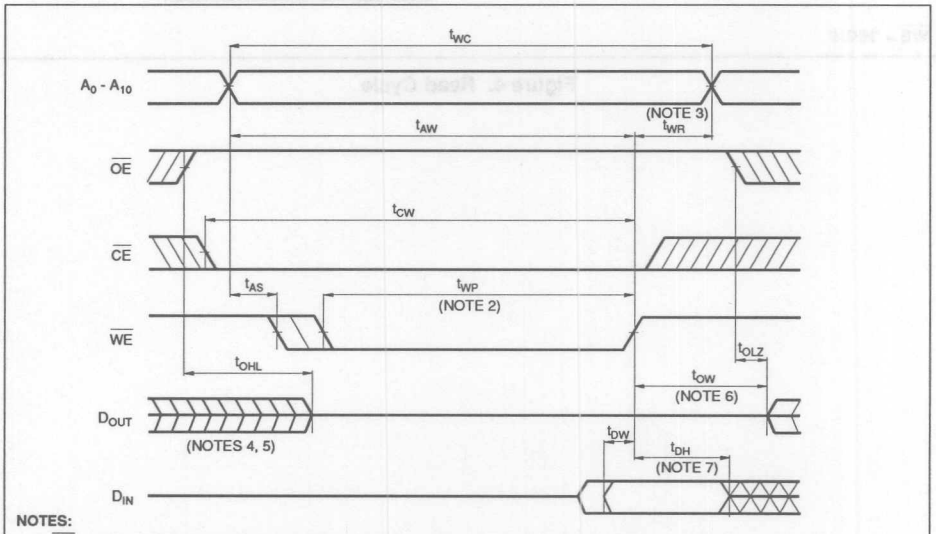
Figure 5. Write Cycle 1



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are all LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the outputs will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pin is in the output state. During this state, input signals of opposite logic level must not be applied.

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Figure 6. Write Cycle 2 (Note 1)

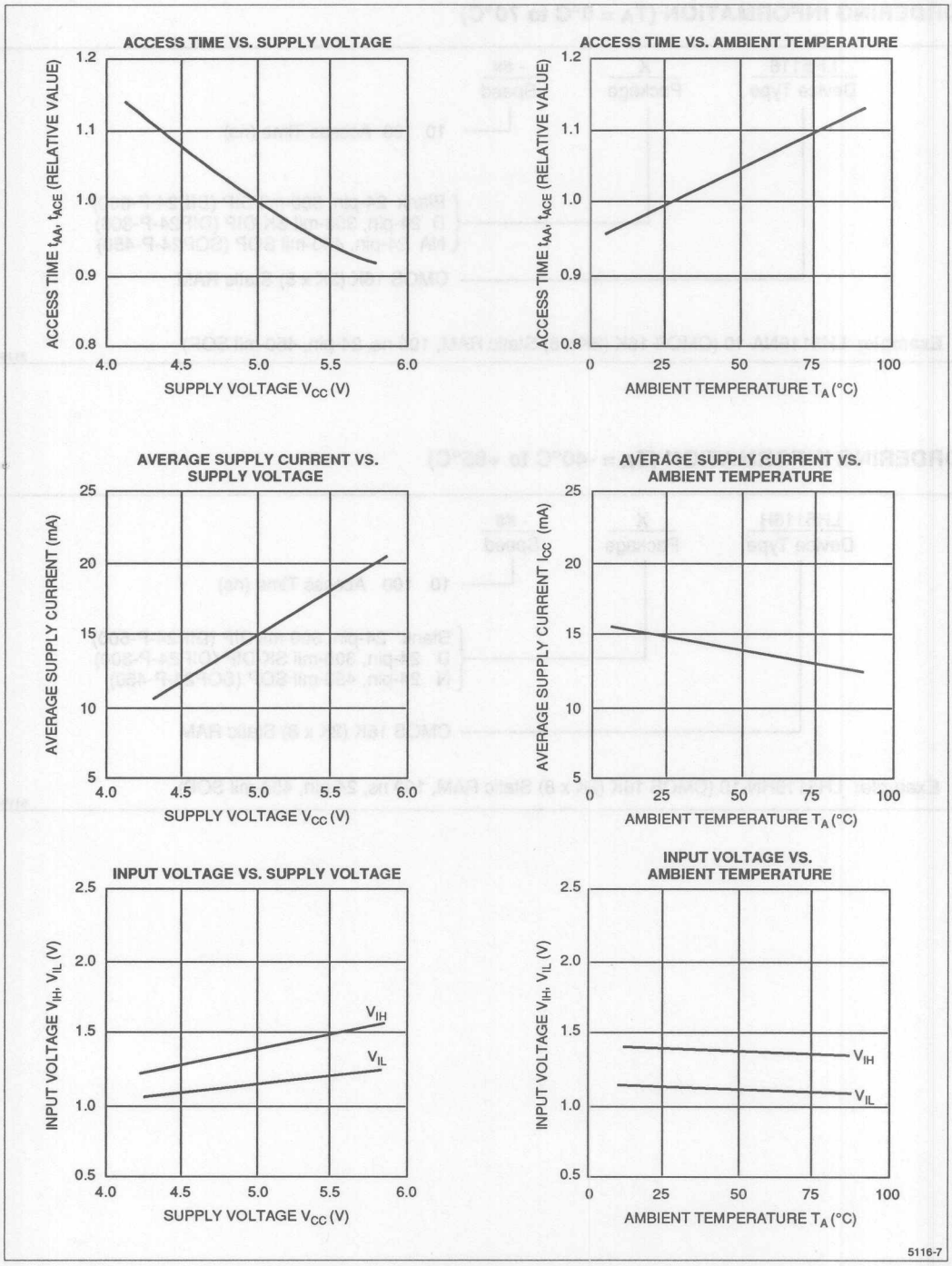
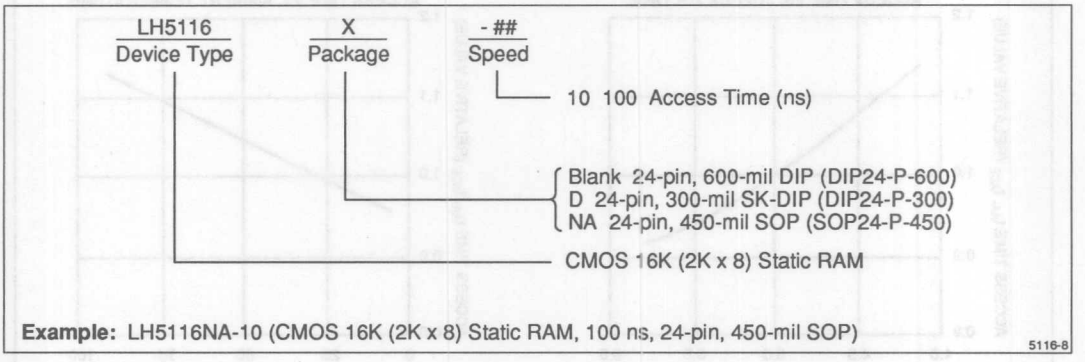
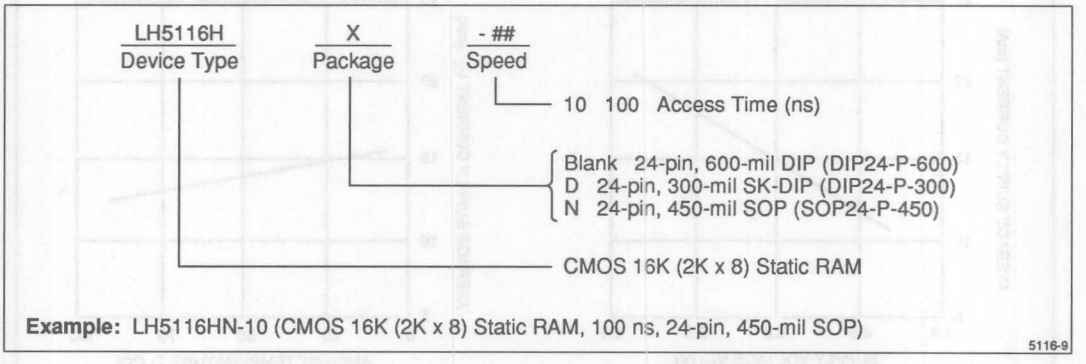


Figure 7. Electrical Characteristic Curves
(V_{CC} = 5 V, T_A = 25°C unless otherwise specified)

ORDERING INFORMATION (T_A = 0°C to 70°C)



ORDERING INFORMATION (T_A = -40°C to +85°C)



LH5116S

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time:
  1000 ns (MAX.)
- Low power consumption:
  Operating: 33 mW (MAX.)
  Standby: 3.3 µW (MAX.)
- Fully static operation
- Three-state outputs
- Single +3 V power supply
- Package:
  24-pin, 450-mil SOP

DESCRIPTION

The LH5116S is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology. It operates at a low supply voltage of 3 V ± 10%.

PIN CONNECTIONS

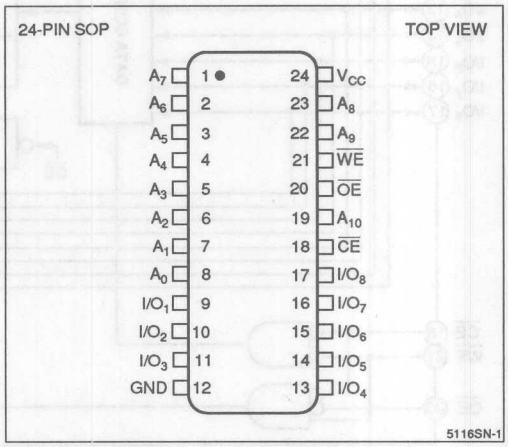


Figure 1. Pin Connections for SOP Package

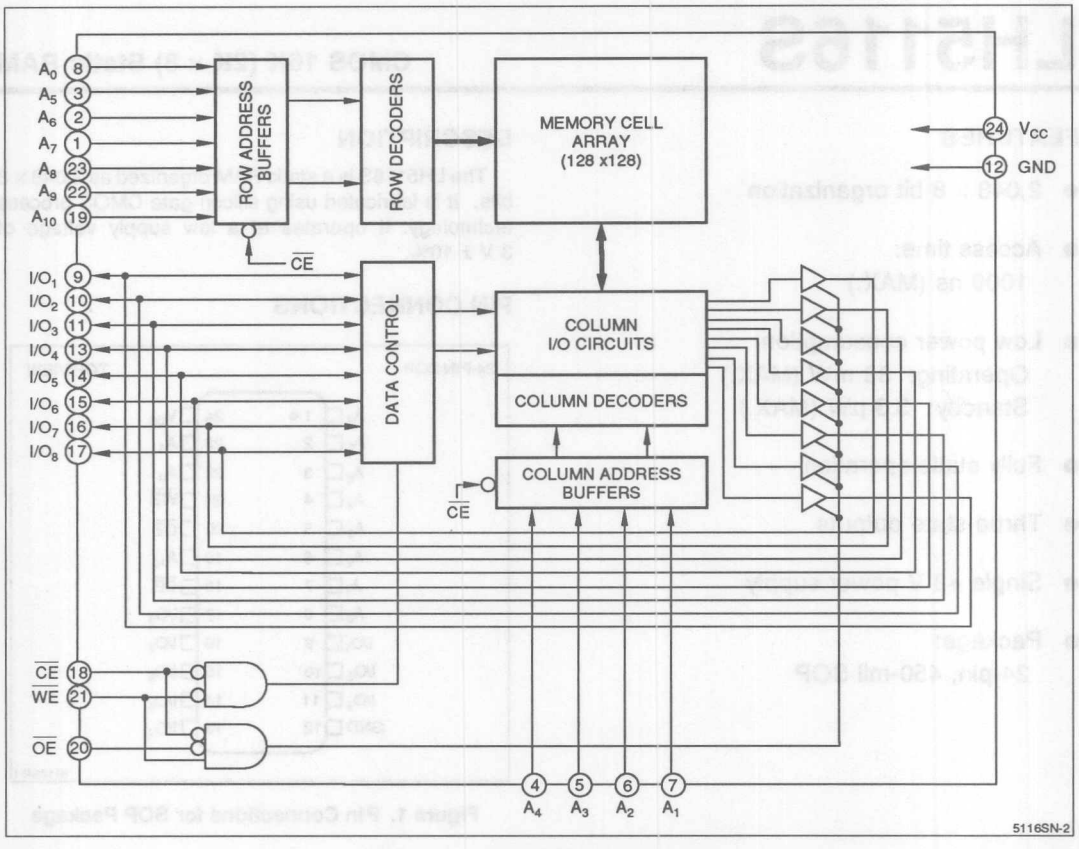


Figure 2. LH5116S Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE}$	Chip Enable input
$\overline{OE}$	Output Enable input
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data input/output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
L	X	L	Write	D_{IN}	Operating (I_{CC})	1
L	L	H	Read	D_{OUT}	Operating (I_{CC})	
H	X	X	Deselected	High-Z	Standby (I_{SB})	1
L	H	X	Output disable	High-Z	Operating (I_{CC})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	0 to +50	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +50°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.7	3.0	3.3	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 3 V ± 10%, T_A = 0 to +50°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output "LOW" voltage	V_{OL}	I_{OL} = 2.1 mA			0.5	V	
Output "HIGH" voltage	V_{OH}	I_{OH} = -1.0 mA	V_{CC} - 0.5			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}			1.0	µA	
Operating current	I_{CC1}	Outputs open ($\overline{OE}$ = V_{CC})		8	10	mA	1
	I_{CC2}	Outputs open ($\overline{OE}$ = V_{IH})		8	10	mA	2
Standby current	I_{CCL}	$\overline{CE}$ ≥ V_{CC} - 0.2 V All other input pins = 0 V to V_{CC}			1.0	µA	

NOTES:
1. $\overline{CE}$ = 0 V; all other input pins = 0 V to V_{CC}
2. $\overline{CE}$ = V_{IL}; all other input pins = V_{IL} to V_{IH}

AC CHARACTERISTICS (V_{CC} = 3 V ± 10%, T_A = 0 to +50°C)

(1) READ CYCLE

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	1000			ns	
Address access time	t_{AA}			1000	ns	
Chip enable access time	t_{ACE}			1000	ns	
$\overline{CE}$ Low to output in Low-Z	t_{CLZ}	10			ns	1
Output enable access time	t_{OE}			100	ns	
Output enable Low to output in Low-Z	t_{OLZ}	10			ns	1
Chip disable to output in High-Z	t_{CHZ}	0		40	ns	1
Output enable to output in High-Z	t_{OHZ}	0		40	ns	1
Output hold time	t_{OH}	10			ns	

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

(2) WRITE CYCLE (V_{CC} = 3 V ± 10%, T_A = 0 to +50°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	1000			ns	
Chip enable to end of write	t_{CW}	100			ns	
Address valid time	t_{AW}	100			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	100			ns	
Write recovery time	t_{WR}	20			ns	
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	1
Data valid to end of write	t_{DW}	50			ns	
Data hold time	t_{DH}	20			ns	
Output active from end of write	t_{OW}	10			ns	1
Output enable to output in High-Z	t_{OHZ}			40	ns	1

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 to V_{CC}
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS (T_A = 0 to +50°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V, V_{CCDR} = 2.0 V			1.0	µA	
					0.2		1
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	2

NOTES:
1. T_A = 25°C
2. t_{RC} = Read cycle time

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

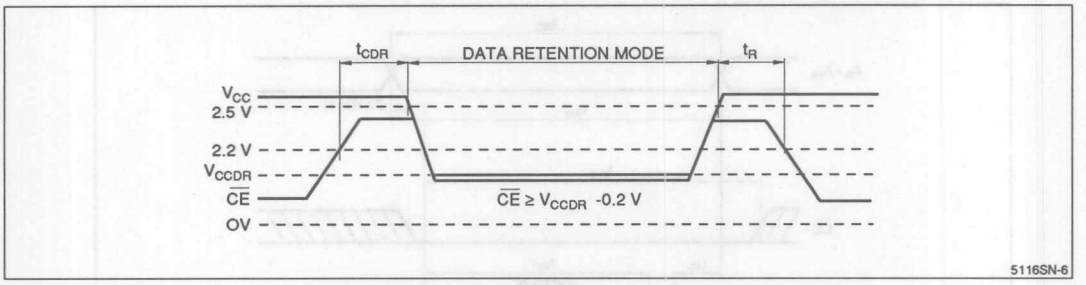


Figure 3. Low Voltage Data Retention

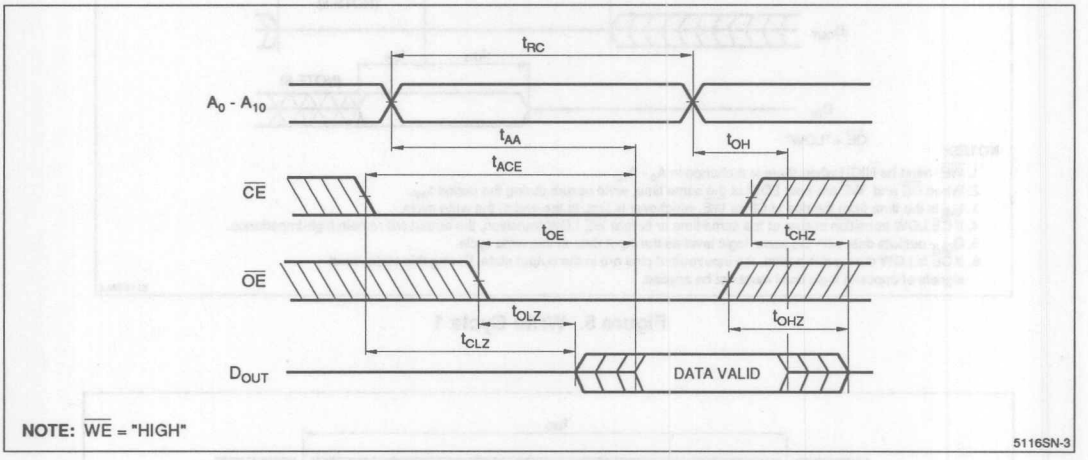
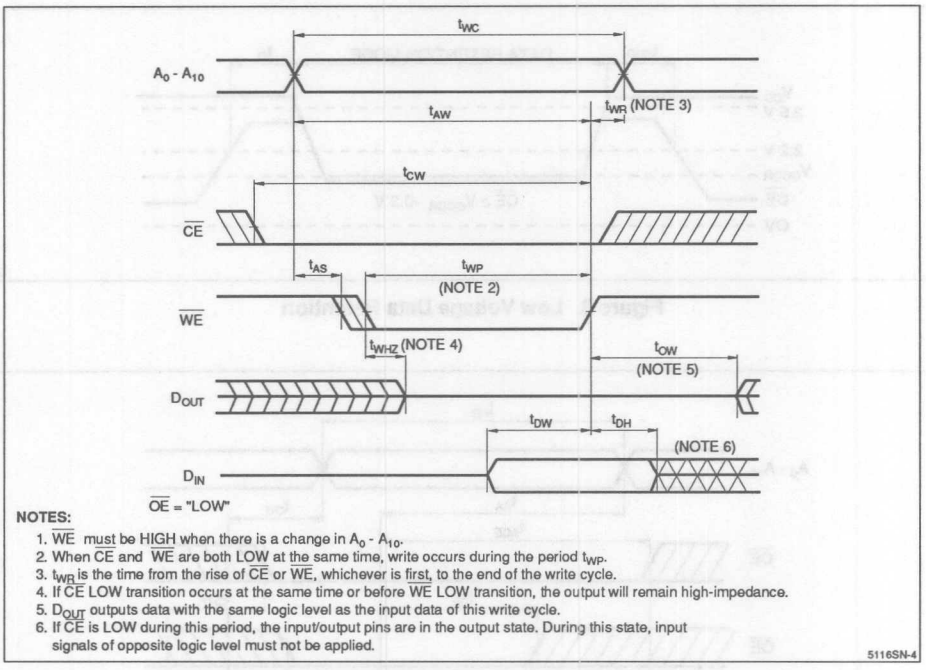


Figure 4. Read Cycle

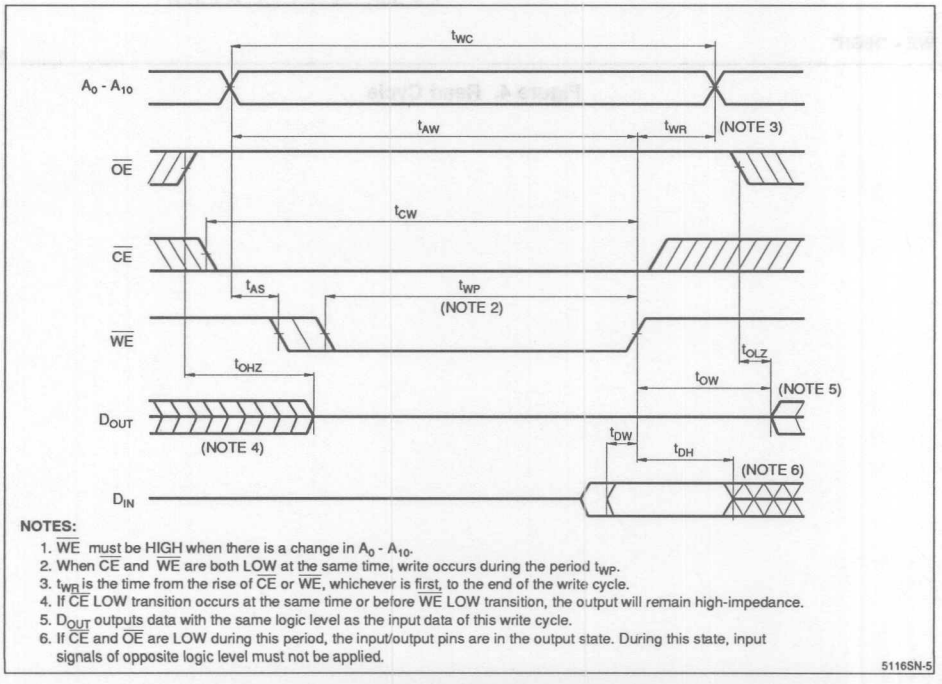


NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are both LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the output will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ is LOW during this period, the input/output pins are in the output state. During this state, input signals of opposite logic level must not be applied.

5116SN-4

Figure 5. Write Cycle 1



NOTES:

1. $\overline{WE}$ must be HIGH when there is a change in A_0 - A_{10}.
2. When $\overline{CE}$ and $\overline{WE}$ are both LOW at the same time, write occurs during the period t_{WP}.
3. t_{WR} is the time from the rise of $\overline{CE}$ or $\overline{WE}$, whichever is first, to the end of the write cycle.
4. If $\overline{CE}$ LOW transition occurs at the same time or before $\overline{WE}$ LOW transition, the output will remain high-impedance.
5. D_{OUT} outputs data with the same logic level as the input data of this write cycle.
6. If $\overline{CE}$ and $\overline{OE}$ are LOW during this period, the input/output pins are in the output state. During this state, input signals of opposite logic level must not be applied.

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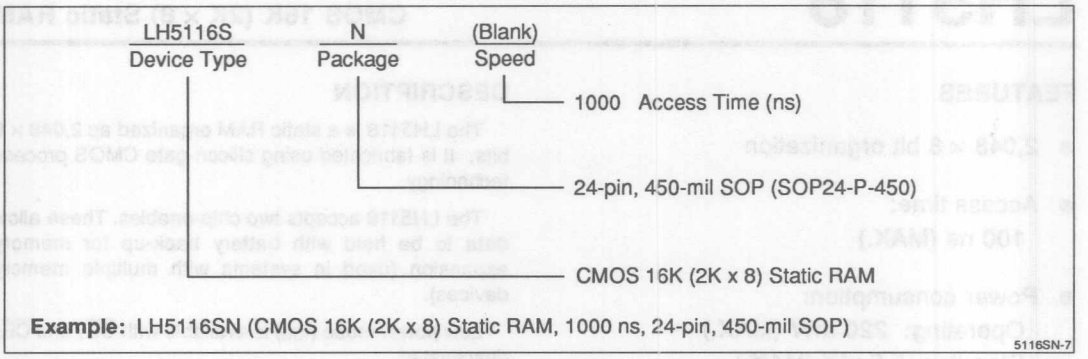
Figure 6. Write Cycle 2

ORDERING INFORMATION



LH5118

CMOS 16K (2K × 8) Static RAM

FEATURES

- 2,048 × 8 bit organization
- Access time:
  100 ns (MAX.)
- Power consumption:
  Operating: 220 mW (MAX.)
  Standby: 5.5 µW (MAX.)
- Single +5 V power supply
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Wide temperature range available
  LH5118H: -40 to + 85°C
- Packages:
  24-pin, 600-mil DIP
  24-pin, 300-mil SK-DIP
  24-pin, 450-mil SOP

DESCRIPTION

The LH5118 is a static RAM organized as 2,048 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5118 accepts two chip-enables. These allow data to be held with battery back-up for memory expansion (used in systems with multiple memory devices).

Low power mode (I_{SB}) is available with $\overline{CE}_1$ and $\overline{CE}_2$ deactivated.

PIN CONNECTIONS

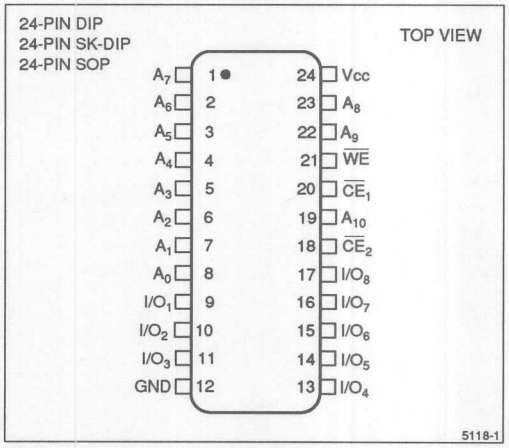


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

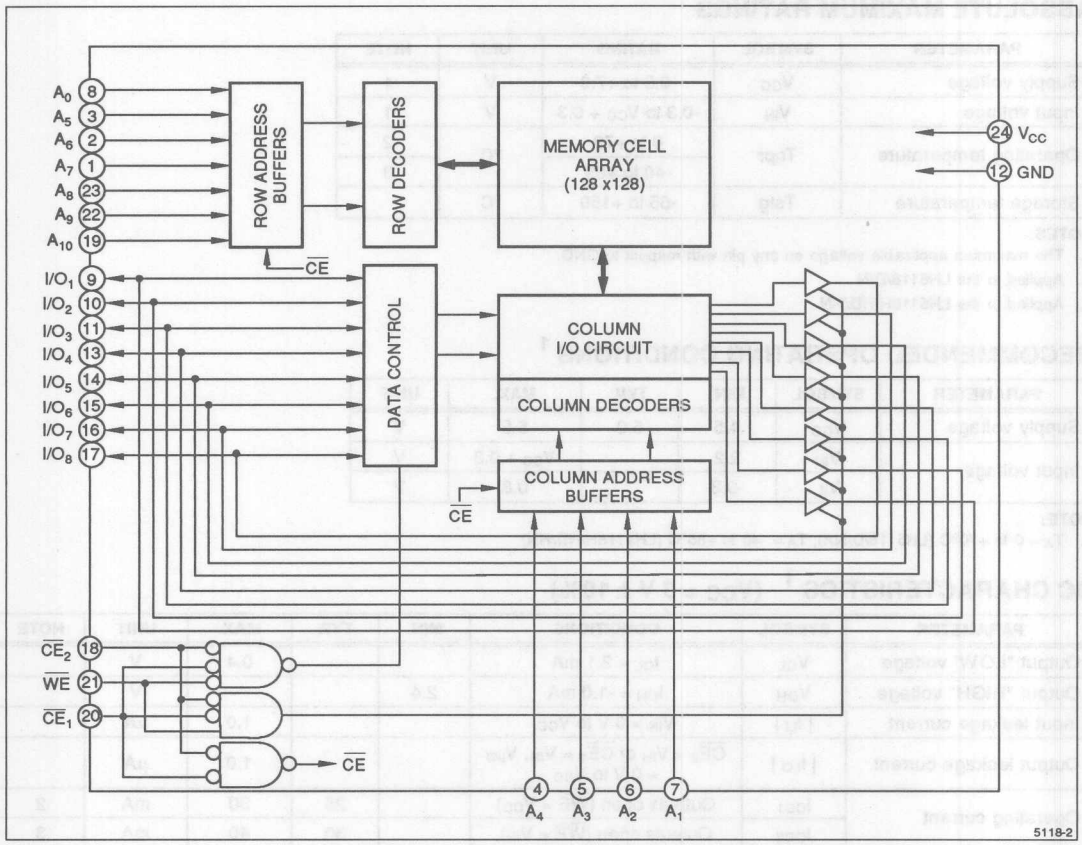


Figure 2. LH5118 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{10}	Address input
$\overline{CE_2}$	Chip Enable input no. 2
$\overline{CE_1}$	Chip Enable input no. 1
$\overline{WE}$	Write Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE_1}$	$\overline{CE_2}$	$\overline{WE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
X	H	X	Deselect	High-Z	Standby (I_{SB})	1
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	L	L	Write	D_{IN}	Operating (I_{CC})	
L	L	H	Read	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V	1
Operating temperature	Topr	0 to +70	°C	2
		-40 to +85		3
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. Applied to the LH5118/D/N
3. Applied to the LH5118H/HD/HN

RECOMMENDED OPERATING CONDITIONS [1]

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

NOTE:
1. T_A = 0 to +70°C (LH5118/D/NA), T_A = -40 to +85°C (LH5118H/HD/HN)

DC CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output "LOW" voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
Output "HIGH" voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_2}$ = V_{IH} or $\overline{CE_1}$ = V_{IH}, $V_{I/O}$ = 0 V to V_{CC}			1.0	µA	
Operating current	I_{CC1}	Outputs open ($\overline{WE}$ = V_{CC})		25	30	mA	2
	I_{CC2}	Outputs open ($\overline{WE}$ = V_{IH})		30	40	mA	3
Standby current	I_{SB}	(1) $\overline{CE_2} \geq V_{CC}$ - 0.2 V, and ($\overline{CE_1} \geq V_{CC}$ - 0.2 V or $\overline{CE_1} \leq$ 0.2 V) or			1.0	µA	
		(2) $\overline{CE_1} \geq V_{CC}$ - 0.2 V, and ($\overline{CE_2} \geq V_{CC}$ - 0.2 V or $\overline{CE_2} \leq$ 0.2 V) All other inputs = 0 V to V_{CC}			0.2	µA	4

NOTES:
1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. $\overline{CE_2}$ = $\overline{CE_1}$ = 0 V; all other input pins = 0 V to V_{CC}
3. $\overline{CE_2}$ = $\overline{CE_1}$ = V_{IL}; all other input pins = V_{IL} to V_{IH}
4. T_A = 25°C

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
$\overline{CE}_1$ access time	t_{ACE1}			100	ns	
$\overline{CE}_2$ access time	t_{ACE2}			100	ns	
$\overline{CE}_1$ Low to output in Low-Z	t_{CLZ1}	10			ns	2
$\overline{CE}_2$ Low to output in Low-Z	t_{CLZ2}	10			ns	2
$\overline{CE}_1$ to output in High-Z	t_{CHZ1}	0		40	ns	2
$\overline{CE}_2$ to output in High-Z	t_{CHZ2}	0		40	ns	2
Data hold time	t_{OH}	10			ns	

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100			ns	
Chip enable to end of write	t_{CW}	80			ns	
Address valid time	t_{AW}	80			ns	
Address setup time	t_{AS}	0			ns	
Write pulse width	t_{WP}	60			ns	
Write recovery time	t_{WR}	10			ns	
$\overline{WE}$ Low to output in High-Z	t_{WHZ}			30	ns	2
Data valid to end of write	t_{DW}	30			ns	
Data hold time	t_{DH}	10			ns	
Output active from end of write	t_{OW}	10			ns	2

NOTE:

1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.8 V to 2.2 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output load condition	1TTL + 100 pF

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE_1} \geq V_{CCDR}$ - 0.2V or $\overline{CE_2} \geq V_{CCDR}$ - 0.2 V	2.0			V	
Data retention current	I_{CCDR}	$\overline{CE_1} \geq V_{CCDR}$ - 0.2V, and ($\overline{CE_2} \geq V_{CCDR}$ - 0.2 V or $\overline{CE_2} \leq$ 0.2 V) or			1.0	µA	
		$\overline{CE_2} \geq V_{CCDR}$ - 0.2V, and ($\overline{CE_1} \geq V_{CCDR}$ - 0.2 V or $\overline{CE_1} \leq$ 0.2 V) V_{CCDR} = 3.0 V			0.2		2
Chip disable to data retention	t_{CDR}		0			ns	
Recovery time	t_R		t_{RC}			ns	3

NOTES:
1. T_A = 0 to +70°C (LH5118/D/N), T_A = -40 to +85°C (LH5118H/HD/HN)
2. T_A = 25°C
3. t_{RC} = Read cycle time

CAPACITANCE [1] (f = 1MHz, T_A = 25°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

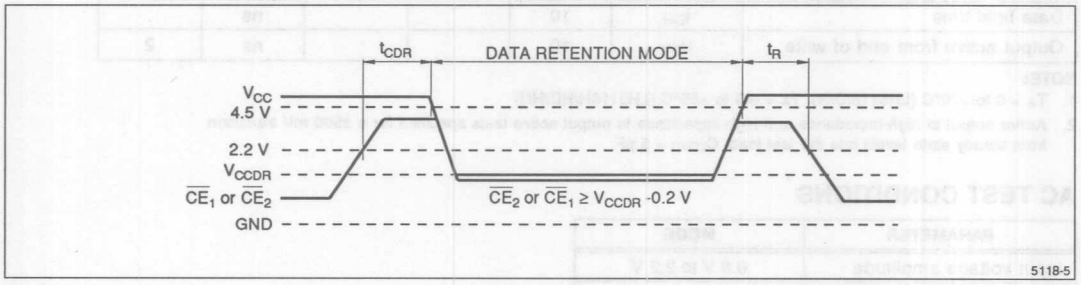


Figure 3. Low Voltage Data Retention

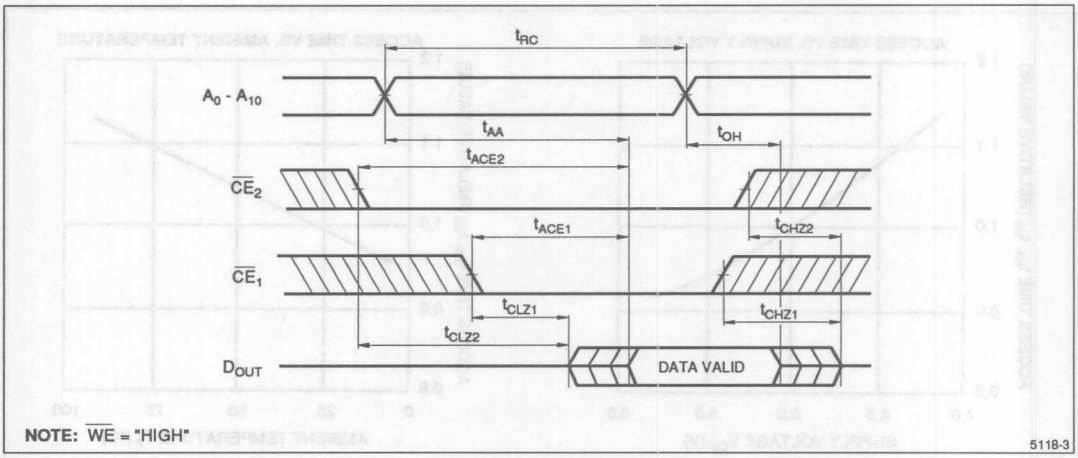


Figure 4. Read Cycle

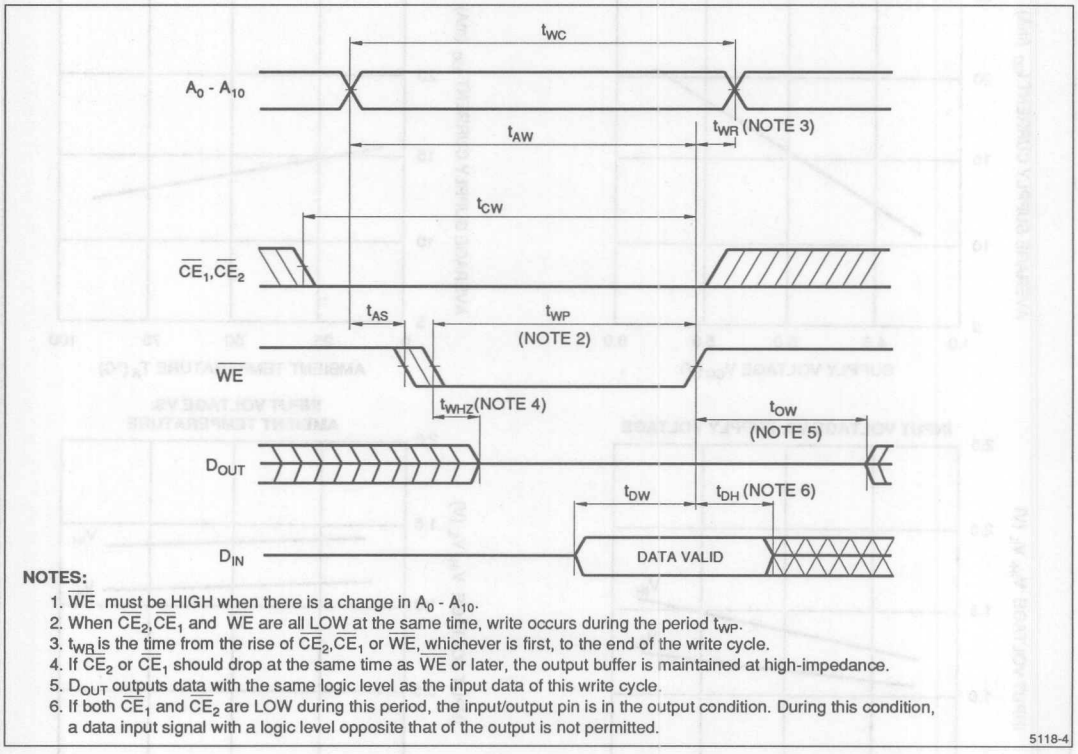


Figure 5. Write Cycle (Note 1)

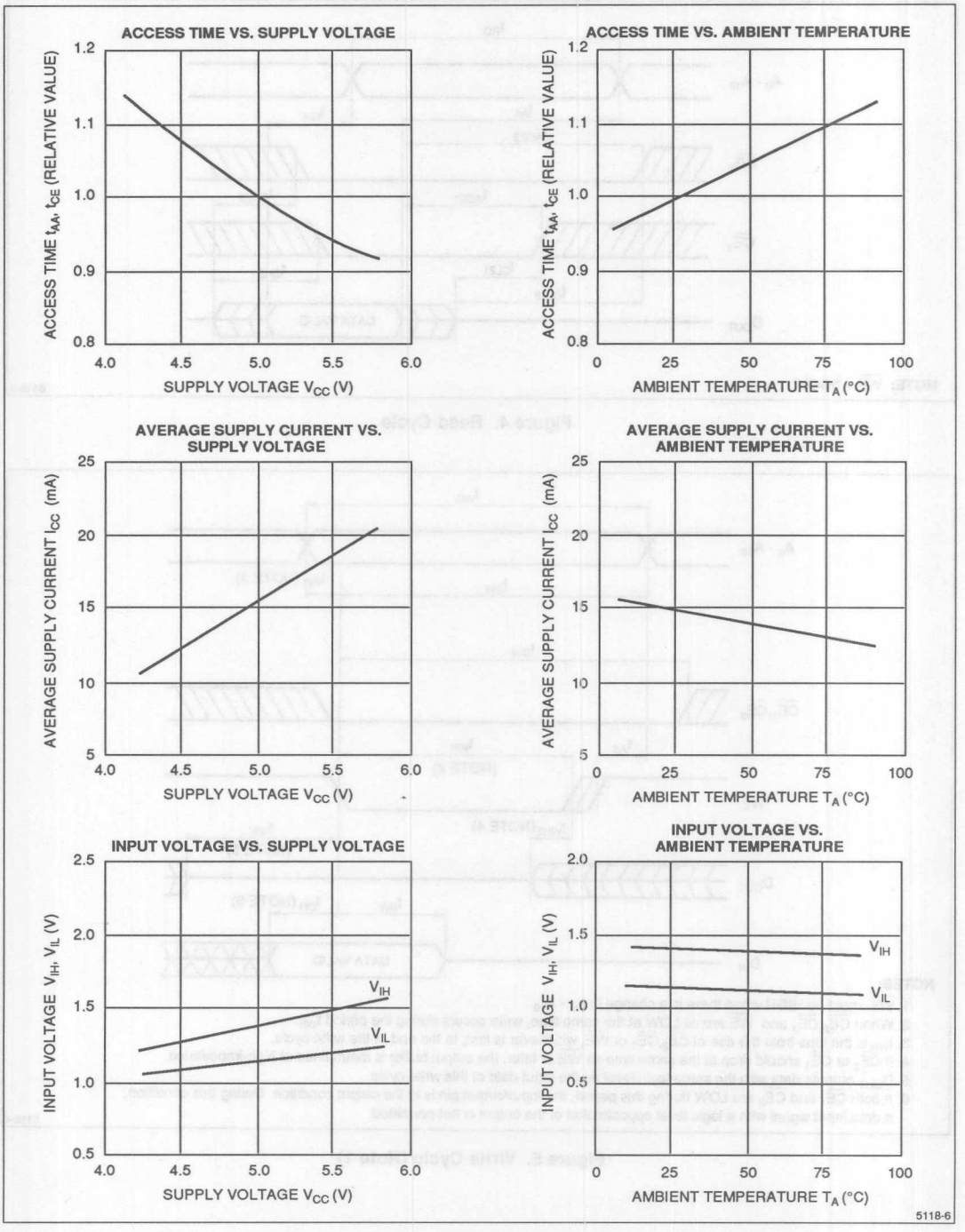
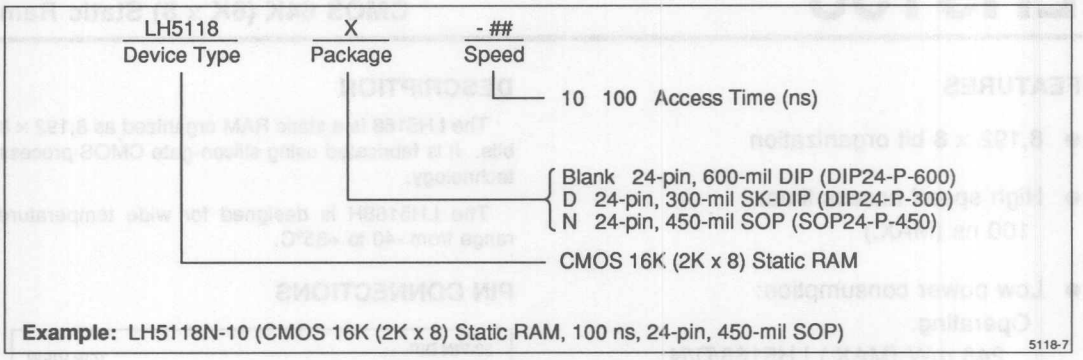


Figure 6. Electrical Characteristic Curves
(V_{CC} = 5 V, T_A = 25°C Unless Otherwise Specified)

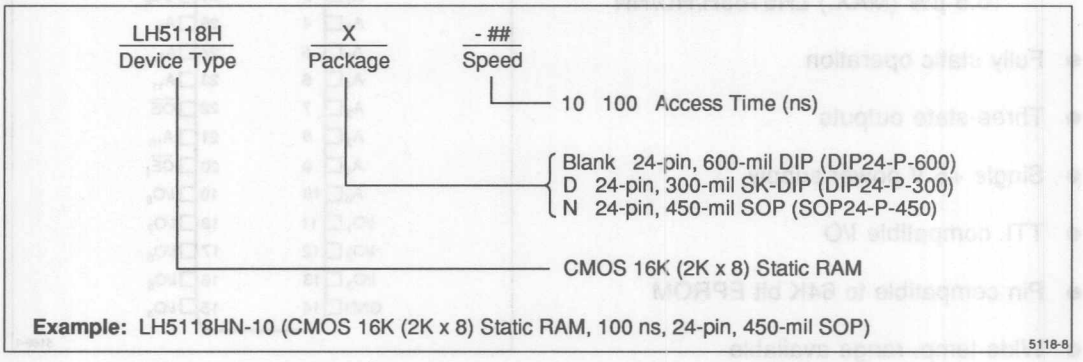
ORDERING INFORMATION (T_A = 0 to +70°C)



Example: LH5118N-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)

5118-7

ORDERING INFORMATION (T_A = -40 to +85°C)



Example: LH5118HN-10 (CMOS 16K (2K x 8) Static RAM, 100 ns, 24-pin, 450-mil SOP)

5118-8

LH5168

CMOS 64K (8K × 8) Static Ram

FEATURES

- 8,192 × 8 bit organization
- High speed access time:
  100 ns (MAX.)
- Low power consumption:
  Operating:
  248 mW (MAX.) LH5168/D/N
  275 mW (MAX.) LH5168H/HD/HN
  Standby:
  5.5 µW (MAX.) LH5168/D/N
  16.5 µW (MAX.) LH5168H/HD/HN
- Fully static operation
- Three-state outputs
- Single +5 V power supply
- TTL compatible I/O
- Pin compatible to 64K bit EPROM
- Wide temp. range available
  LH5168H: -40 to +85°C
- Packages:
  28-pin, 600-mil DIP
  28-pin, 300-mil SK-DIP
  28-pin, 450-mil SOP
  28-pin, TSOP (Type I)

DESCRIPTION

The LH5168 is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

The LH5168H is designed for wide temperature range from -40 to +85°C.

PIN CONNECTIONS

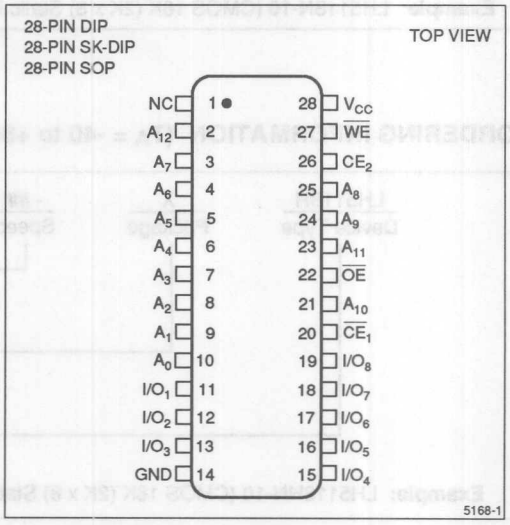


Figure 1. Pin Connections for DIP, SK-DIP, and SOP Packages

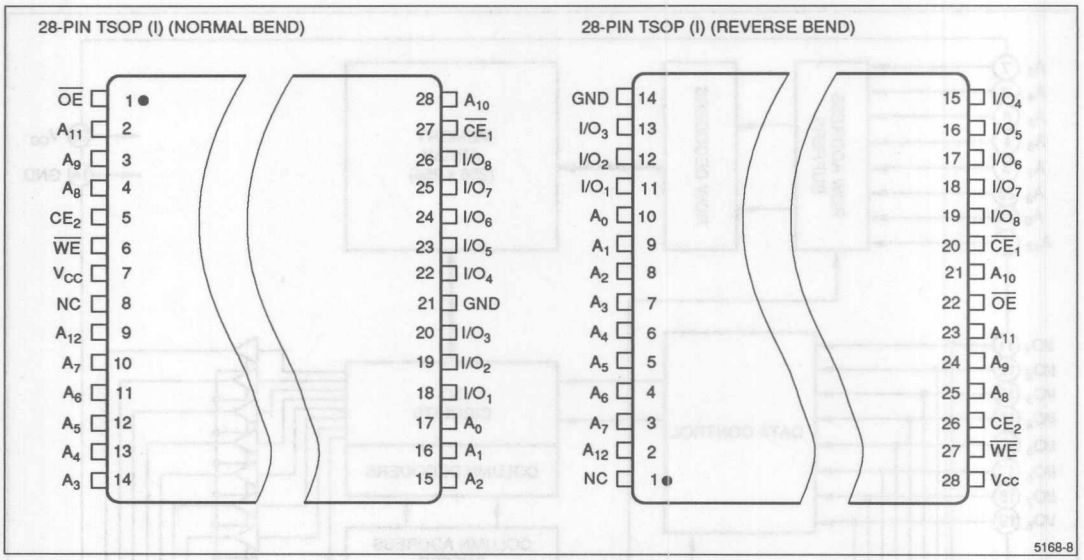


Figure 2. Pin Connections for TSOP Packages

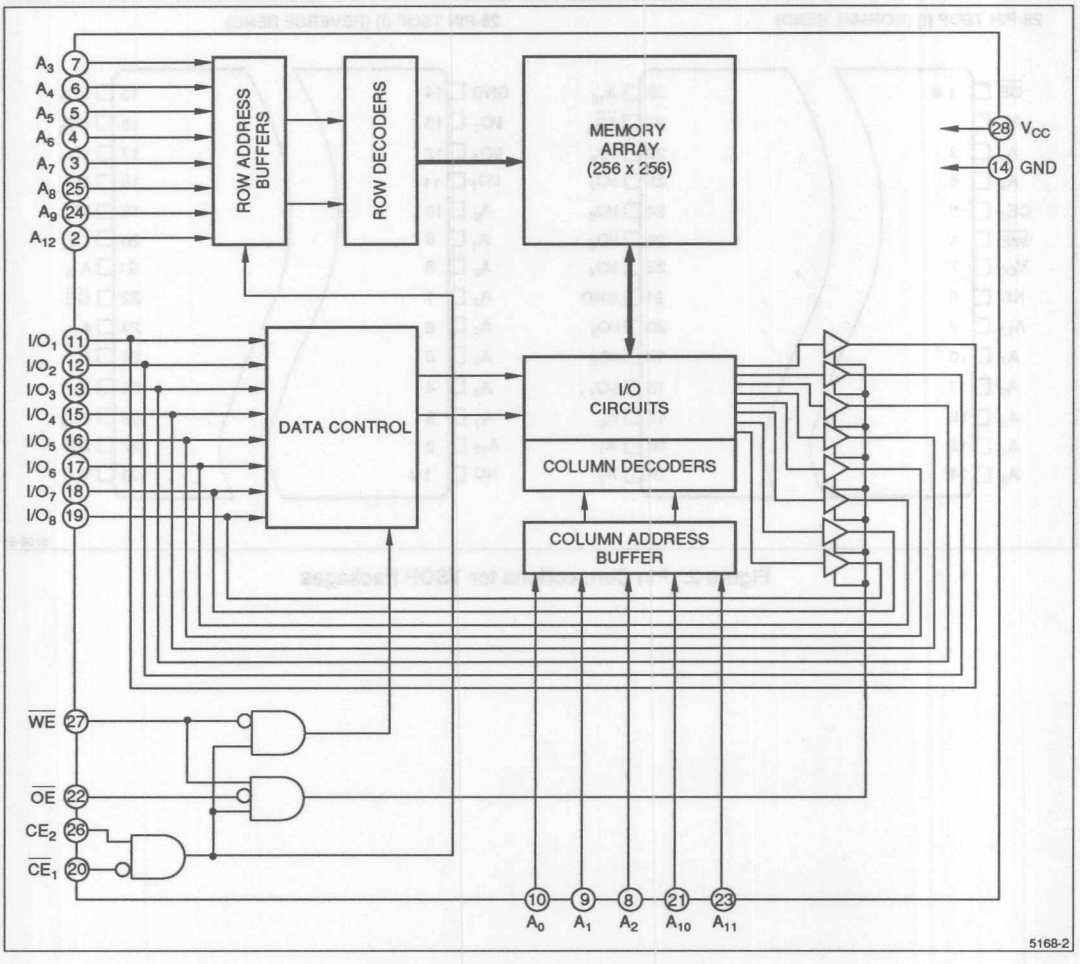


Figure 3. LH5168 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE_1}$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	Non-connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I_{SB})	1
X	L	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	-10 to +70	°C	2
		-40 to +85	°C	3
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.
2. LH5168/D/N
3. LH5168H/HD/HN

RECOMMENDED OPERATING CONDITIONS (Note 1)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

NOTE:
1. T_A = -10 to +70°C (LH5168/D/N), T_A = -40 to +85°C (LH5168H/HD/HN).

DC CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Input leakage current	I_{LI}	V_{IN} = 0 to V_{CC}			1.0	µA	
Output leakage current	I_{LO}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 to V_{CC}			1.0	µA	
Operating current	I_{CC}	$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} to V_{IH} CE_2 = V_{IH}, Outputs open	t_{CYCLE} = 100 ns		45	mA	2
					50		3
		$\overline{CE_1}$ = V_{IL}, V_{IN} = 0.2 V to V_{CC} - 0.2 V CE_2 = V_{IH}, Outputs open	t_{CYCLE} = 1.0 µs		10		
Standby current	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			10	mA	
	I_{SB}	CE_2 ≤ 0.2 V or $\overline{CE_1}$, CE_2 ≥ V_{CC} - 0.2 V	T_A ≤ 70°C		1.0	µA	2
			T_A ≤ 85°C		3.0	µA	3
Output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V	
	V_{OH}	I_{OH} = -1 mA		2.4		V	

NOTES:
1. T_A = -10 to 70°C (LH5168/D/N), T_A = -40 to +85°C (LH5168H/HD/HN)
2. LH5168/D/N
3. LH5168H/HD/HN

AC CHARACTERISTICS [1]

(1) READ CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle		t_{RC}	100		ns	
Address access time		t_{AA}		100	ns	
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		100	ns	
	(CE_2)	t_{ACE2}		100	ns	
Output enable access time		t_{OE}		40	ns	
Output hold time		t_{OH}	10		ns	
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	10		ns	2
	(CE_2)	t_{LZ2}	10		ns	2
Output enable to output in Low-Z		t_{OLZ}	5		ns	2
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	30	ns	2
	(CE_2)	t_{HZ2}	0	30	ns	2
Output disable to output in High-Z		t_{OHZ}	0	20	ns	2

NOTE:

1. T_A = -10 to +70°C (LH5168/D/N), T_A = -40 to +85°C (LH5168H/HD/HN)
2. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	100		ns	
Chip enable to end of write	t_{CW}	80		ns	
Address valid to end of write	t_{AW}	80		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	60		ns	
Write recovery time	t_{WR}	0		ns	
Data valid to end of write	t_{DW}	40		ns	
Data hold time	t_{DH}	0		ns	
Output active from end of write	t_{OW}	10		ns	1
$\overline{WE}$ to output in High-Z	t_{WZ}	0	30	ns	1
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	20	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	(1TTL + C_L = 100 pF)

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

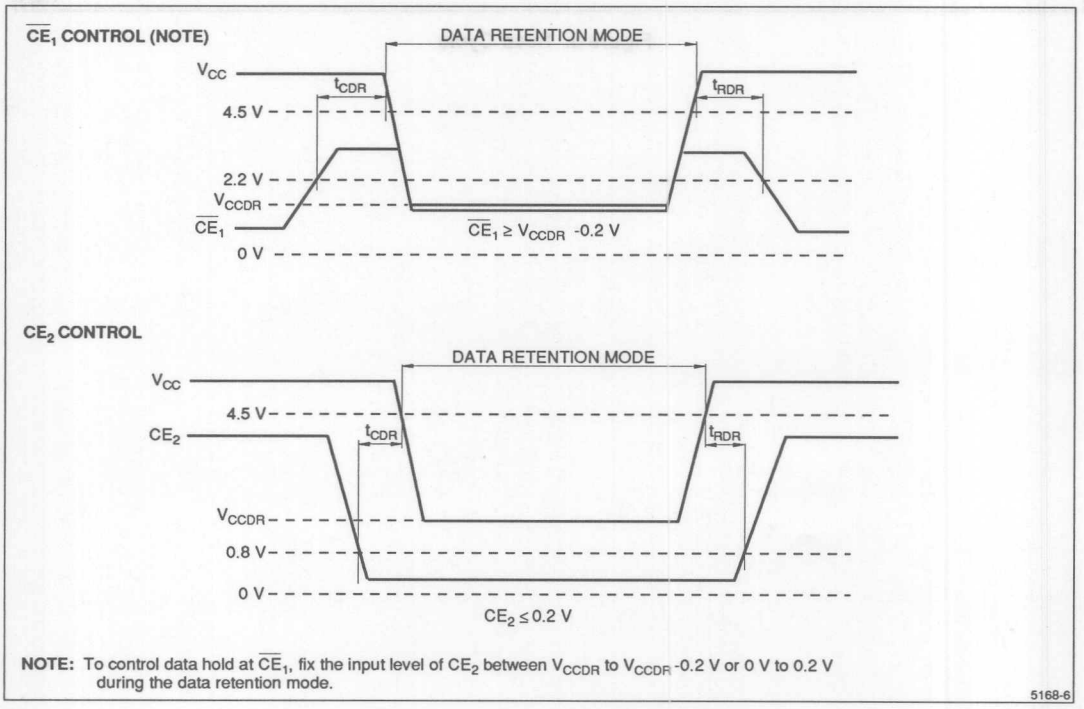
PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS [1]

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE_1}$, $CE_2 \ge V_{CC}$ - 0.2 V	2.0		V	
Data retention current	I_{CCDR}	V_{CCDR} = 3 V, $CE_2 \le 0.2$ V or $\overline{CE_1}$, $CE_2 \ge V_{CCDR}$ - 0.2 V		0.6	µA	2
				1.5	µA	3
Chip disable to data retention	t_{CDR}		0		ns	
Recovery time	t_{RDR}		t_{RC}		ns	4

NOTES:
1. T_A = -10 to +70°C (LH5168/D/N), T_A = -40 to +85°C (LH5168H/HD/HN)
2. LH5168/D/N at $T_A \le 70$°C
3. LH5168H/HD/HN at $T_A \le 85$°C
4. t_{RC} = Read cycle time



NOTE: To control data hold at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} -0.2 V or 0 V to 0.2 V during the data retention mode.

5168-6

Figure 4. Low Voltage Data Retention

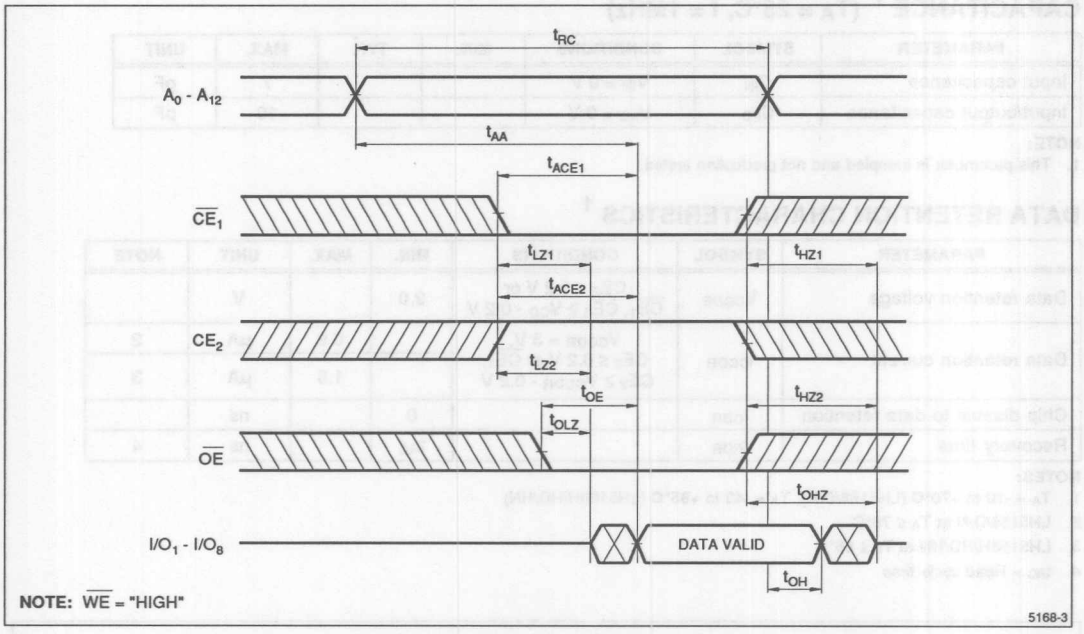
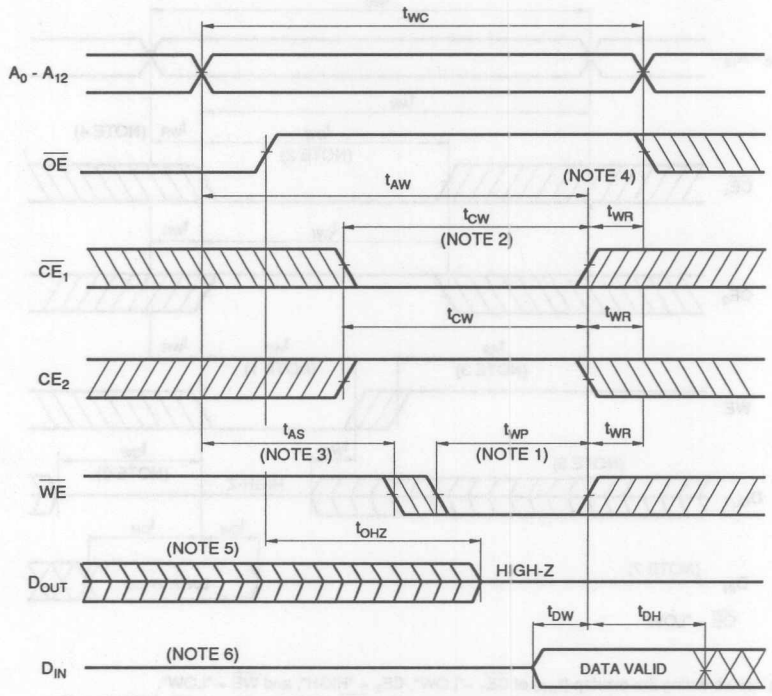


Figure 5. Read Cycle

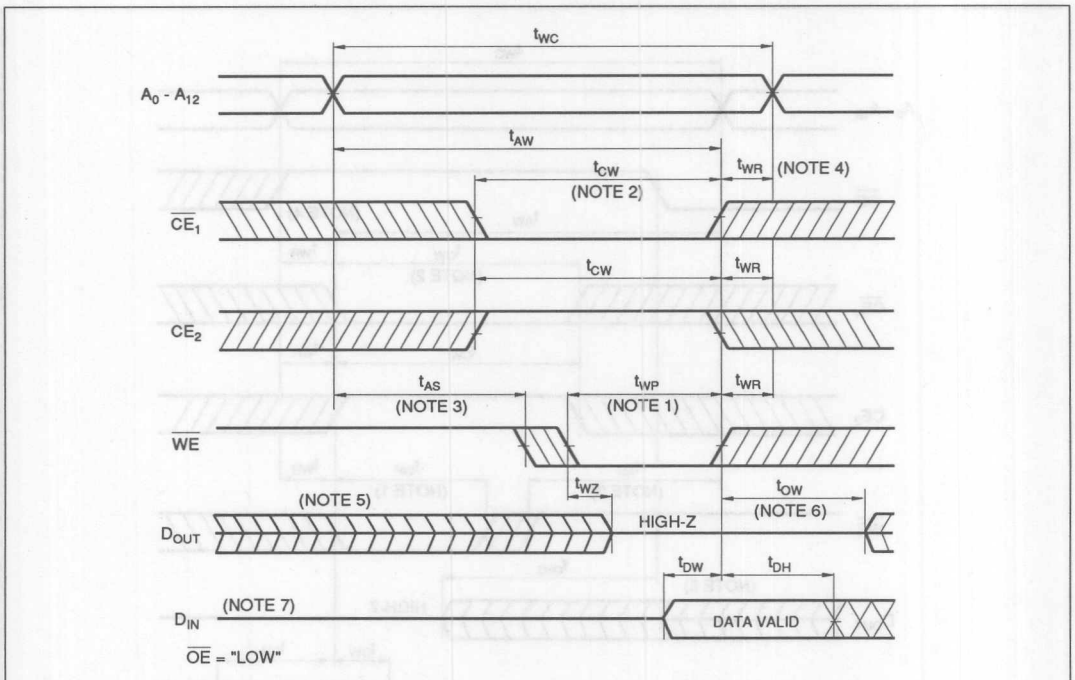


NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5168-4

Figure 6. Write Cycle 1



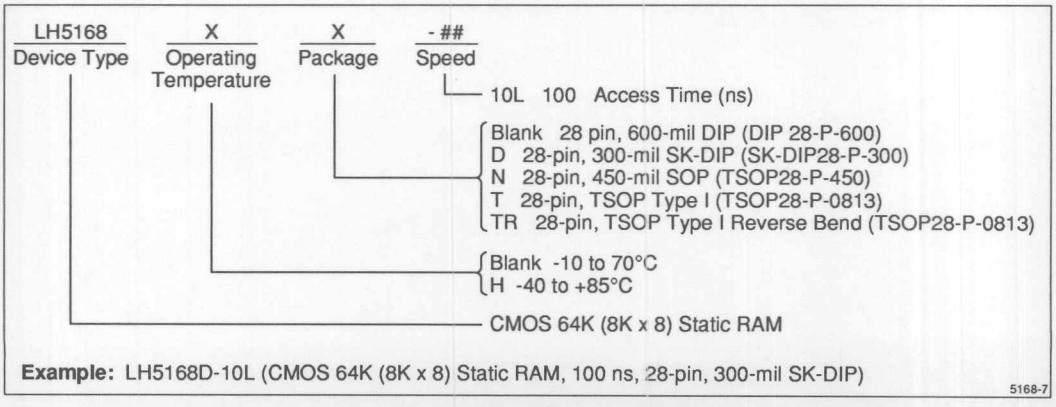
NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
7. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5168-5

Figure 7. Write Cycle 2

ORDERING INFORMATION



Example: LH5168D-10L (CMOS 64K (8K x 8) Static RAM, 100 ns, 28-pin, 300-mil SK-DIP)

5168-7

LH5168SH

CMOS 64K (8K × 8) Static Ram

FEATURES

- 8,192 × 8 bit organization
- Access time:
  500 ns (MAX.)
- Low current consumption:
  Operating:
  20 mA (MAX.),
  10 mA (t_{RC}, t_{WC} = 1 µS)
  Standby:
  1 µA (MAX.) @ 70°C
  3 µA (MAX.) @ 85°C
- Fully static operation
- Three-state outputs
- Single 2.5 to 5.5 V power supply
- TTL compatible I/O
- Wide temp. range
  t_{OPR}: -40 to +85°C
- Package:
  28-pin, 450-mil SOP

DESCRIPTION

The LH5168SH is a static RAM organized as 8,192 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

It is designed for 2.5 to 5.5 V low voltage operation and wide temperature range from -40 to +85°C.

PIN CONNECTIONS

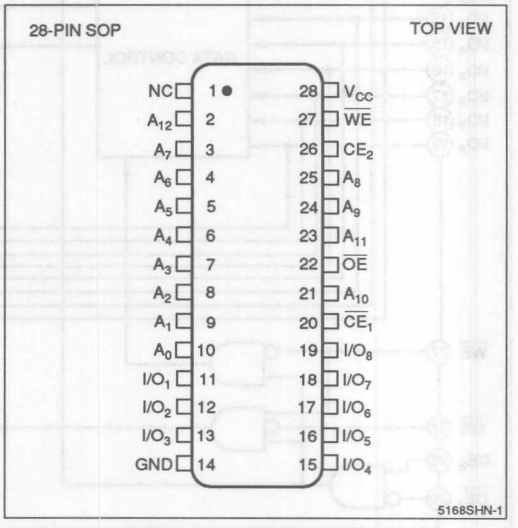


Figure 1. Pin Connections for SOP Package

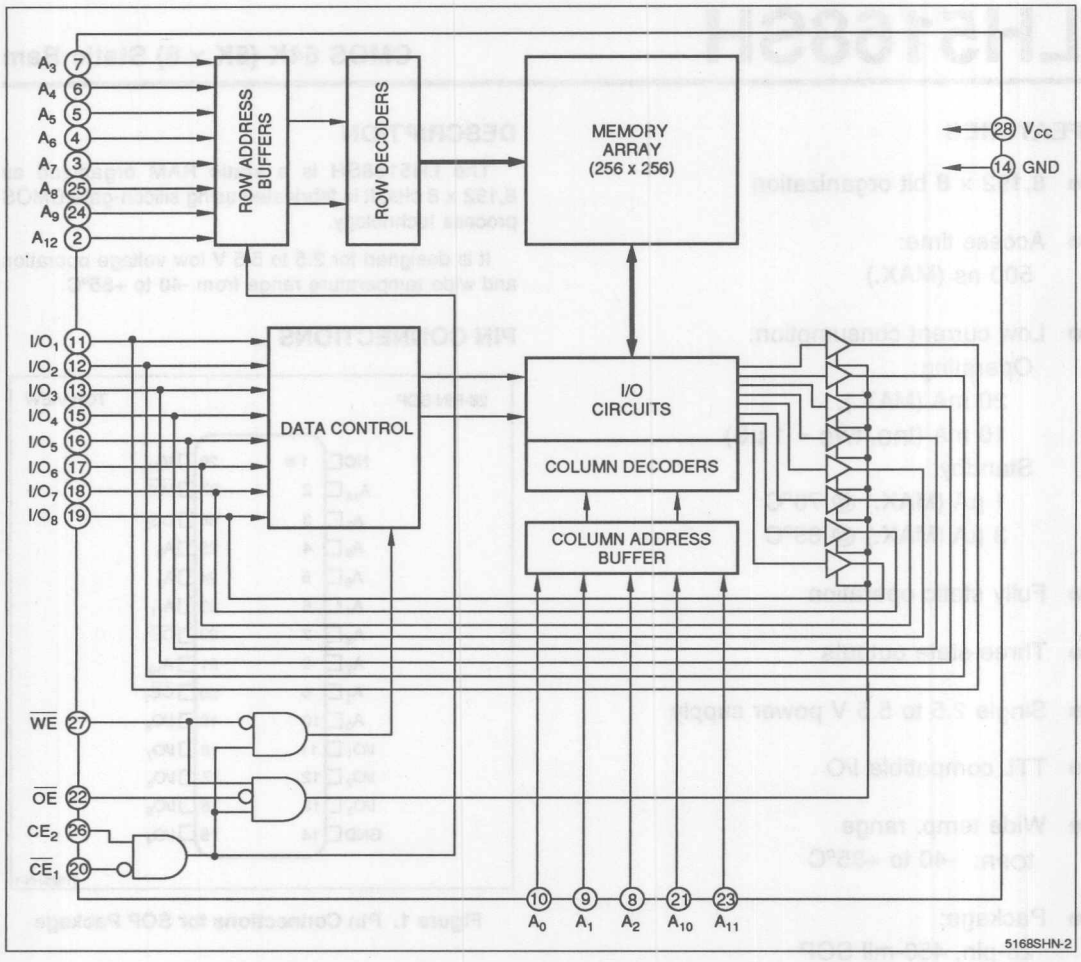


Figure 2. LH5168SH Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{12}	Address inputs
$\overline{CE_1}$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground
NC	Non connection

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	X	Deselect	High-Z	Standby (I_{SB})	1
X	L	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	2.5	3.0	5.5	V
Input voltage (V_{CC} = 2.5 to 4.5 V)	V_{IH}	V_{CC} - 0.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.2	V
Input voltage (V_{CC} = 4.5 to 5.5 V)	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 to V_{CC}		-1.0	1.0	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = 0 to V_{CC}		-1.0	1.0	µA	
Operating supply current	I_{CC}	$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Output open	t_{CYCLE} = 500 ns		20	mA	
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Output open	t_{CYCLE} = 1.0 µs		10		
		$\overline{CE_1}$ = 0.2 V, V_{IN} = 0.2 V or V_{CC} - 0.2 V CE_2 = V_{CC} - 0.2 V, Output open, V_{CC} = 3.3 V	t_{CYCLE} = 1.0 µs		8		
Standby current	I_{SB}	$CE_2 \le 0.2$ V or $\overline{CE_1} \ge V_{CC}$ - 0.2 V	~ +70°C		1.0	µA	
			~ +85°C		3.0		1
	I_{SB1}	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			5	mA	
Output Low voltage	V_{OL}	I_{OL} = 500 µA			0.5	V	
Output High voltage	V_{OH}	I_{OH} = -500 µA		V_{CC} - 0.5		V	2

NOTE:
1. CE_2 should be ≥ V_{CC} - 0.2 V or ≤ 0.2 V.
2. V_{OH} is 4.5 V (Min.) at V_{CC} > 5 V.

AC CHARACTERISTICS

(1) READ CYCLE (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER		SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle		t_{RC}	500		ns	
Address access time		t_{AA}		500	ns	
Chip enable access time	($\overline{CE}_1$)	t_{ACE1}		500	ns	
	(CE_2)	t_{ACE2}		500	ns	
Output enable access time		t_{OE}		200	ns	
Output hold time		t_{OH}	10		ns	
Chip enable to output in Low-Z	($\overline{CE}_1$)	t_{LZ1}	20		ns	1
	(CE_2)	t_{LZ2}	20		ns	1
Output enable to output in Low-Z		t_{OLZ}	10		ns	1
Chip enable to output in High-Z	($\overline{CE}_1$)	t_{HZ1}	0	60	ns	1
	(CE_2)	t_{HZ2}	0	60	ns	1
Output disable to output in High-Z		t_{OHZ}	0	40	ns	1

(2) WRITE CYCLE (T_A = -40 to +85°C, V_{CC} = 2.5 to 5.5 V)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	500		ns	
Chip enable to end of write	t_{CW}	250		ns	
Address valid to end of write	t_{AW}	250		ns	
Address setup time	t_{AS}	100		ns	
Write pulse width	t_{WP}	150		ns	
Write recovery time	t_{WR}	50		ns	
Data valid to end of write	t_{DW}	100		ns	
Data hold time	t_{DH}	0		ns	
Output active from end of write	t_{OW}	20		ns	
$\overline{WE}$ to output in High-Z	t_{WZ}	0	60	ns	1
$\overline{OE}$ to output in High-Z	t_{OHZ}	0	40	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0 to V_{CC}
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	No load

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

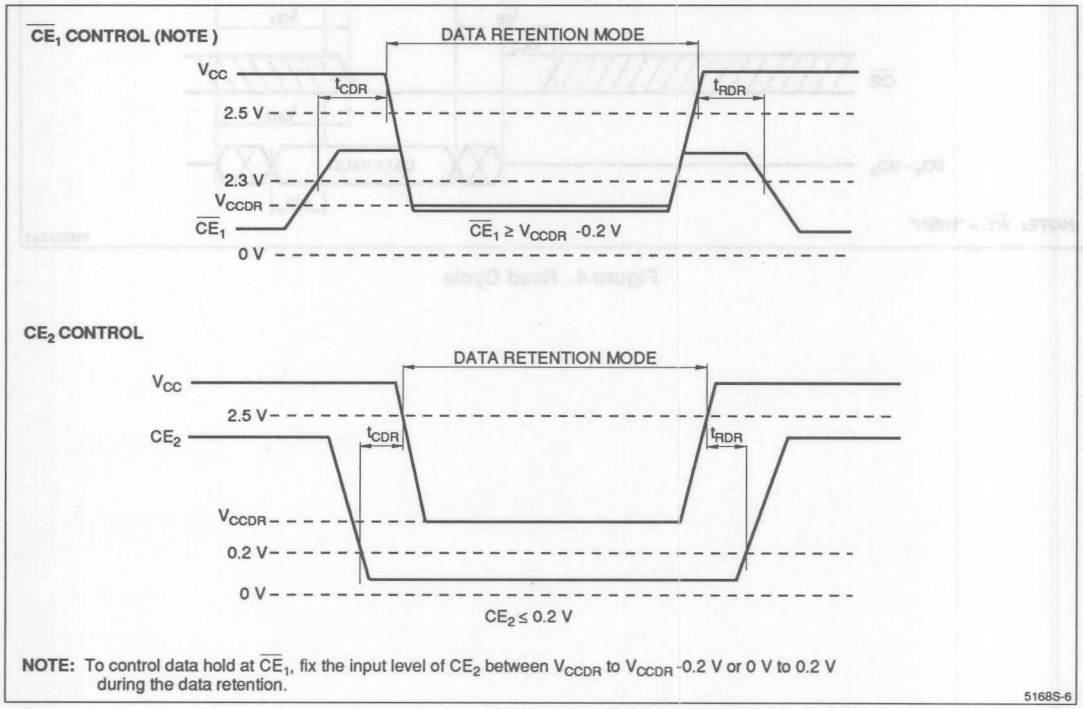
NOTE:

This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE_1} \geq V_{CCDR}$ - 0.2 V, $CE_2 \leq 0.2$ V		2.0		V	1
Data retention current	I_{CCDR}	V_{CCDR} = 3.0 V, $\overline{CE_1} \geq V_{CCDR}$ - 0.2 V, $CE_2 \leq 0.2$ V	T_A = 25°C		0.2	µA	
			T_A = 70°C		0.6		
					1.5		1
Chip disable to data retention	t_{CDR}			0		ns	
Recovery time	t_{RDR}			t_{RC}		ns	2

NOTE:
1. CE_2 should be ≥ V_{CCDR} - 0.2 V or ≤ 0.2 V.
2. t_{RC} = Read cycle time



NOTE: To control data hold at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} to V_{CCDR} -0.2 V or 0 V to 0.2 V during the data retention.

5168S-6

Figure 3. Low Voltage Data Retention

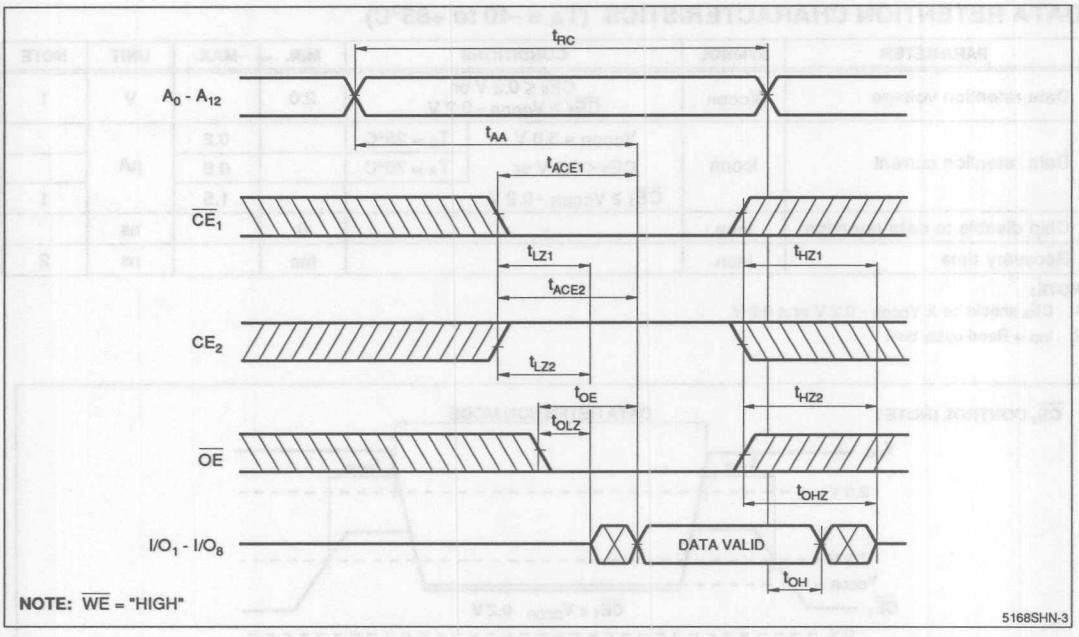
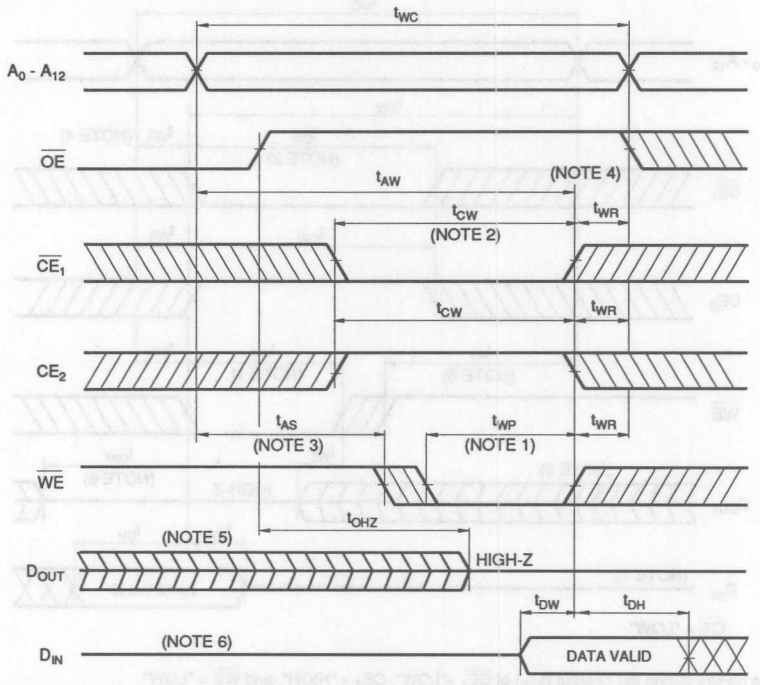


Figure 4. Read Cycle

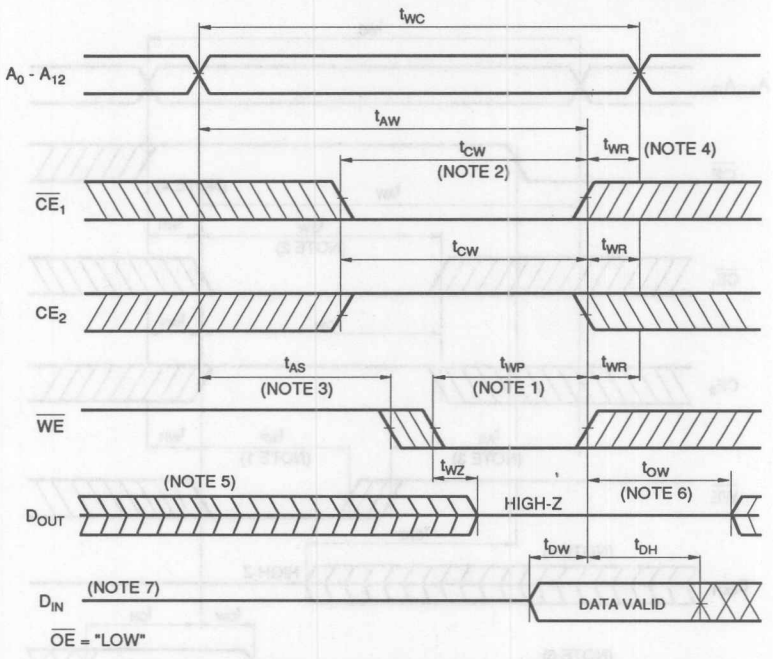


NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5168SHN-4

Figure 5. Write Cycle 1



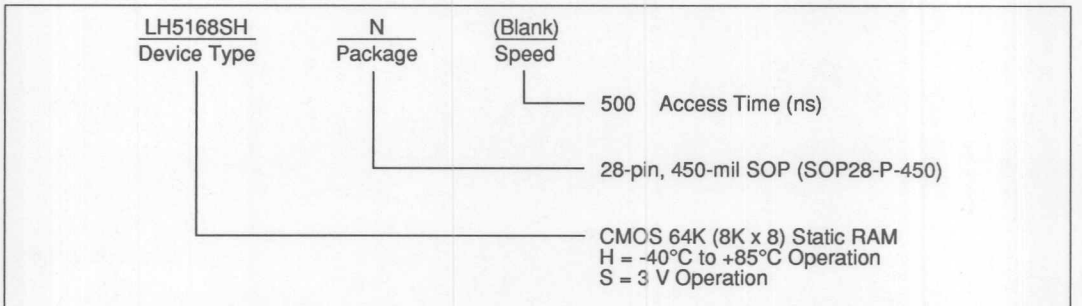
NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
7. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

5168SHN-5

Figure 6. Write Cycle 2

ORDERING INFORMATION



Example: LH5168SHN (CMOS 64K (8K x 8) Static RAM, 500 ns, 28-pin, 450-mil SOP)

5168SHN-7

LH51256L

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access times:
  100/120 ns (MAX.)
- Power consumption:
  Operating: 248 mW (MAX.)
  (T_A = -40 to 85°C, minimum cycle)
  Standby: 5.5 µW (MAX.)
  (T_A = 0 to 60°C)
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH51256L is a 256K bit static RAM organized as 32,768 × 8 bits which provides low-power standby mode. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

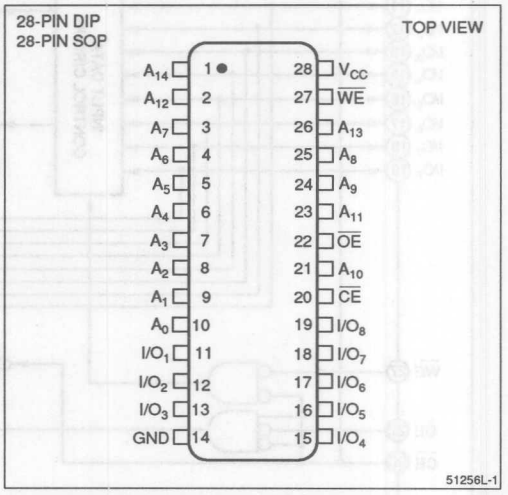


Figure 1. Pin Connections for DIP and SOP Packages

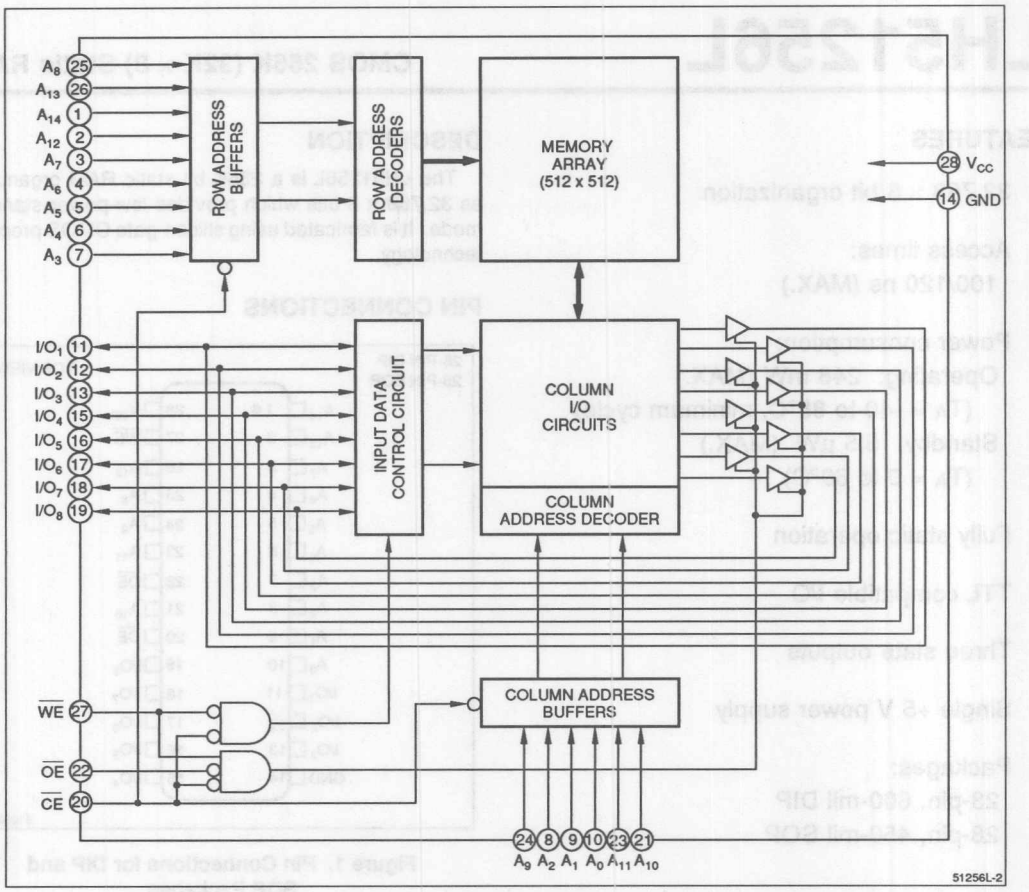


Figure 2. LH51256L Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address input
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	Non selected	High-Z	Standby (I_{SB})	1
L	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	$\|I_{LI}\|$	V_{CC} = 5.5 V V_{IN} = 0 to V_{CC}			1	µA
Output leakage current	$\|I_{LO}\|$	$\overline{CE}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}			1	µA
Operating current	I_{CC}	$\overline{CE}$ = V_{IL}, Outputs open			45	mA
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			10	mA
	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V T_A = 0 to +60°C			1	µA
		$\overline{CE}$ ≥ V_{CC} - 0.2 V T_A = -40 to +85°C			5	µA
Output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH51256/N-10L		LH51256/N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		ns	
Address access time	t_{AA}		100		120	ns	
Chip enable access time	t_{ACE}		100		120	ns	
Output enable access time	t_{OE}		50		60	ns	
Output hold time	t_{OH}	5		5		ns	
$\overline{CE}$ Low to output in Low-Z	t_{LZ}	5		5		ns	1
$\overline{OE}$ Low to output in Low-Z	t_{OLZ}	5		5		ns	1
$\overline{CE}$ High to output in High-Z	t_{HZ}	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	0	30	ns	1

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH51256/N-10L		LH51256/N-12L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		ns	
$\overline{CE}$ Low to end of write	t_{CW}	90		100		ns	
Address valid to end of write	t_{AW}	90		100		ns	
Address setup time	t_{AS}	5		5		ns	
Write recovery time	t_{WR}	15		15		ns	
Write pulse width	t_{WP}	50		50		ns	
Input data setup time	t_{DW}	30		30		ns	
Input data hold time	t_{DH}	10		10		ns	
$\overline{WE}$ High to output in High-Z	t_{OW}	0		0		ns	1
$\overline{WE}$ Low to output in High-Z	t_{WZ}	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	0	30	ns	1

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + C_L = 100 pF (Includes scope and jig capacitance)

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 TO +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V	2.0			V	
Data retention current	I_{CCDR}	V_{CCDR} = 3.0 V, $\overline{CE} \geq V_{CCDR}$ - 0.2 V, T_A = 0 to +60°C, V_{IN} = 0 to V_{CCDR}			0.6	µA	
		V_{CCDR} = 3.0 V $\overline{CE} \geq V_{CCDR}$ - 0.2 V, T_A = -40 to +85°C, V_{IN} = 0 to V_{CCDR}			3.0	µA	
$\overline{CE}$ setup time	t_{CDR}		0			ns	
$\overline{CE}$ hold time	t_{RDR}		t_{RC}			ns	1

NOTE:
1. t_{RC} = Read cycle time

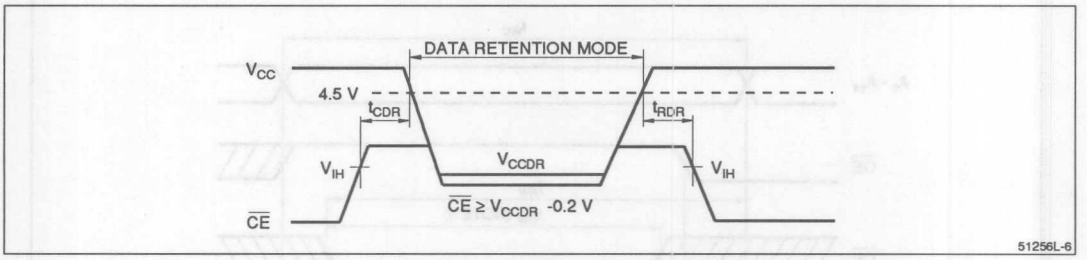


Figure 3. Data Retention Characteristics

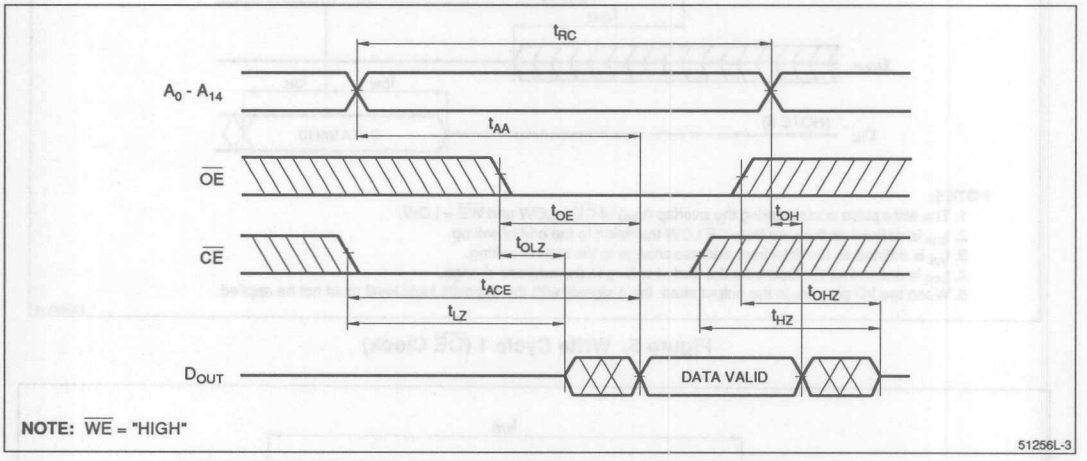
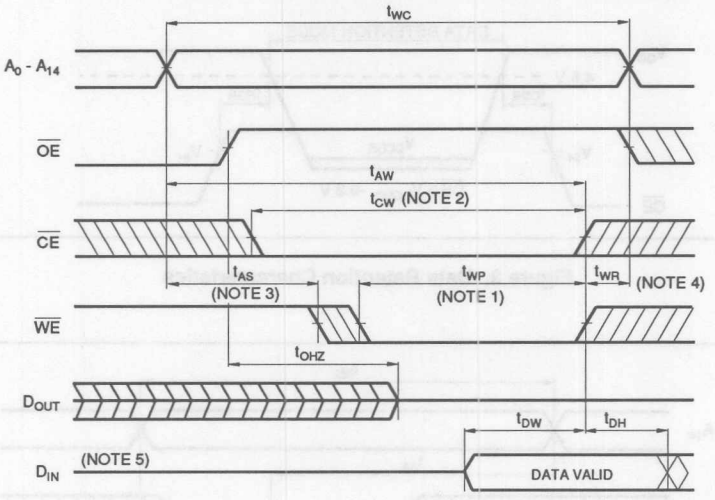


Figure 4. Read Cycle



NOTES:
1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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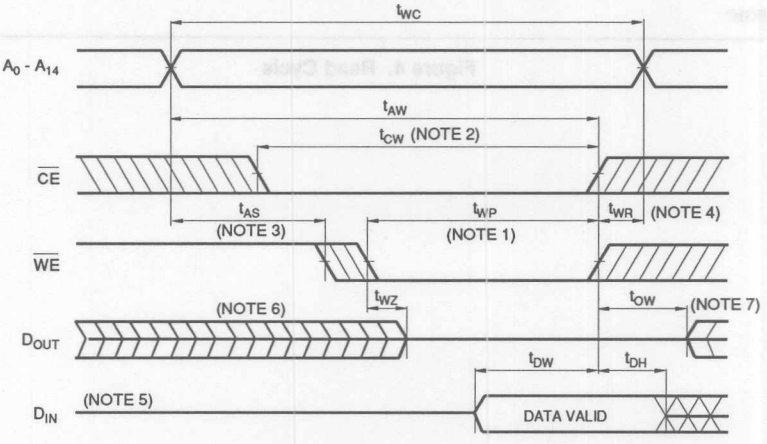
Figure 5. Write Cycle 1 ($\overline{OE}$ Clock)



NOTES:
1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{CW} is defined as the time from $\overline{CE}$ LOW transition to the end of writing.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
7. If $\overline{CE}$ HIGH transition occurs at the same time or prior to the $\overline{WE}$ HIGH transition, the output will remain high-impedance.

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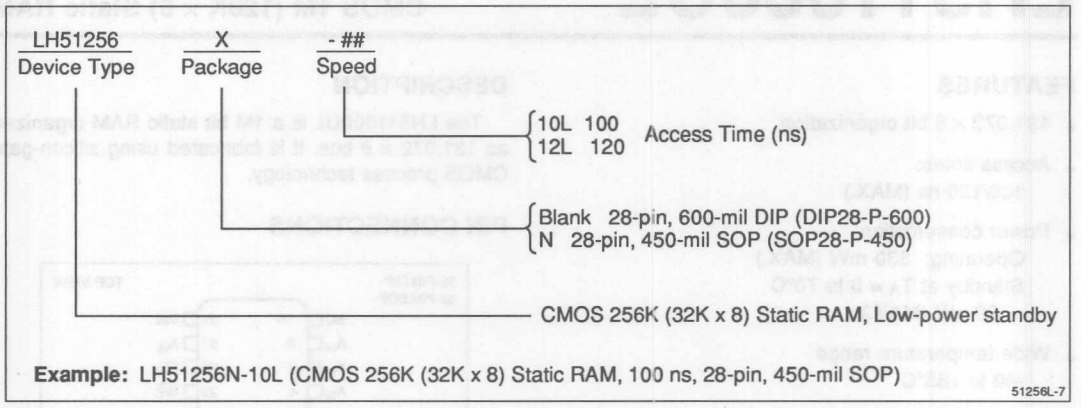
Figure 6. Write Cycle 2 ($\overline{OE}$ Low)

ORDERING INFORMATION



LH511000UL

PRELIMINARY

CMOS 1M (128K × 8) Static RAM

FEATURES

- 131,072 × 8 bit organization
- Access times:
  100/120 ns (MAX.)
- Power consumption:
  Operating: 330 mW (MAX.)
  Standby at T_A = 0 to 70°C
  22 µW (MAX.)
- Wide temperature range
  -40 to +85°C
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  32-pin, 8 × 20 mm^2 TSOP (Type I)
  (normal and reverse bend pins)

DESCRIPTION

The LH511000UL is a 1M bit static RAM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

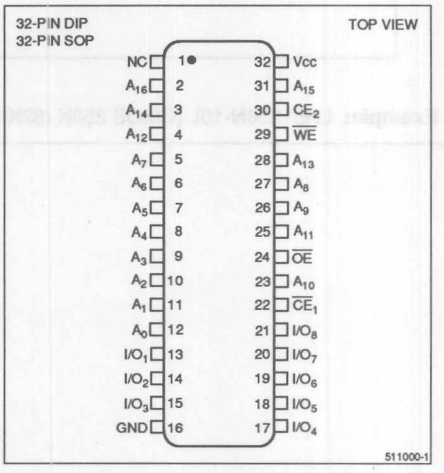


Figure 1. Pin Connections for DIP and SOP Packages

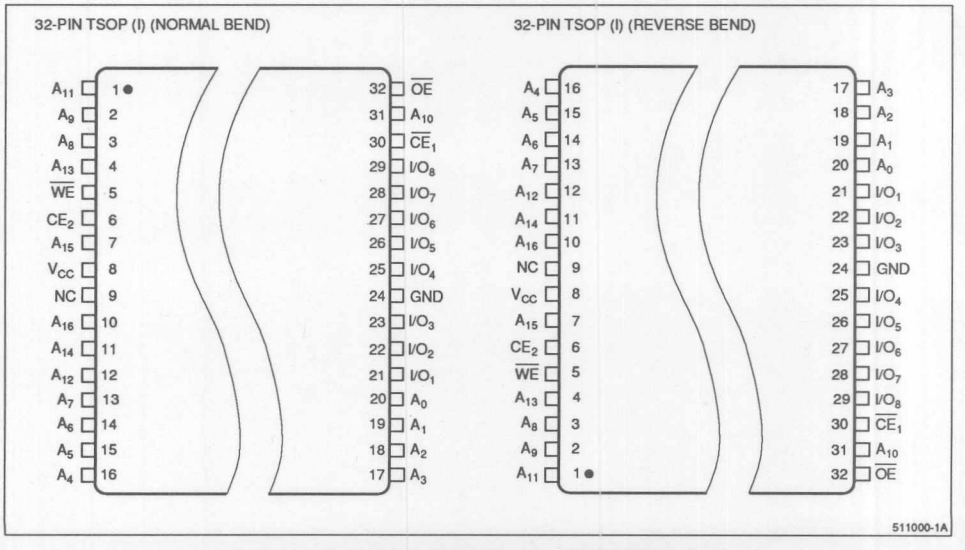


Figure 2. Pin Connections for TSOP Packages

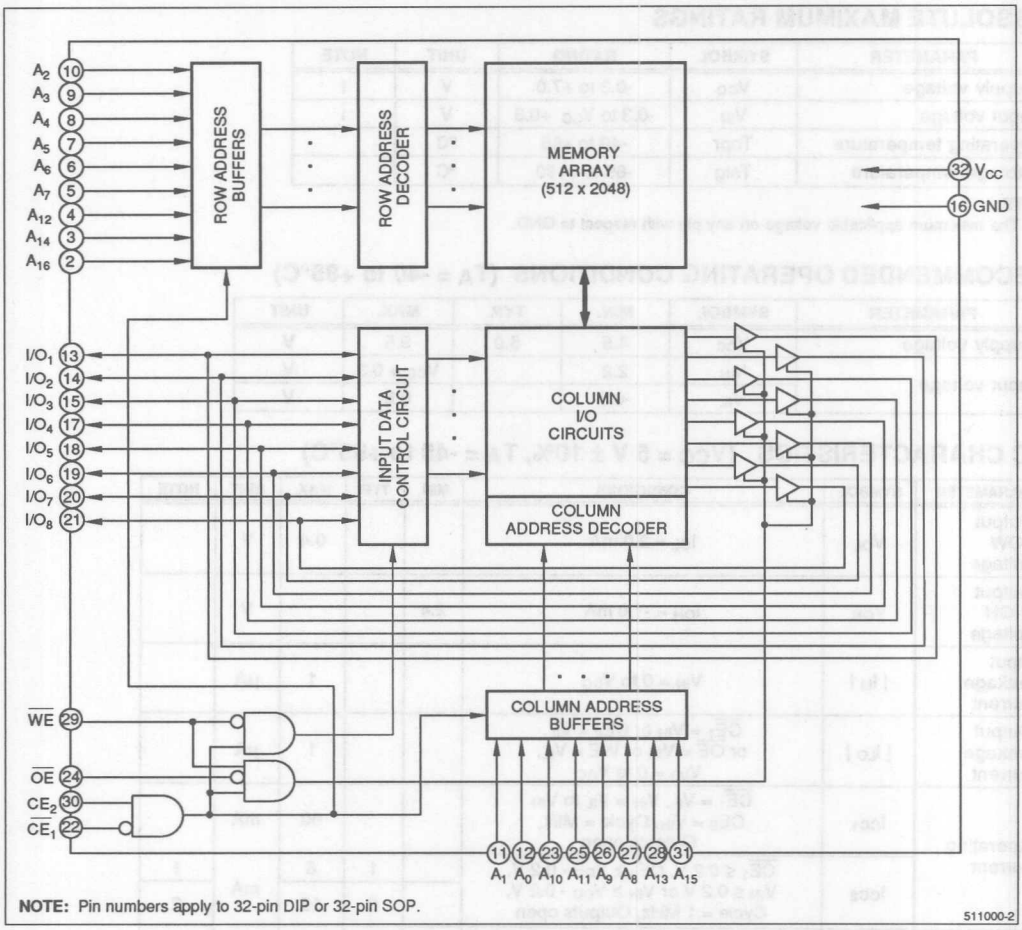


Figure 3. LH511000UL Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
$\overline{CE_1}$ - CE_2	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data Input/Output
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	STANDBY CURRENT	NOTE
H	X	X	X	Non selected	High-Z	Standby (I_{SB}, I_{SB1})	1
X	L	X	X	Non selected	High-Z	Standby (I_{SB}, I_{SB1})	1
L	H	L	X	Write	D_{IN}	Operating (I_{CC})	1
L	H	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	H	Output disable	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-65 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} + 0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Output LOW voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output HIGH voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 to V_{CC}			1	µA	
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}, or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}, $V_{I/O}$ = 0 to V_{CC}			1	µA	
Operating current	I_{CC1}	$\overline{CE_1}$ = V_{IL}, V_{IN} = V_{IL} to V_{IH} CE_2 = V_{IH}, Cycle = MIN. Outputs open			60	mA	
	I_{CC2}	$\overline{CE_1}$ ≤ 0.2 V, CE_2 ≥ V_{CC} - 0.2 V, V_{IN} ≤ 0.2 V or V_{IN} ≥ V_{CC} - 0.2 V, Cycle = 1 MHz, Outputs open		1	6	mA	1
				5	15		2
Standby current	I_{SB1}	CE_2, $\overline{CE_1}$ = V_{IH} or CE_2 = V_{IL}			3	mA	
	I_{SB}	CE_2 ≤ 0.2 V or $\overline{CE_1}$, CE_2 ≥ V_{CC} - 0.2 V			4	µA	3
					12		4

NOTES:
1. Read cycle
2. Write cycle
3. T_A = 0 to 70°C
4. T_A = -40 to +85°C

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	100 ns		120 ns		UNIT
		MIN.	MAX.	MIN.	MAX.	
Read cycle time	t_{RC}	100		120		ns
Address access time	t_{AA}		100		120	ns
Chip enable access time	t_{ACE1}		100		120	ns
	t_{ACE2}		100		120	ns
Output enable time	t_{OE}		50		60	ns
Output hold time	t_{OH}	10		10		ns
$\overline{CE}$ Low to output in Low-Z	t_{LZ1}	5		5		ns
	t_{LZ2}	5		5		ns
$\overline{OE}$ Low to output in Low-Z	t_{OLZ}	5		5		ns
$\overline{CE}$ High to output in High-Z	t_{HZ1}	0	35	0	45	ns
	t_{HZ2}	0	35	0	45	ns
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	35	0	45	ns

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH511000/N-10UL		LH511000/N-12UL		UNIT
		MIN.	MAX.	MIN.	MAX.	
Write cycle time	t_{WC}	100		120		ns
$\overline{CE}$ Low to end of write	t_{CW}	80		100		ns
Address valid to end of write	t_{AW}	80		100		ns
Address setup time	t_{AS}	0		0		ns
Write recovery time	t_{WR}	0		0		ns
Write pulse width	t_{WP}	75		85		ns
Input data setup time	t_{DW}	40		50		ns
Input data hold time	t_{DH}	0		0		ns
$\overline{WE}$ High to output in High-Z	t_{OW}	0		0		ns
$\overline{WE}$ Low to output in High-Z	t_{WZ}	5		5		ns
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	35	0	45	ns

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + 100 pF (Includes scope and jig capacitance)

CAPACITANCE (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input capacitance	C_{IN}	V_{IN} = 0 V			10	pF	1
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF	1

NOTE:
1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$CE_2 \le 0.2$ V or $\overline{CE_1}$, $CE_2 \ge V_{CC}$ - 0.2 V		2.0			V	
	I_{CCDR}	$CE_2 \le 0.2$ V, V_{CC} = 2 V or $\overline{CE_1}$, $CE_2 \ge V_{CC}$ - 0.2 V V_{CC} = 3 V	25°C			0.1	µA	
			0 to 70°C			2	µA	
			-40 to 85°C			6	µA	
$\overline{CE}$ setup time	t_{CDR}			0			ns	
$\overline{CE}$ hold time	t_R			t_{RC}			ns	1

NOTE:
1. t_{RC} = Read cycle time

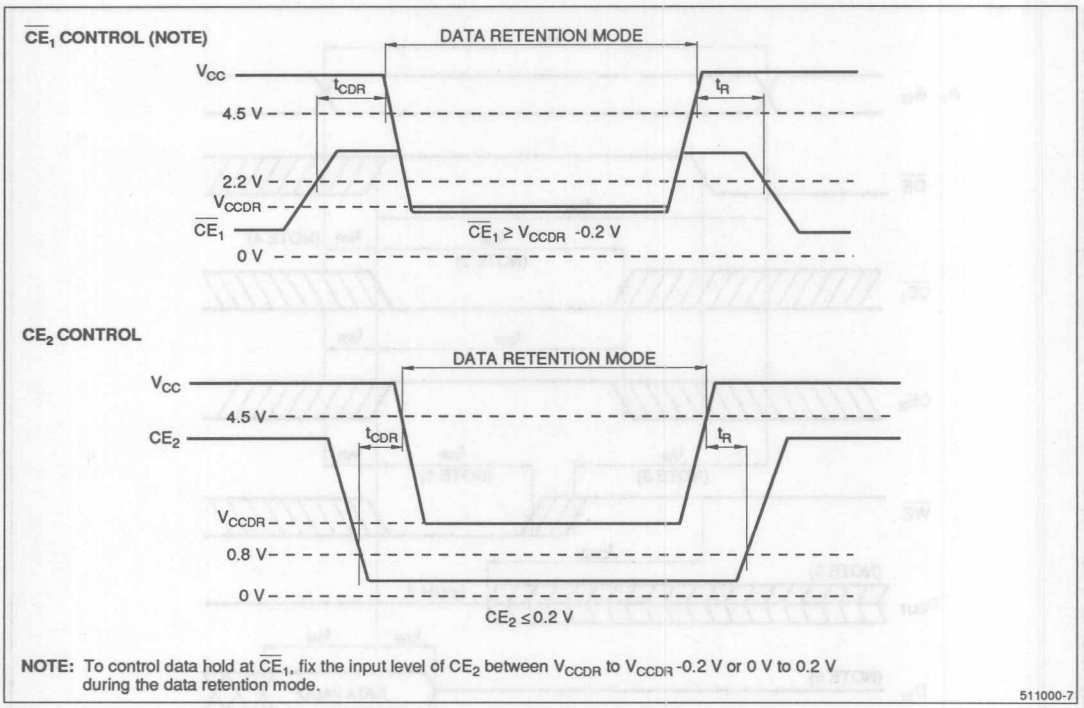


Figure 4. Low Voltage Data Retention

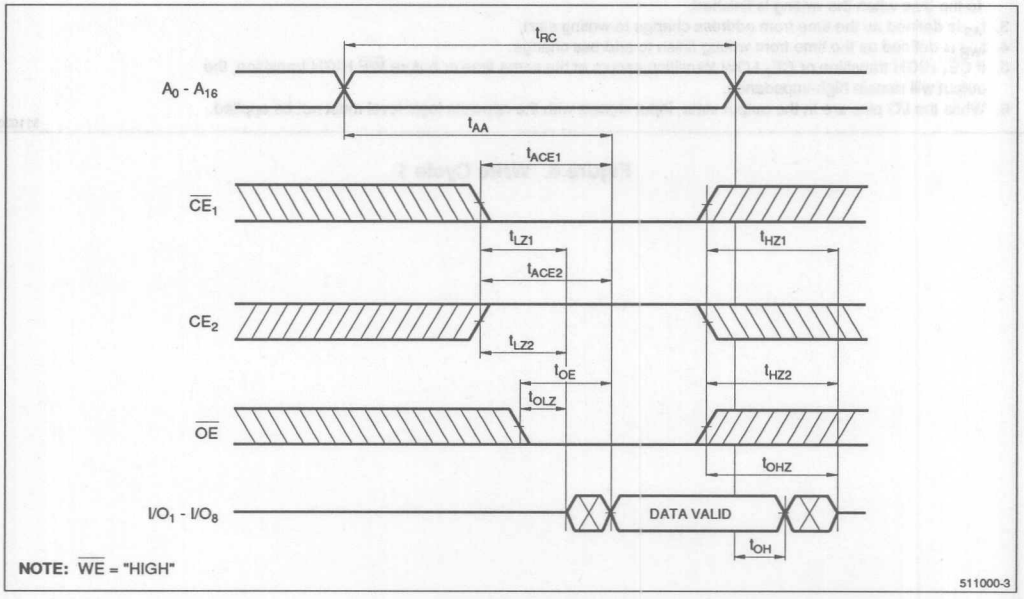
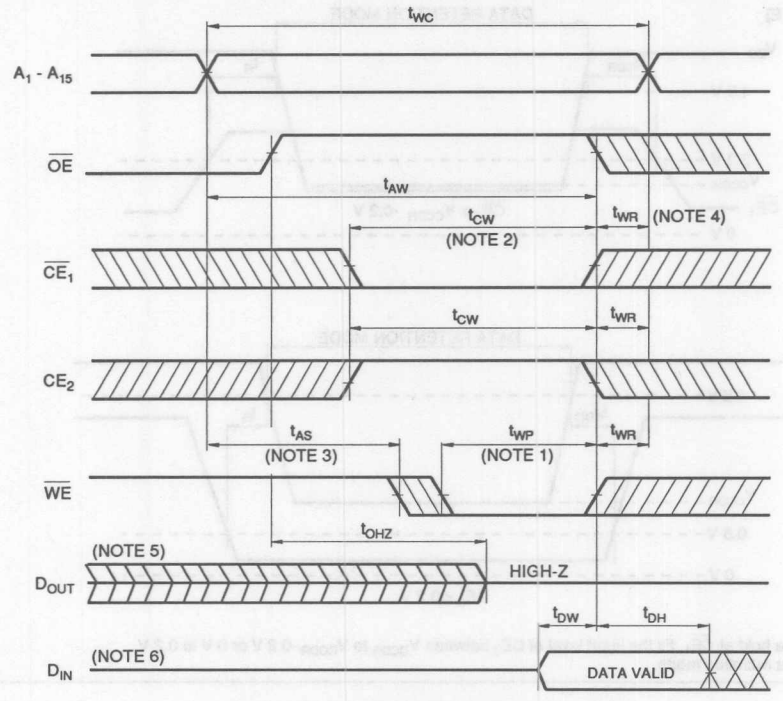


Figure 5. Read Cycle

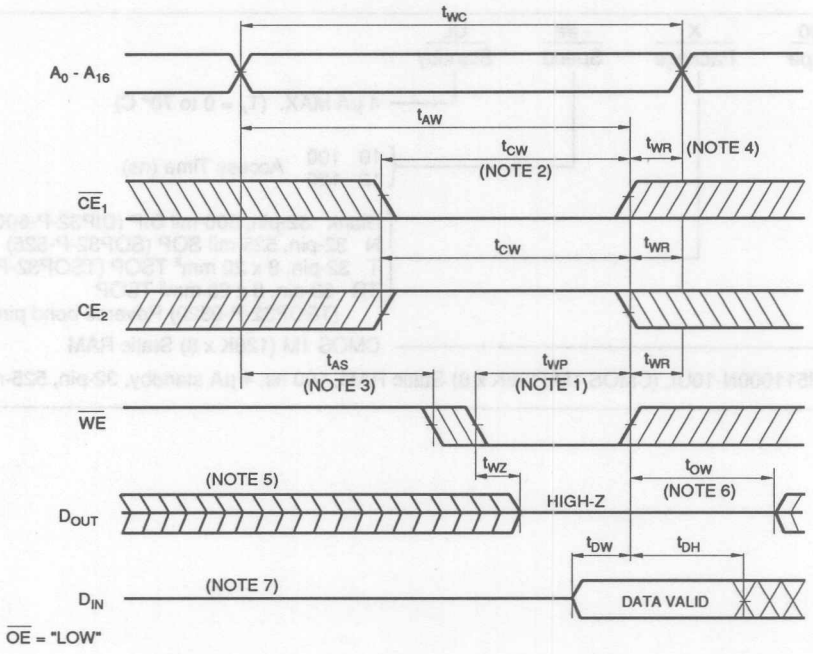


NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
6. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

511000-4

Figure 6. Write Cycle 1



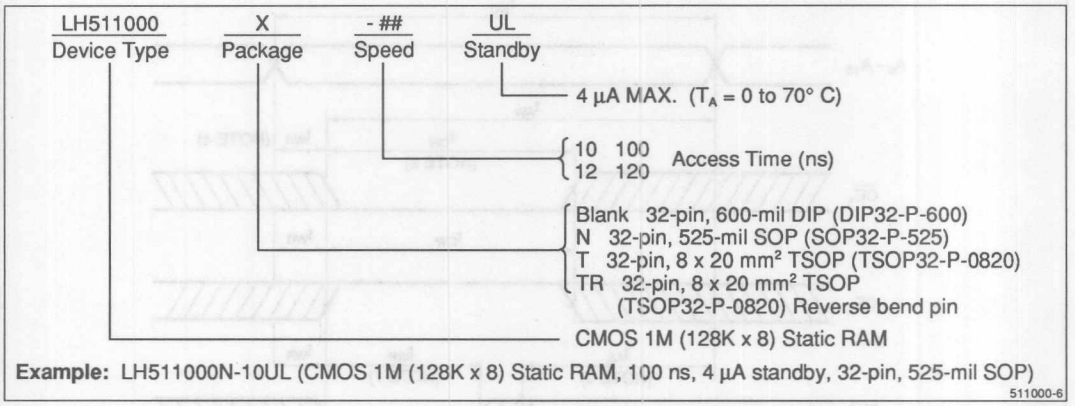
NOTES:

1. The writing occurs during the overlap (t_{WP}) of $\overline{CE_1}$ ="LOW", CE_2 = "HIGH", and $\overline{WE}$ = "LOW".
2. t_{CW} is defined as the time from the last occuring transition, either $\overline{CE_1}$ LOW transition or CE_2 HIGH transition, to the time when the writing is finished.
3. t_{AS} is defined as the time from address change to writing start.
4. t_{WR} is defined as the time from writing finish to address change.
5. If $\overline{CE_1}$ LOW transition or CE_2 HIGH transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE_1}$ HIGH transition or CE_2 LOW transition occurs at the same time or before $\overline{WE}$ HIGH transition, the output will remain high-impedance.
7. While the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

511000-5

Figure 7. Write Cycle 2

ORDERING INFORMATION



Example: LH511000N-10UL (CMOS 1M (128K x 8) Static RAM, 100 ns, 4 µA standby, 32-pin, 525-mil SOP)

511000-6

LH52250AL

CMOS 32K × 8 Static RAM

FEATURES

- Access Times: 70/100 ns
- Automatic Power Down During Long Read Cycles
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 600-mil DIP
  28-Pin, 450-mil SOP

FUNCTIONAL DESCRIPTION

The LH52250AL is a high-density 262,144 bit static RAM organized as 32K×8. An efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address. An Automatic Power Down feature decreases current consumption when Read cycles extend beyond their minimum cycle time.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

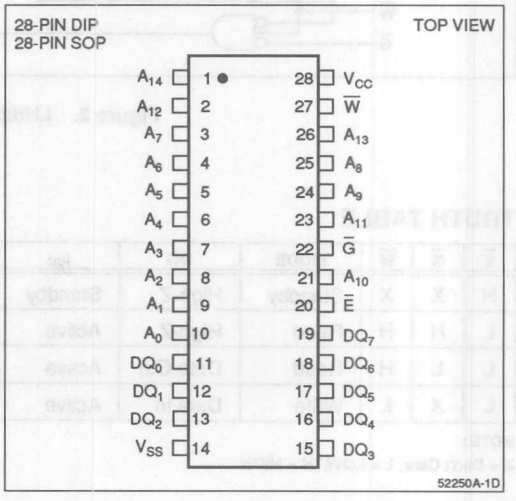


Figure 1. Pin Connections for DIP and SOP Packages

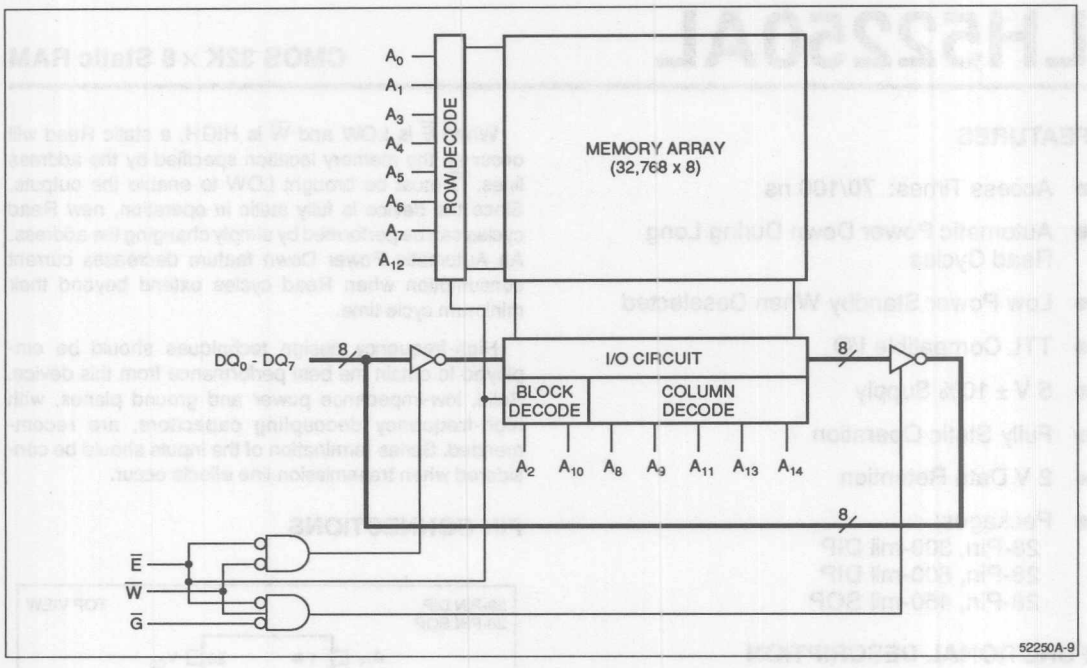


Figure 2. LH52250AL Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Standby	High-Z	Standby
L	H	H	Read	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
Vcc	Positive Power Supply
Vss	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{RC} = 70 ns			80	mA
I_{CC1}	Operating Current [1]	t_{RC} = 100 ns			70	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V			0.1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$			3	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−1		1	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−1		1	µA
V_{OH}	Output High Voltage	I_{OH} = −1.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	VCC = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V		6	50	µA

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	0.6 to 2.4 V
Input Rise and Fall Times	10 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

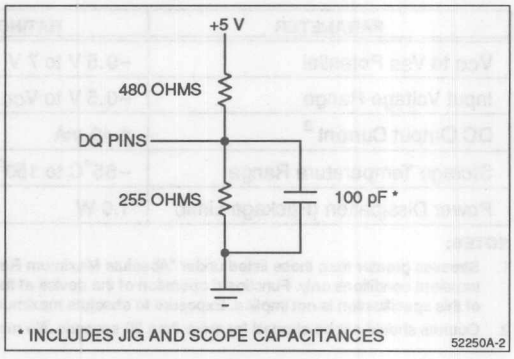


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_{DQ} (I/O Capacitance)	10 pF

NOTE:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are "Don't Care."

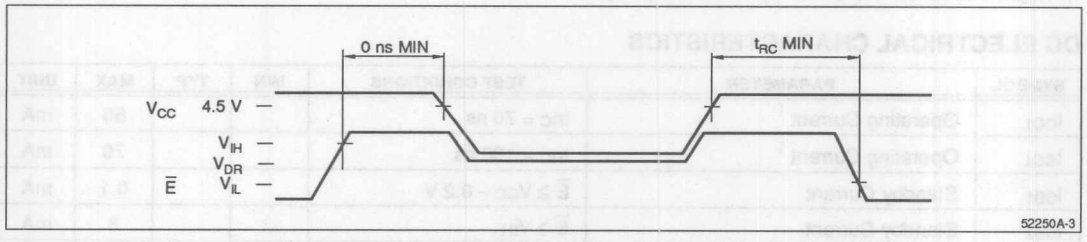


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-70		-10		UNITS
		MIN	MAX	MIN	MAX	
	READ CYCLE					
t_{RC}	Read Cycle Time	70		100		ns
t_{AA}	Address Access Time		70		100	ns
t_{OH}	Output Hold from Address Change	10		10		ns
t_{EA}	$\overline{E}$ Low to Valid Data		70		100	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	5		5		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]	0	35	0	45	ns
t_{GA}	$\overline{G}$ Low to Valid Data		40		60	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	5		5		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	35	0	45	ns
	WRITE CYCLE					
t_{WC}	Write Cycle Time	70		100		ns
t_{EW}	$\overline{E}$ Low to End of Write	45		65		ns
t_{AW}	Address Valid to End of Write	65		90		ns
t_{AS}	Address Setup	0		0		ns
t_{WR}	Address Hold from End of Write	0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	45		65		ns
t_{DW}	Input Data Setup Time	30		35		ns
t_{DH}	Input Data Hold Time	0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]	0	40	0	45	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	5		5		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load.
3. Sample tested only.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read Cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid Data will be present following t_{GA} only if t_{EA} timing is met.

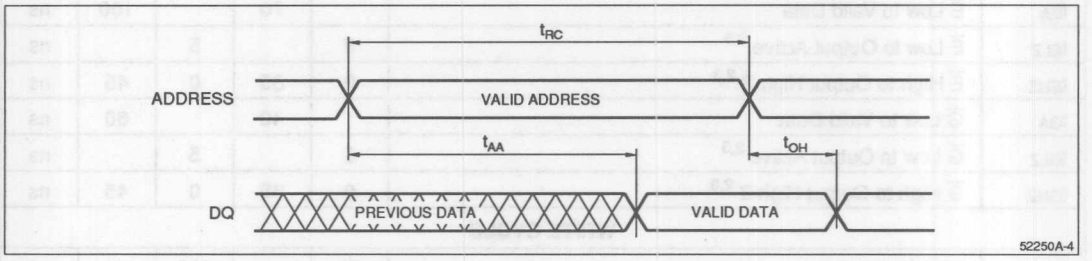


Figure 5. Read Cycle No. 1

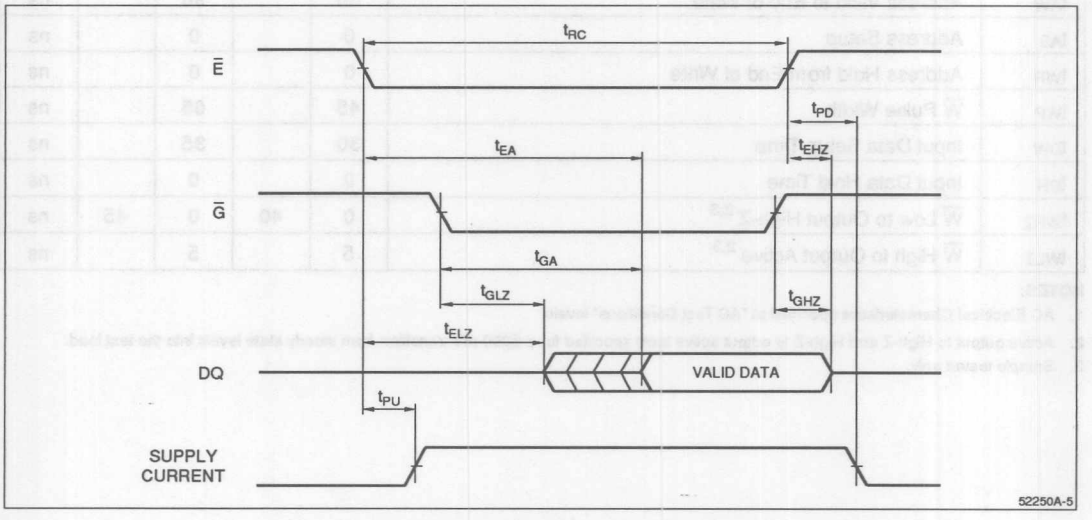


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write Cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH52250A/LH52250AL's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write Cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

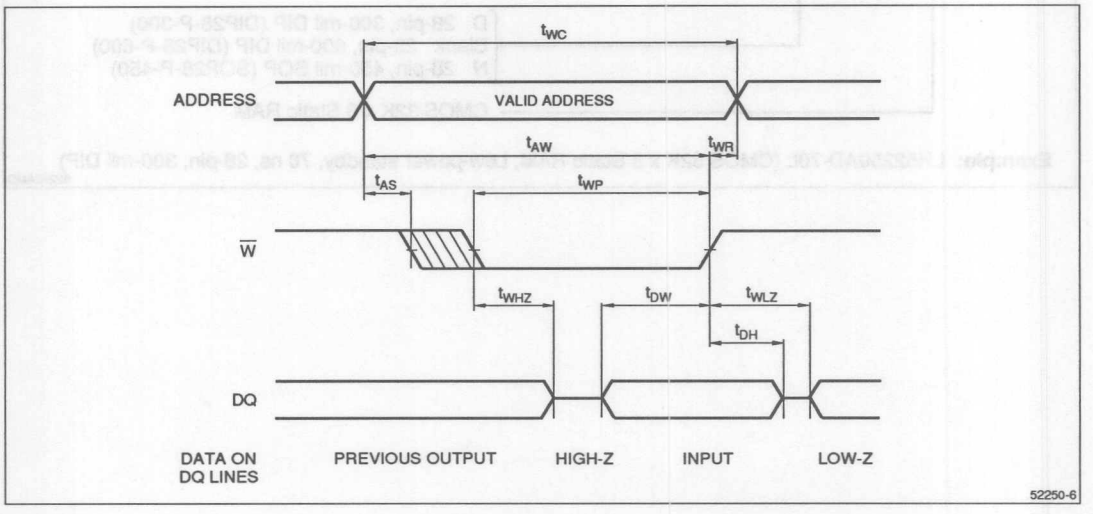


Figure 7. Write Cycle No. 1

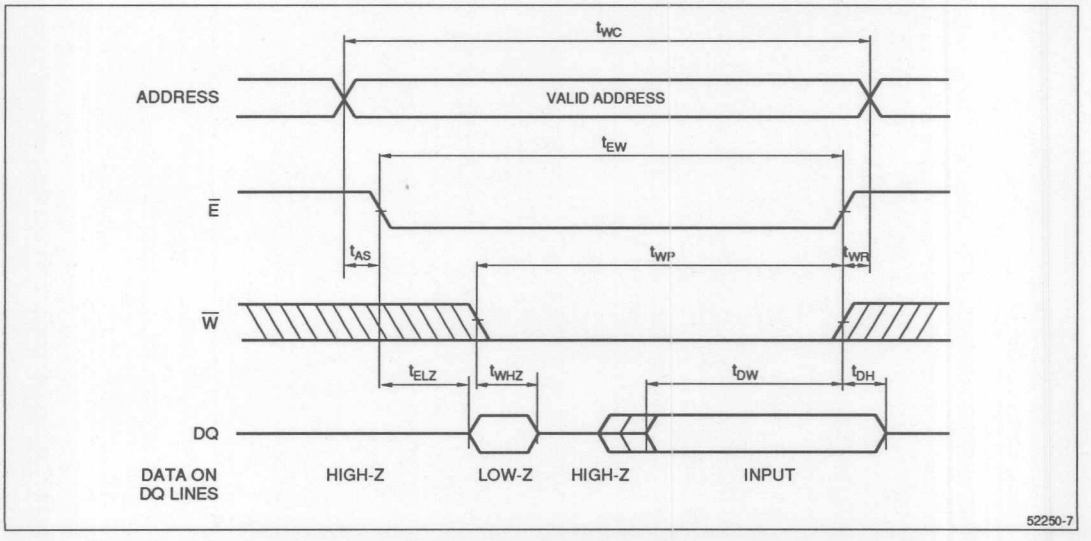
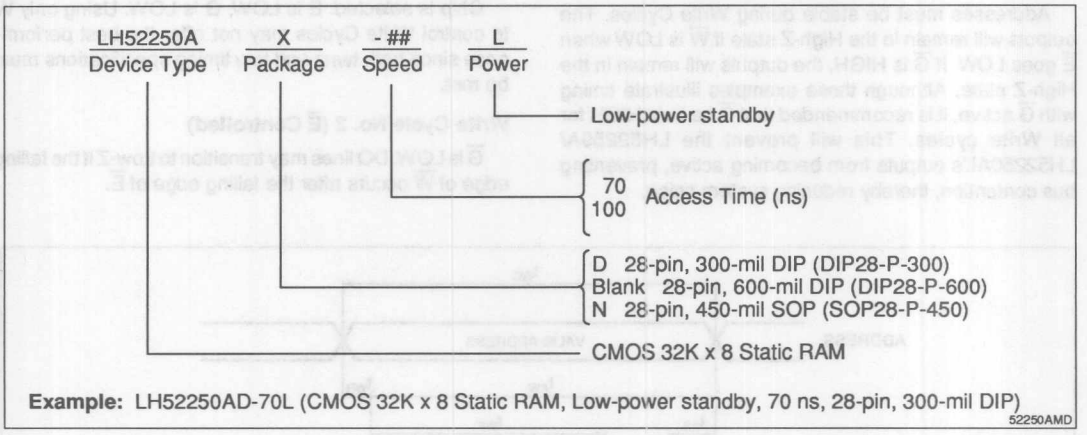


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH52256LL

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access time:
  90 ns (MAX.)
- Low power consumption:
  Operating: 385 mW (MAX.)
  Standby: 220 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH52256LL is an ultra-low power CMOS-periphery static RAM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

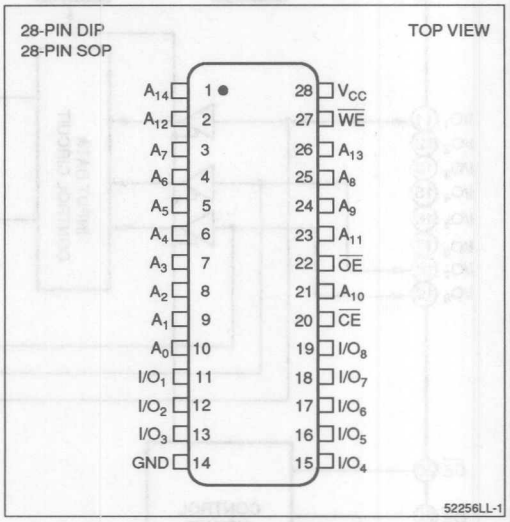


Figure 1. Pin Connections for DIP and SOP Packages

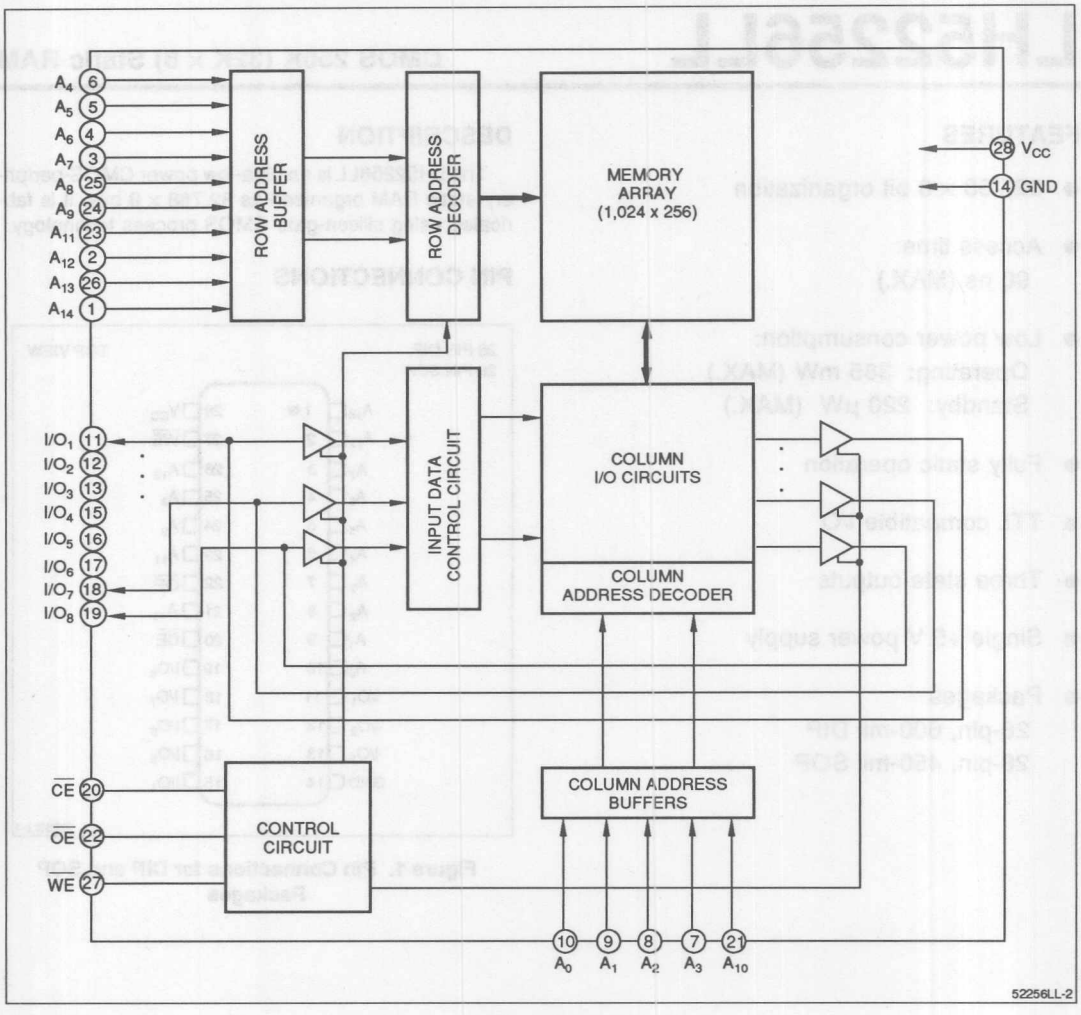


Figure 2. LH52256LL Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address inputs
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data inputs and outputs
V_{CC}	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	SUPPLY CURRENT	NOTE
H	X	X	Deselect	High-Z	Standby (I_{SB})	1
L	H	L	Read	D_{OUT}	Operating (I_{CC})	
L	H	H	Output disable	High-Z	Operating (I_{CC})	
L	L	X	Write	D_{IN}	Operating (I_{CC})	1

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2	3.5	V_{CC} + 0.3	V
	V_{IL}	-0.3		+0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5 V_{IN} = 0 to V_{CC}			1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ = V_{IH} or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}			1	µA
Operating current	I_{CC}	$\overline{CE}$ = V_{IL}, Outputs open			70	mA
	I_{CC1}	V_{IH} = 3.5 V, V_{IL} = 0.6 V Outputs open			65	mA
	I_{CC2}	V_{IH} = 2.2 V, V_{IL} = 0.8 V Outputs open			70	mA
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA
	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V		2	40	µA
Output voltage	V_{OL}	I_{OL} = 2 mA			0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	90		ns	
Address access time	t_{AA}		90	ns	
Chip enable access time	t_{ACE}		90	ns	
Output enable access time	t_{OE}		50	ns	
Output hold from address change	t_{OH}	10		ns	
Chip enable Low to output in Low-Z	t_{LZ}	5		ns	1
Output enable Low to output in Low-Z	t_{OLZ}	5		ns	1
Chip disable to output in High-Z	t_{HZ}	0	40	ns	1
Output enable High to output in High-Z	t_{OHZ}	0	40	ns	1

(2) WRITE CYCLE (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Write cycle time	t_{WC}	90		ns	
Chip enable to end of write	t_{CW}	55		ns	
Address valid to end of write	t_{AW}	80		ns	
Address setup time	t_{AS}	0		ns	
Write pulse width	t_{WP}	55		ns	
Write recovery time	t_{WR}	5		ns	
Data valid to end of write	t_{DW}	30		ns	
Data hold time	t_{DH}	0		ns	
Output active from end of write	t_{OW}	5		ns	1
Write Low to output in High-Z	t_{WZ}	0	40	ns	1
Output enable High to output in High-Z	t_{OHZ}	0	40	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6 to 2.4 V
Input rise/fall time	1.0 ns
Timing reference level	1.5 V
Output load conditions	1TTL gate, C_L = 100 pF (Includes scope and jig capacitance)

DATA RETENTION CHARACTERISTICS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS		MIN.	TYP.	MAX.	UNIT
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V		2.0			V
Data retention current	I_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2 V, V_{CCDR} = 3.0 V	T_A = 25°C			1	µA
			T_A = 0 to 40°C			3	
			T_A = 0 to 70°C			20	
Chip disable to data retention	t_{CDR}			0			ns
Recovery time	t_R			t_{RC}*			ns

* t_{RC} = Read cycle time

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V		8	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V		10	pF

NOTE:
1. This parameter is sampled and not production tested.

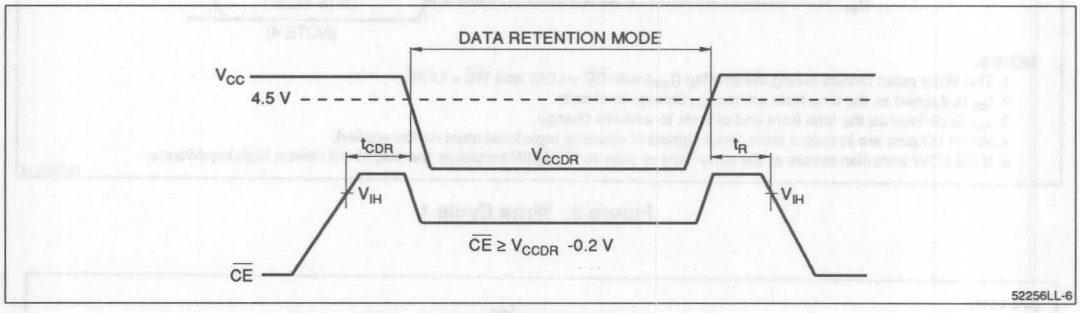


Figure 3. Low Voltage Data Retention

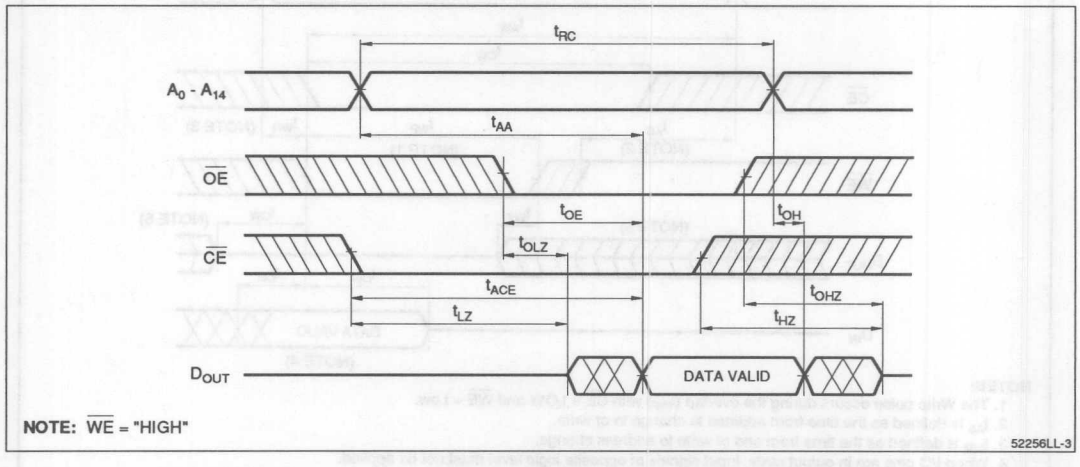
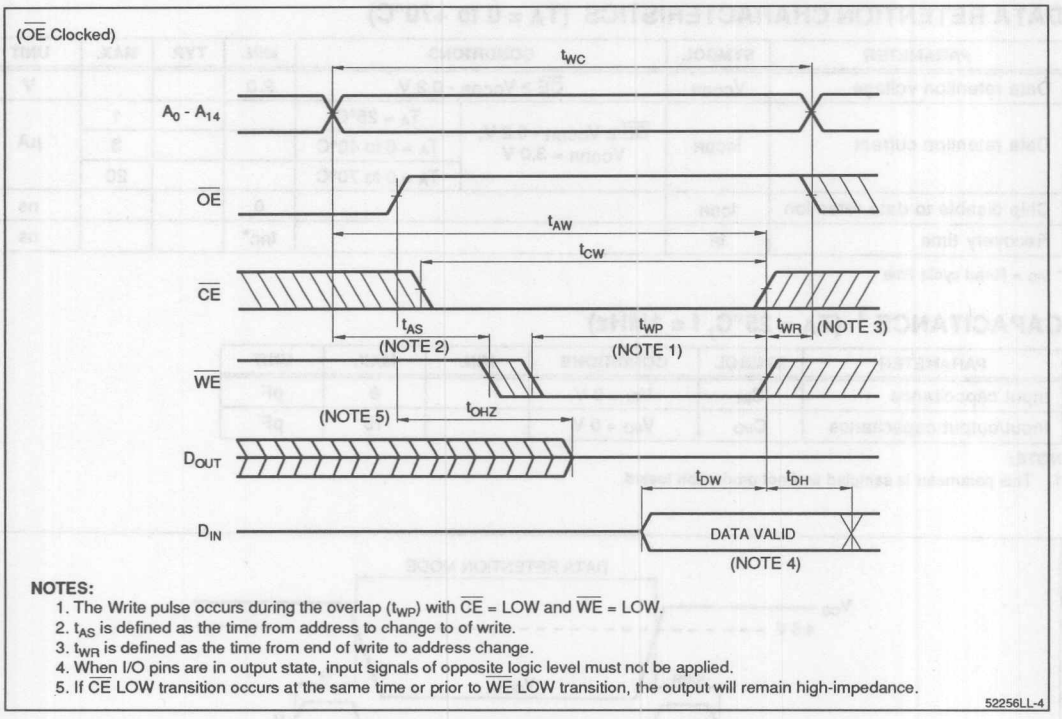


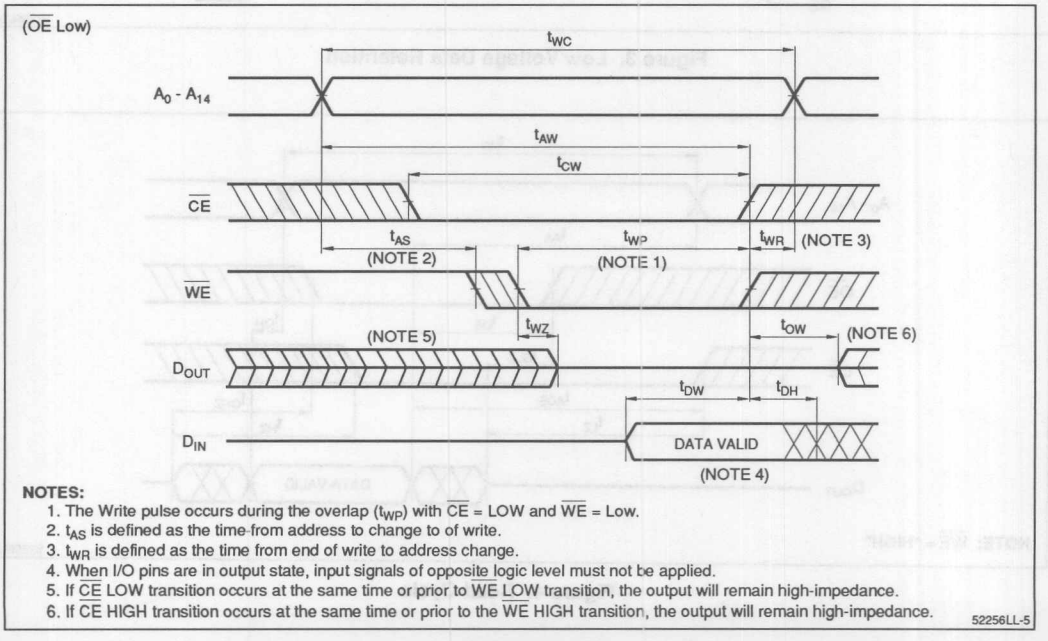
Figure 4. Read Cycle



NOTES:
1. The Write pulse occurs during the overlap (t_{WP}) with $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{AS} is defined as the time from address to change to of write.
3. t_{WR} is defined as the time from end of write to address change.
4. When I/O pins are in output state, input signals of opposite logic level must not be applied.
5. If $\overline{CE}$ LOW transition occurs at the same time or prior to $\overline{WE}$ LOW transition, the output will remain high-impedance.

52256LL-4

Figure 5. Write Cycle 1

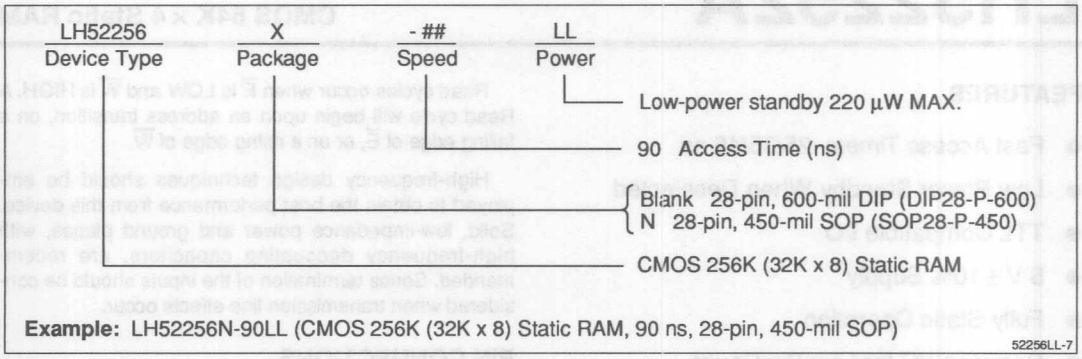


NOTES:
1. The Write pulse occurs during the overlap (t_{WP}) with $\overline{CE}$ = LOW and $\overline{WE}$ = Low.
2. t_{AS} is defined as the time from address to change to of write.
3. t_{WR} is defined as the time from end of write to address change.
4. When I/O pins are in output state, input signals of opposite logic level must not be applied.
5. If $\overline{CE}$ LOW transition occurs at the same time or prior to $\overline{WE}$ LOW transition, the output will remain high-impedance.
6. If $\overline{CE}$ HIGH transition occurs at the same time or prior to the $\overline{WE}$ HIGH transition, the output will remain high-impedance.

52256LL-5

Figure 6. Write Cycle 2

ORDERING INFORMATION



LH52252A

CMOS 64K × 4 Static RAM

FEATURES

- Fast Access Times: 25/35/45 ns
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count
- JEDEC Standard Pinouts
- Packages:
  24-Pin, 300-mil DIP
  24-Pin, 300-mil SOJ

FUNCTIONAL DESCRIPTION

The LH52252A is a high-speed 262,144 bit static RAM organized as 64K × 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is HIGH. Standby power (I_{SB1}) drops to its lowest level when $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 16 address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

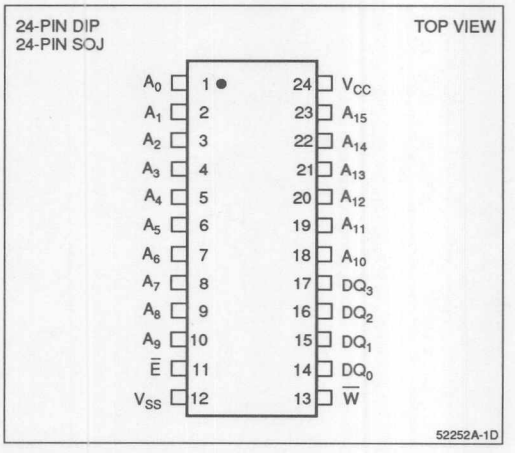


Figure 1. Pin Connections for DIP and SOJ Packages

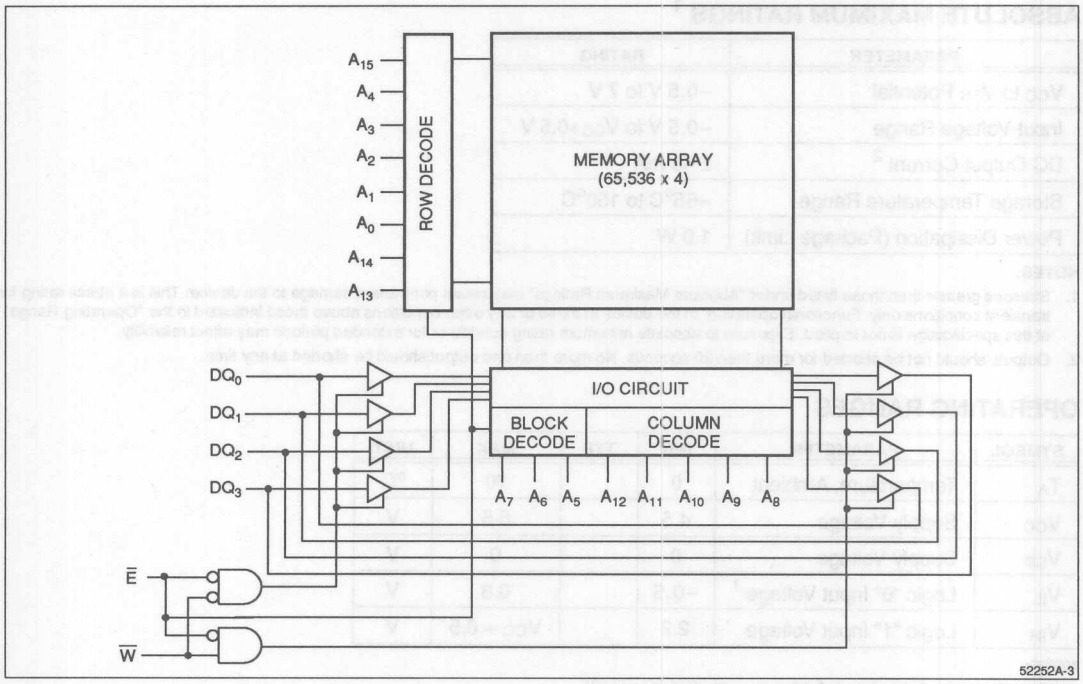


Figure 2. LH52252A Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	DQ	I_{CC}
H	X	Not Selected	High-Z	Standby
L	H	Read	Data Out	Active
L	L	Write	Data In	Active

NOTE:
X = Don't, Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{15}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC}+0.5 V
DC Output Current [2]	±40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	Outputs open, t_{RC} = 25 ns		110	150	mA
I_{CC1}	Operating Current [2]	Outputs open, t_{RC} = 35 ns		95	120	mA
I_{CC1}	Operating Current [2]	Outputs open, t_{RC} = 45 ns		85	100	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.02	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$		3	5	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTE:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

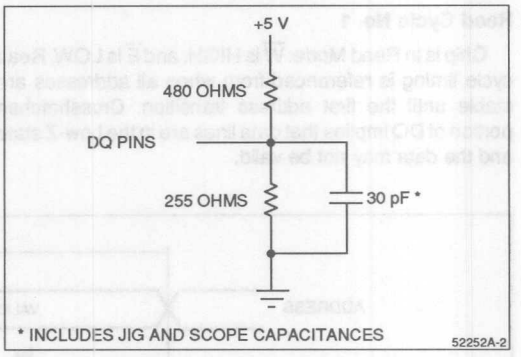


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-25		-35		-45		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
	READ CYCLE							
t_{RC}	Read Cycle Timing	25		35		45		ns
t_{AA}	Address Access Time		25		35		45	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		25		35		45	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [3]	5		5		5		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		12		15		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [4]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [4]		30		35		40	ns
	WRITE CYCLE							
t_{WC}	Write Cycle Time	25		35		45		ns
t_{EW}	$\overline{E}$ Low to End of Write	20		30		35		ns
t_{AW}	Address Valid to End of Write	20		30		35		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	20		25		35		ns
t_{DW}	Input Data Setup Time	12		15		20		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [3]	0		0		0		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load.
3. Sample tested only.
4. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid while $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Outputs will transition from High-Z to Valid Data Out.

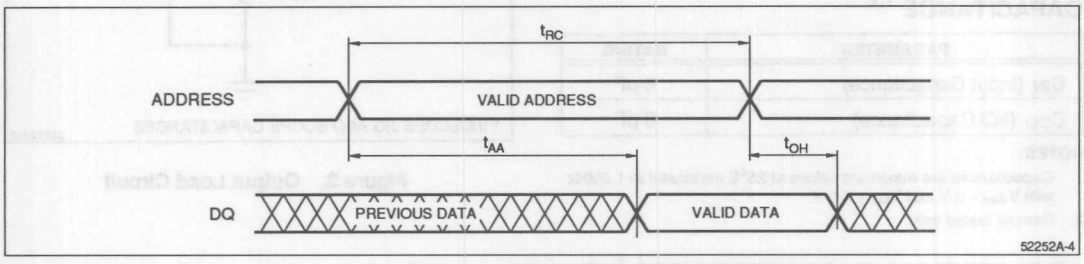


Figure 4. Read Cycle No. 1

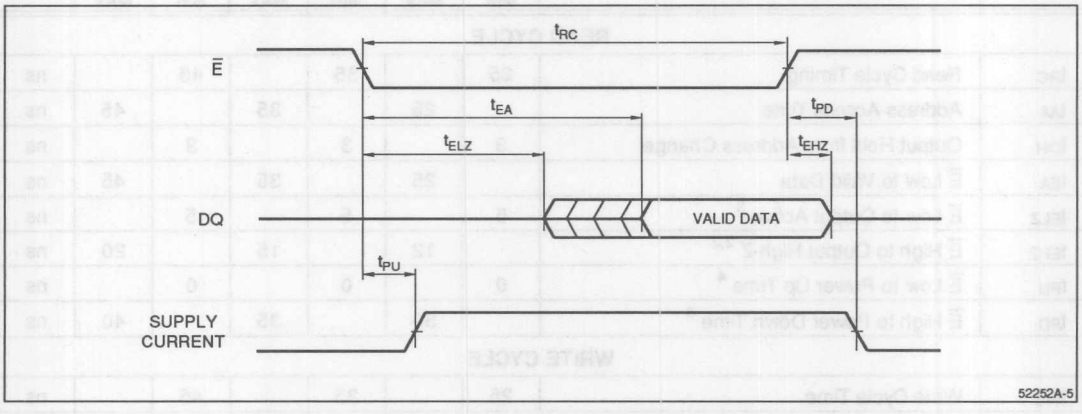


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be high during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

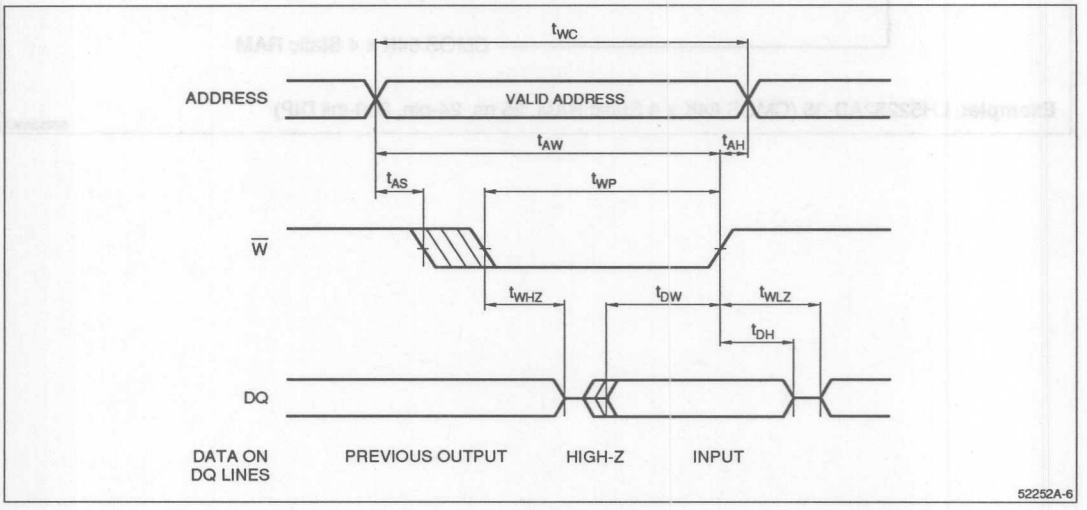


Figure 6. Write Cycle No. 1

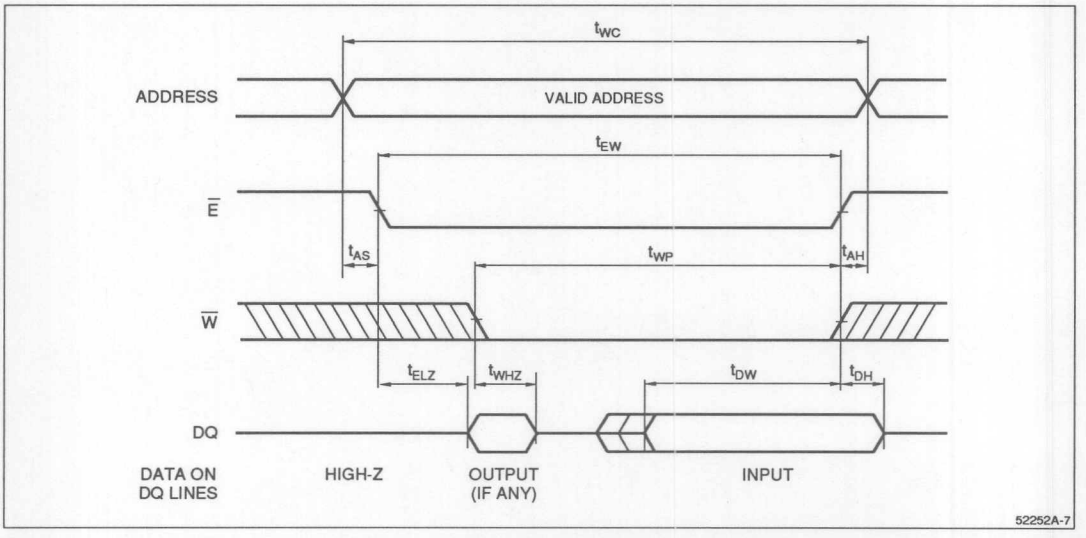
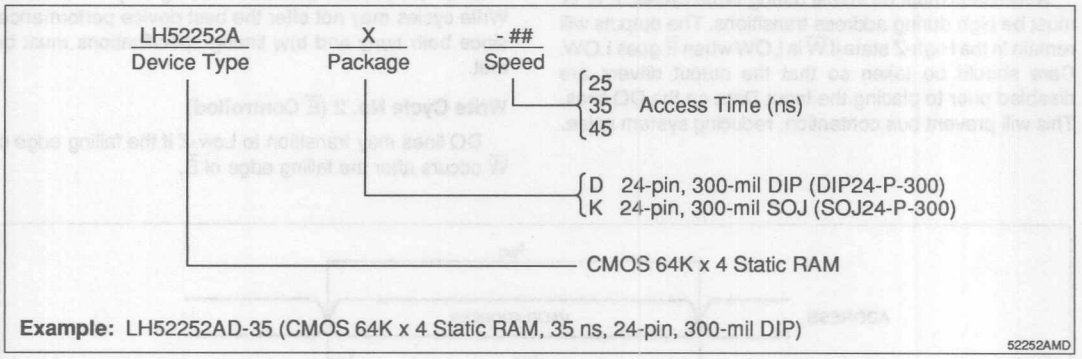


Figure 7. Write Cycle No. 2

ORDERING INFORMATION



LH52252B

ADVANCE INFORMATION

CMOS 64K × 4 Static RAM

FEATURES

- Fast Access Times: 20/25 ns
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count
- JEDEC Standard Pinouts
- Packages:
  24-Pin, 300-mil DIP
  24-Pin, 300-mil SOJ

FUNCTIONAL DESCRIPTION

The LH52252B is a high-speed 262,144 bit static RAM organized as 64K × 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is HIGH. Standby power (I_{SB1}) drops to its lowest level when $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 16 address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

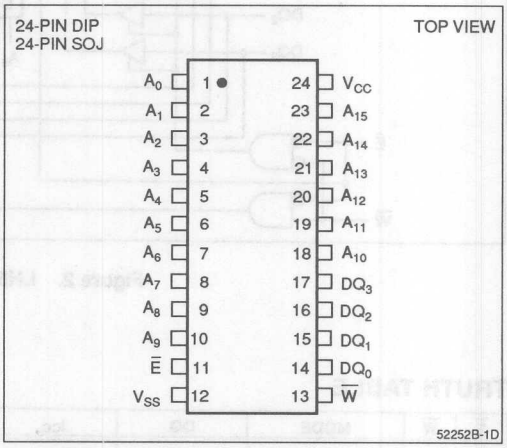


Figure 1. Pin Connections for DIP and SOJ Packages

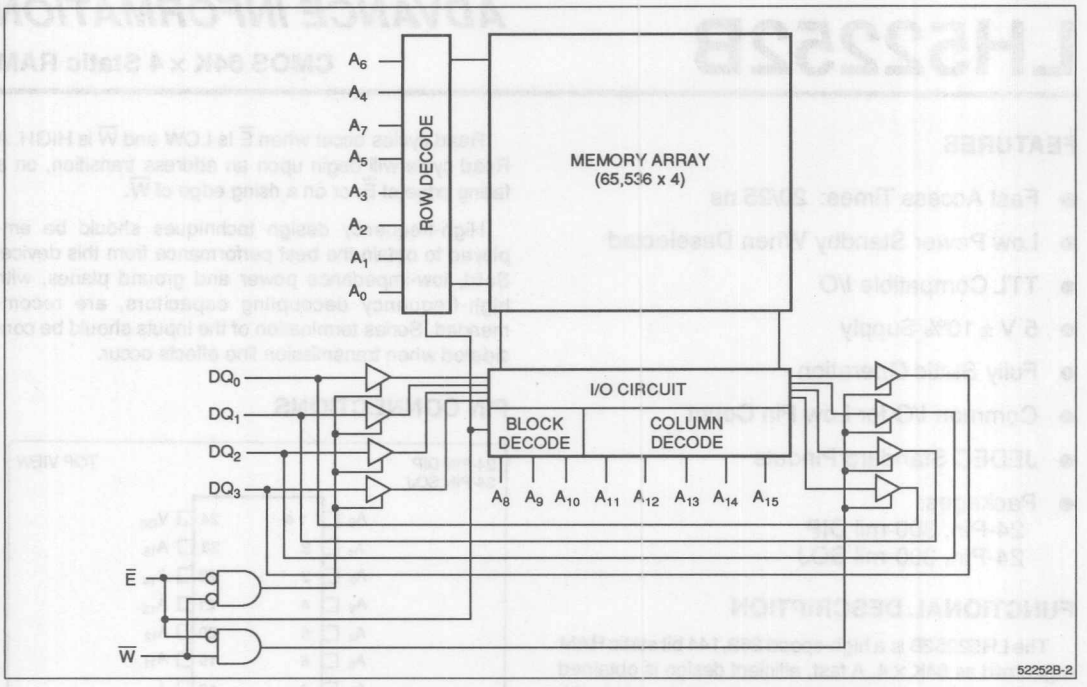


Figure 2. LH52252B Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	MODE	DQ	I_{CC}
H	X	Not Selected	High-Z	Standby
L	H	Read	Data Out	Active
L	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{15}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC}+0.5 V
DC Output Current [2]	±40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	Outputs open, t_{CYCLE} = 20 ns		70	145	mA
I_{CC1}	Operating Current [2]	Outputs open, t_{CYCLE} = 25 ns		60	135	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.005	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$		5	10	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTES:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

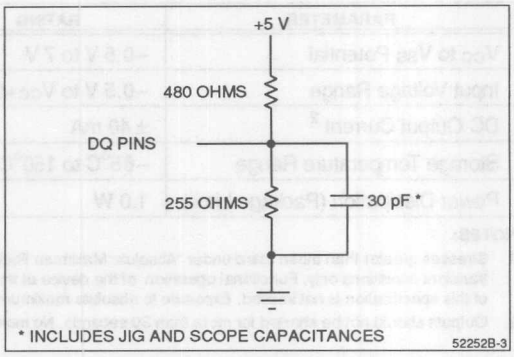


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	8 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		UNITS
		MIN	MAX	MIN	MAX	
	READ CYCLE					
t_{RC}	Read Cycle Timing	20		25		ns
t_{AA}	Address Access Time		20		25	ns
t_{OH}	Output Hold from Address Change	3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [3]	4		4		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		12	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		25		30	ns
	WRITE CYCLE					
t_{WC}	Write Cycle Time	20		25		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		ns
t_{AW}	Address Valid to End of Write	15		20		ns
t_{AS}	Address Setup	0		0		ns
t_{AH}	Address Hold from End of Write	0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	12		15		ns
t_{DW}	Input Data Setup Time	10		10		ns
t_{DH}	Input Data Hold Time	0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		7		8	ns
t_{WLZ}	$\overline{W}$ High to Output Active [3]	4		4		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, and $\overline{E}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid while $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}.

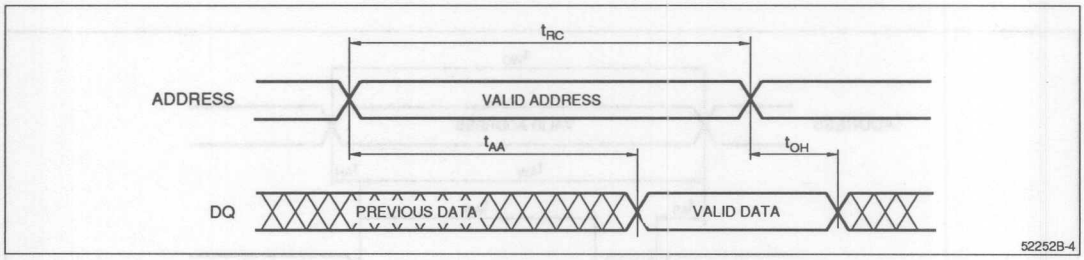


Figure 4. Read Cycle No. 1

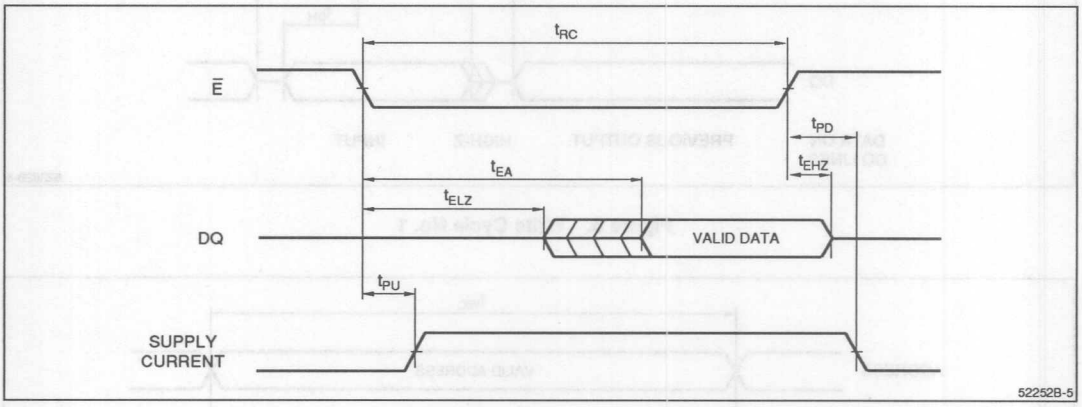


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be high during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

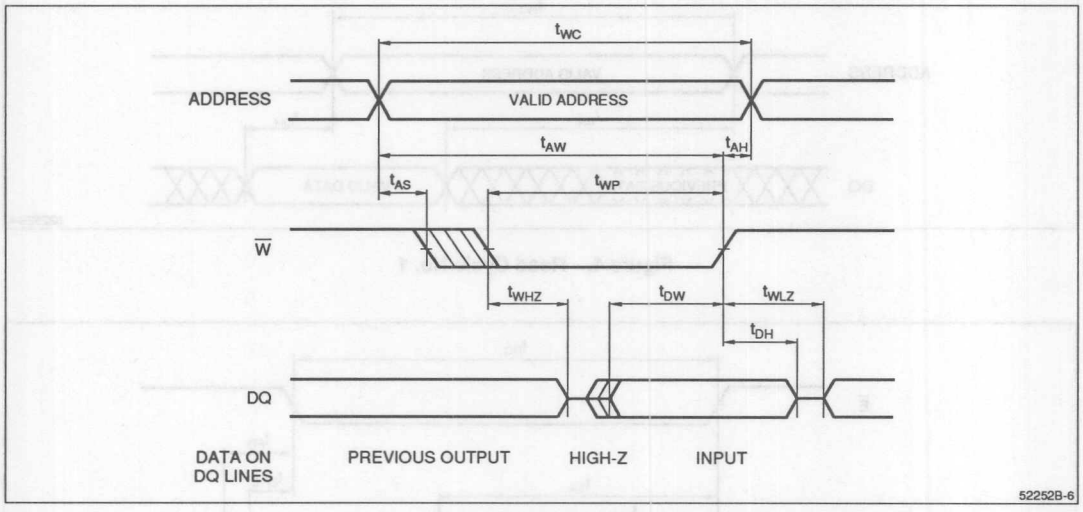


Figure 6. Write Cycle No. 1

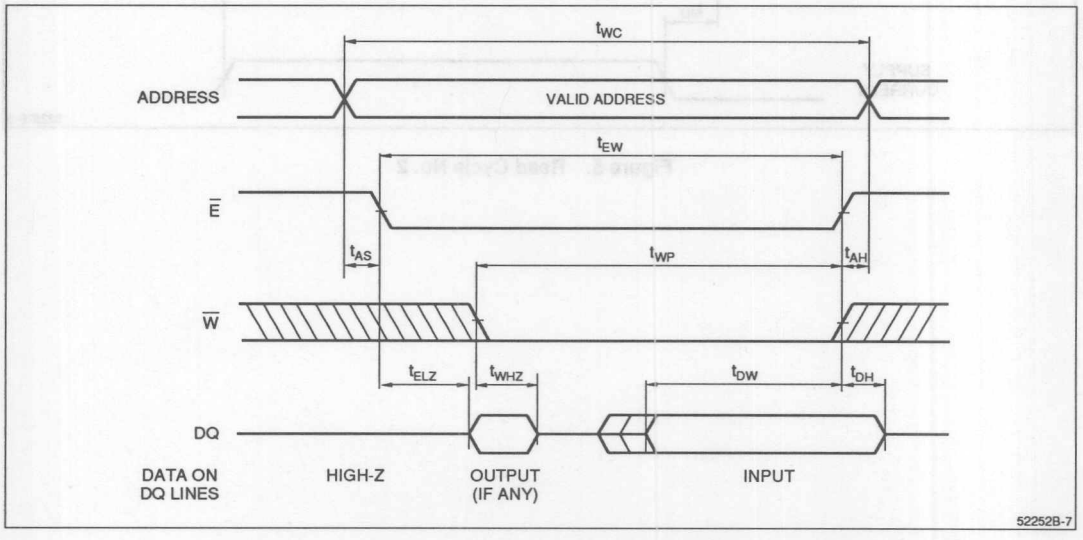
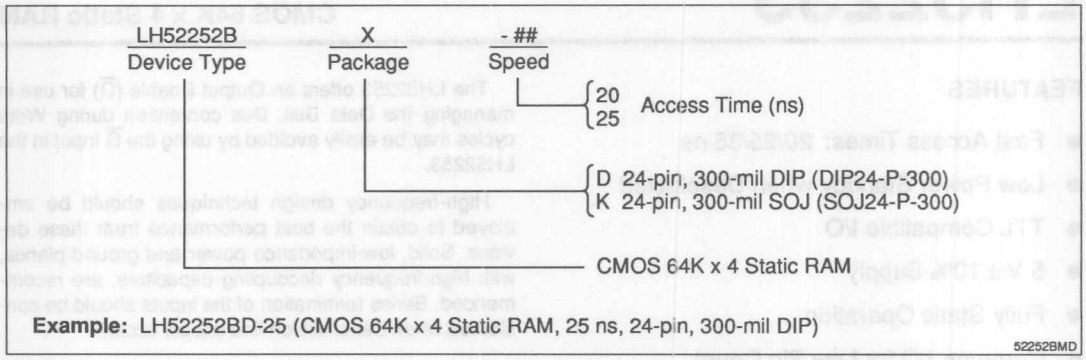


Figure 7. Write Cycle No. 2

ORDERING INFORMATION



LH52253

CMOS 64K × 4 Static RAM

FEATURES

- Fast Access Times: 20/25/35 ns
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count
- JEDEC Standard Pinouts
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 300-mil SOJ

FUNCTIONAL DESCRIPTION

The LH52253 is a very high-speed 256K-bit static RAM organized as 64K × 4. This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is inactive (HIGH). The combination of $\overline{E}$ and $\overline{W}$ control the mode of operation of the LH52253.

Write cycles occur when both $\overline{E}$ and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 16 address lines.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static read of the memory location specified by the address lines will occur. Since the device is fully static in operation, new read cycles can be performed by simply changing the address. An Automatic Power Down feature reduces the current consumption when Read and Write cycles extend beyond their minimum cycle times.

The LH52253 offers an Output Enable ($\overline{G}$) for use in managing the Data Bus. Bus contention during Write cycles may be easily avoided by using the $\overline{G}$ input in the LH52253.

High-frequency design techniques should be employed to obtain the best performance from these devices. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

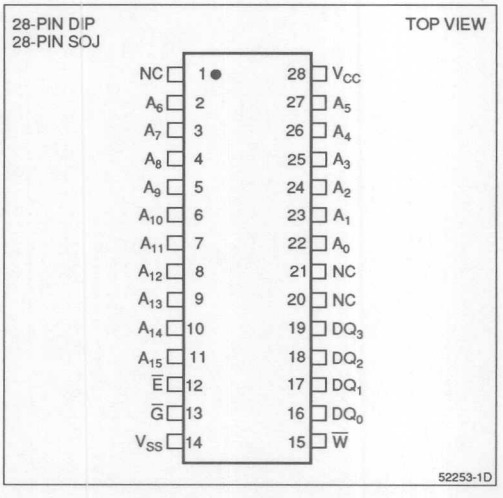


Figure 1. Pin Connections for DIP and SOJ

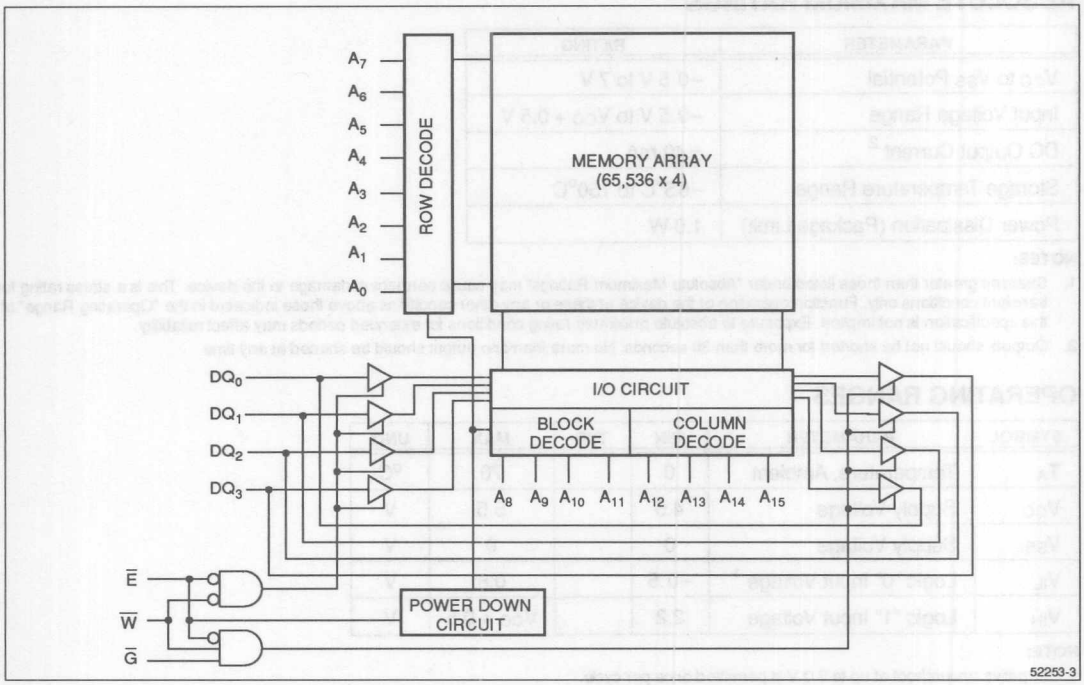


Figure 2. LH52253 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{W}$	$\overline{G}$	MODE	DQ	Icc
H	X	X	Not Selected	High-Z	Standby
L	H	L	Read	Data Out	Active
L	H	H	Read	High-Z	Active
L	L	X	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{15}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
$\overline{G}$	Output Enable input
Vcc	Positive Power Supply
Vss	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	±40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Function operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	Outputs open, t_{CYCLE} = 20 ns $\overline{G} = V_{IH}$, $\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$ or V_{IH}		70	145	mA
I_{CC1}	Operating Current [2]	Outputs open, t_{CYCLE} = 25 ns $\overline{G} = V_{IH}$, $\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$ or V_{IH}		60	135	mA
I_{CC1}	Operating Current [2]	Outputs open, t_{RC} = 35 ns $\overline{G} = V_{IH}$, $\overline{CE} = V_{IL}$, $\overline{WE} = V_{IL}$ or V_{IH}		50	135	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.005	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$ min		5	10	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTE:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	8 pF
C_{DQ} (Input/Output Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

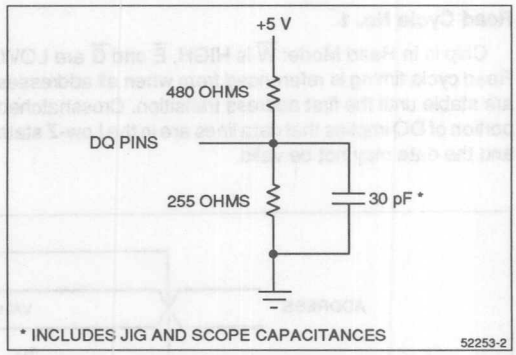


Figure 3. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
	READ CYCLE							
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold From Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	4		4		4		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		10		12	ns
t_{GA}	$\overline{G}$ Low to Valid Data		10		12		15	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	9	0	10	0	12	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		25		30		35	ns
	WRITE CYCLE							
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		25		ns
t_{AW}	Address Valid to End of Write	15		20		25		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold From End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	12		15		20		ns
t_{DW}	Input Data Setup Time	10		10		12		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	4		4		4		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		7		8		10	ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of DQ implies that data lines are in the Low-Z state and the data may not be valid.

Read Cycle No. 2

Chip is in the Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid when $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Valid Data will be present following t_{GA} only if t_{EA} timing has been met.

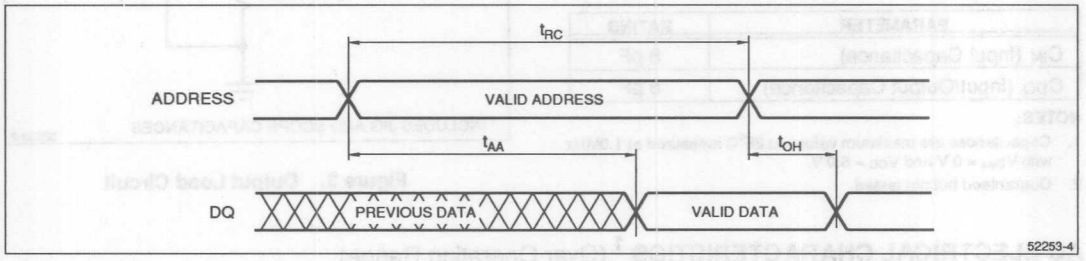


Figure 4. Read Cycle No. 1

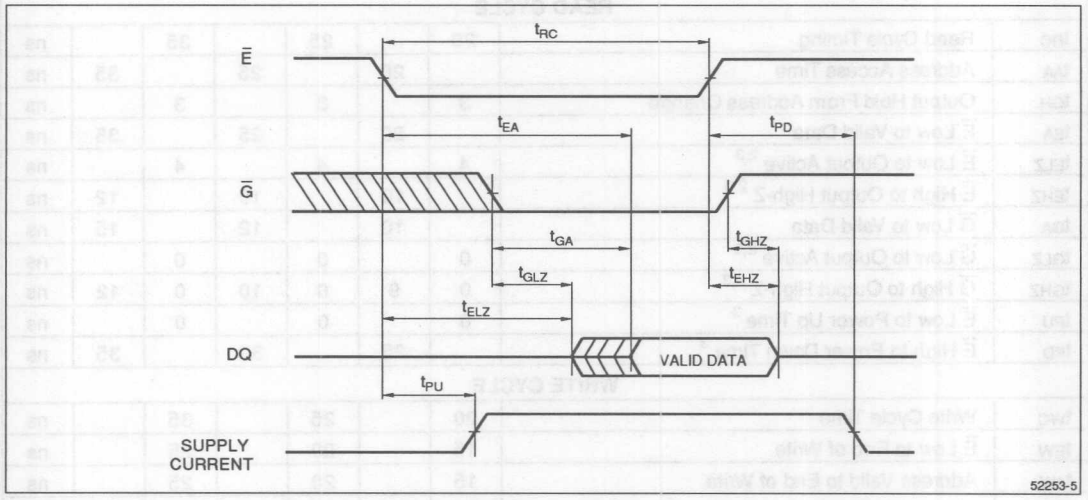


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise. These timing diagrams assume $\overline{G}$ is LOW, but it should be kept HIGH during Write cycles to insure that the output drivers are disabled.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

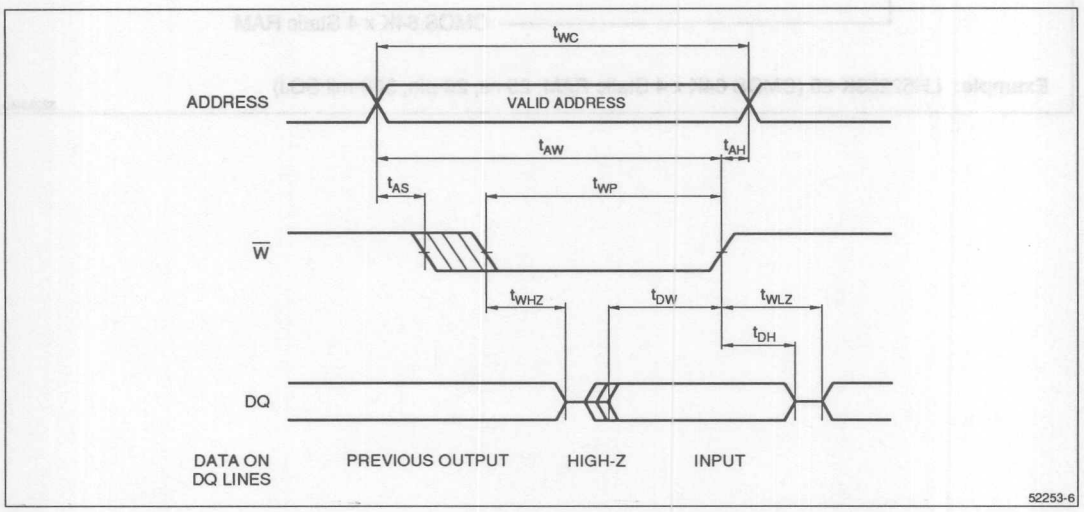


Figure 6. Write Cycle No. 1

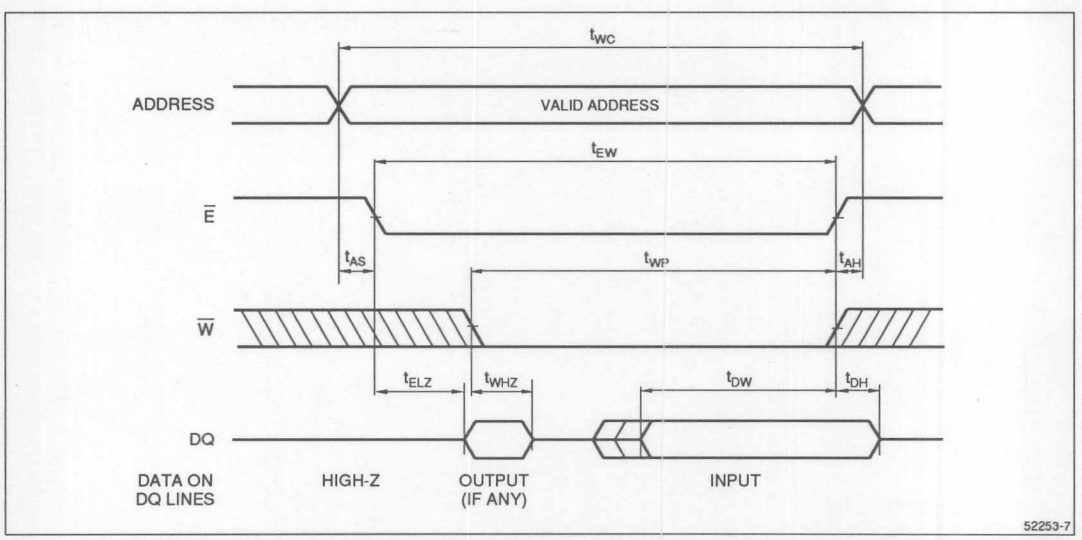
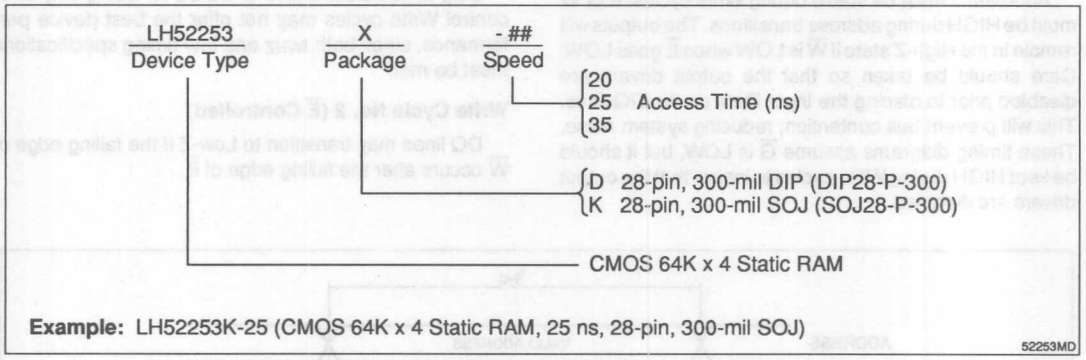


Figure 7. Write Cycle No. 2

ORDERING INFORMATION



LH52258

CMOS 32K × 8 Static RAM

FEATURES

- Fast Access Times: 35/45/55 ns
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 300-mil SOJ

FUNCTIONAL DESCRIPTION

The LH52258 is a high-speed 262,144 bit static RAM organized as 32K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. Proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

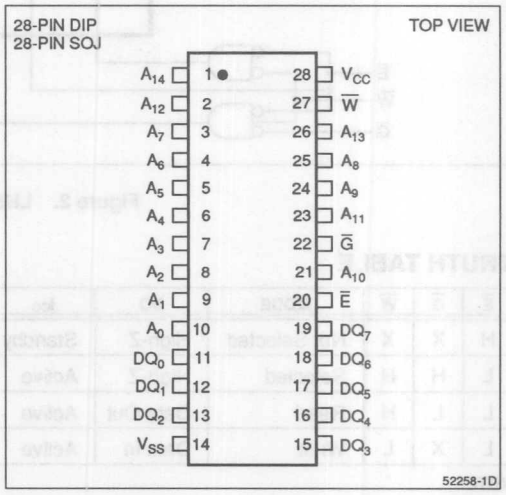


Figure 1. Pin Connections for DIP and SOJ Packages

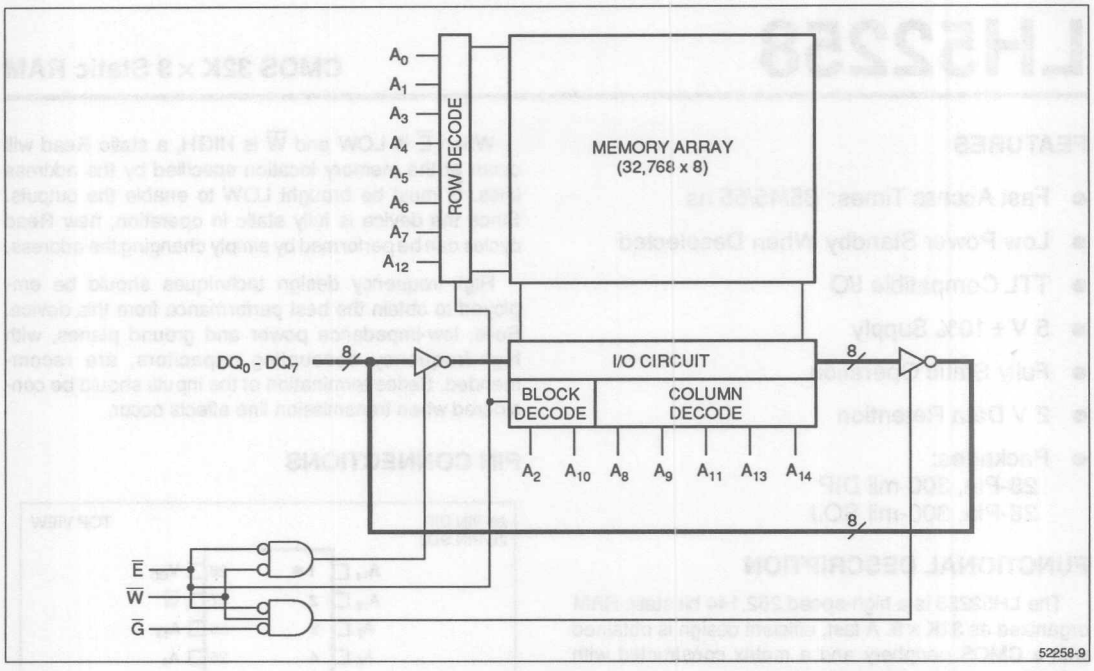


Figure 2. LH52258 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	I_{CC}
H	X	X	Not Selected	High-Z	Standby
L	H	H	Selected	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	$\overline{G} = V_{IH}$, $\overline{E} = V_{IL}$, I_{OUT} = 0 mA All other Inputs = V_{IL} or V_{IH} minimum cycle time = 35 ns		130	170	mA
I_{CC1}	Operating Current [2]	$\overline{G} = V_{IH}$, $\overline{E} = V_{IL}$, I_{OUT} = 0 mA All other Inputs = V_{IL} or V_{IH} minimum cycle time = 45 ns		110	155	mA
I_{CC1}	Operating Current [2]	$\overline{G} = V_{IH}$, $\overline{E} = V_{IL}$, I_{OUT} = 0 mA All other Inputs = V_{IL} or V_{IH} minimum cycle time = 55 ns		100	155	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.02	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$		2	5	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			200	µA

NOTE:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

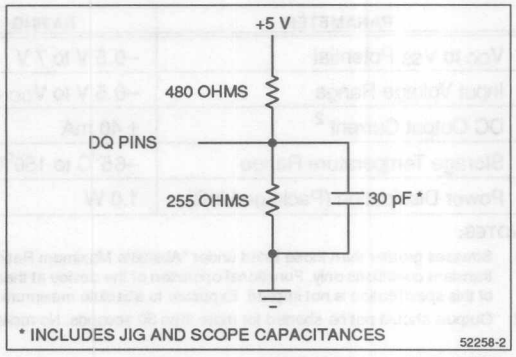


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are "Don't Care."

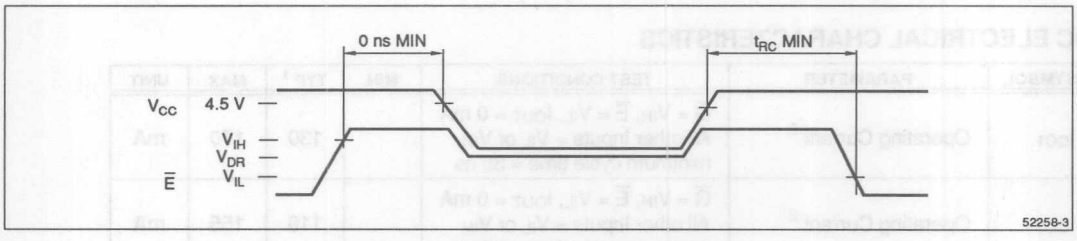


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-35		-45		-55		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Time	35		45		55		ns
t_{AA}	Address Access Time		35		45		55	ns
t_{OH}	Output Hold from Address Change	5		5		5		ns
t_{EA}	$\overline{E}$ Low to Valid Data		35		45		55	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		15		20		25	ns
t_{GA}	$\overline{G}$ Low to Valid Data		15		20		25	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	3		3		3		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		15		20		25	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		35		45		55	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	35		45		55		ns
t_{EW}	$\overline{E}$ Low to End of Write	30		40		50		ns
t_{AW}	Address Valid to End of Write	30		40		50		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	20		25		25		ns
t_{DW}	Input Data Setup Time	15		20		25		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		15		15		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	0		0		0		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±200 mV transition from steady state levels into the test load.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

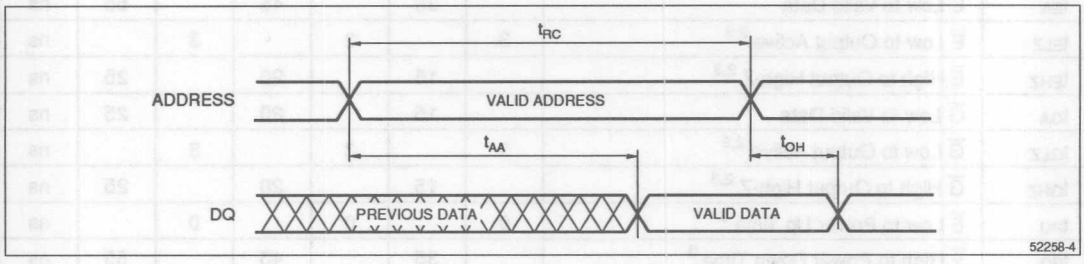


Figure 5. Read Cycle No. 1

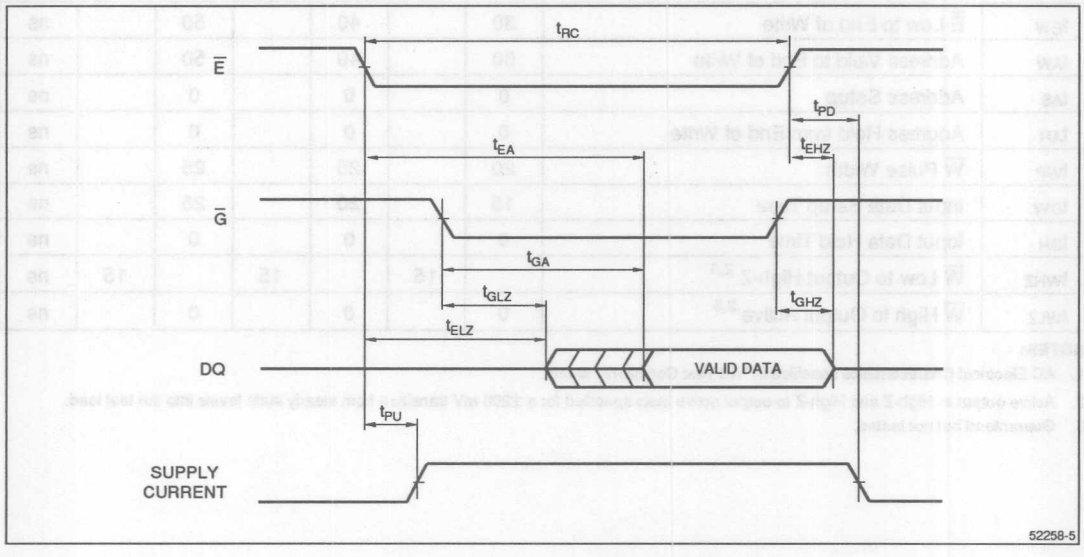


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH52258's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

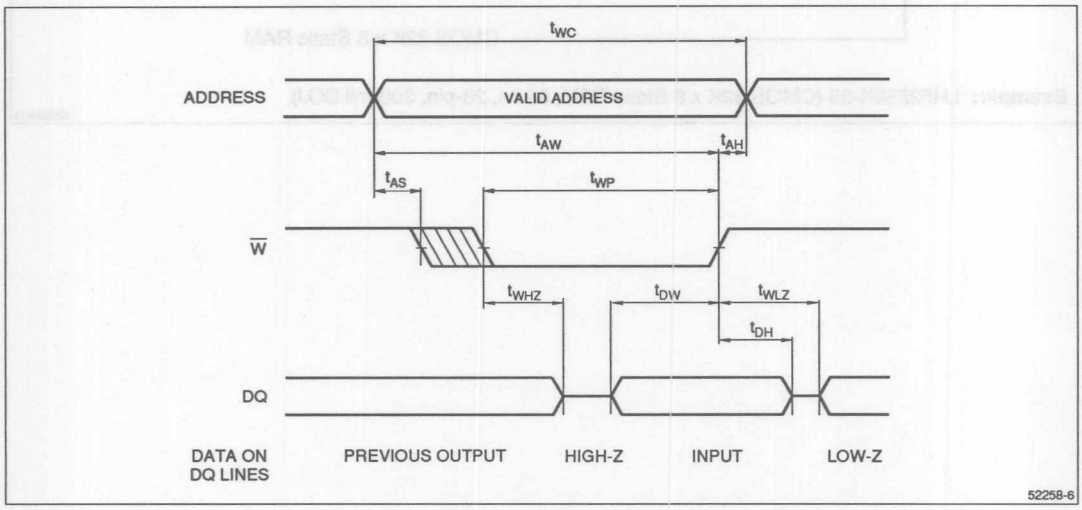


Figure 7. Write Cycle No. 1

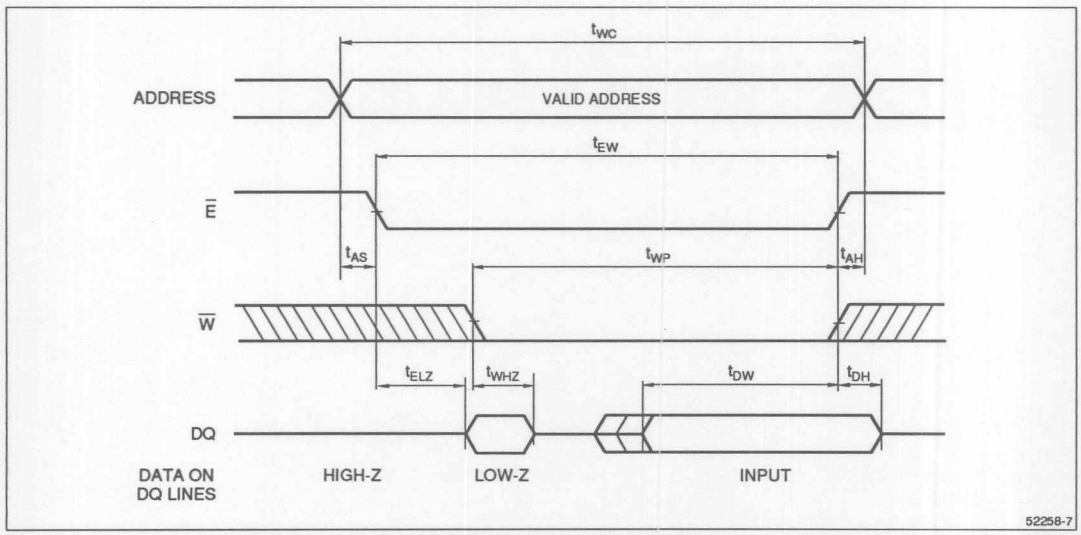
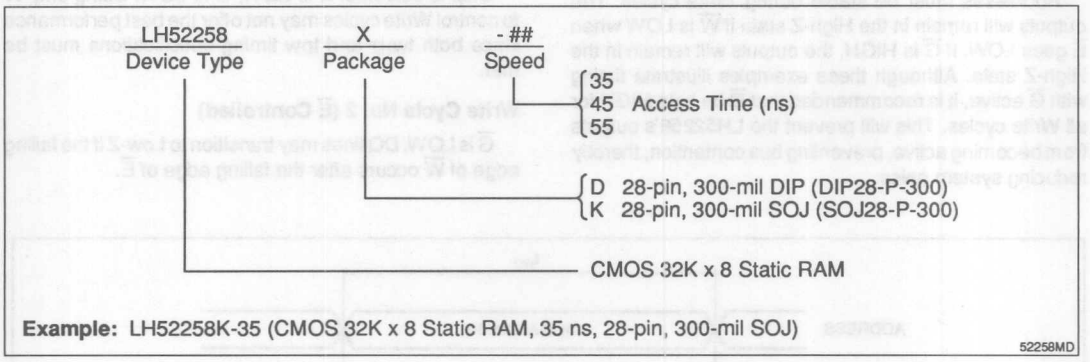


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



Example: LH52258K-35 (CMOS 32K x 8 Static RAM, 35 ns, 28-pin, 300-mil SOJ)

LH52258A

CMOS 32K × 8 Static RAM

FEATURES

- Fast Access Times: 20/25 ns
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- JEDEC Standard Pinout
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 300-mil SOJ

FUNCTIONAL DESCRIPTION

The LH52258A is a high-speed 262,144 bit static RAM organized as 32K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High-frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high-frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

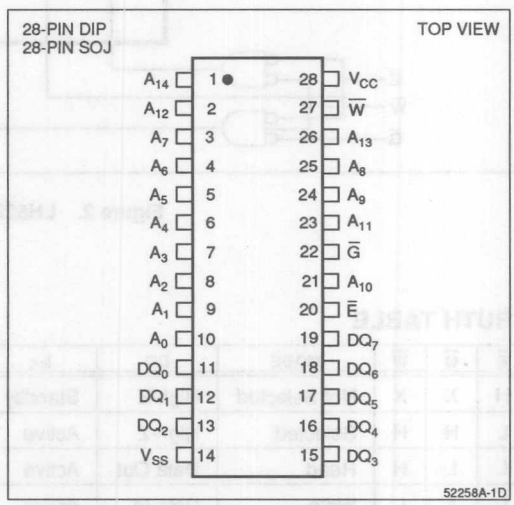


Figure 1. Pin Connections for DIP and SOJ Packages

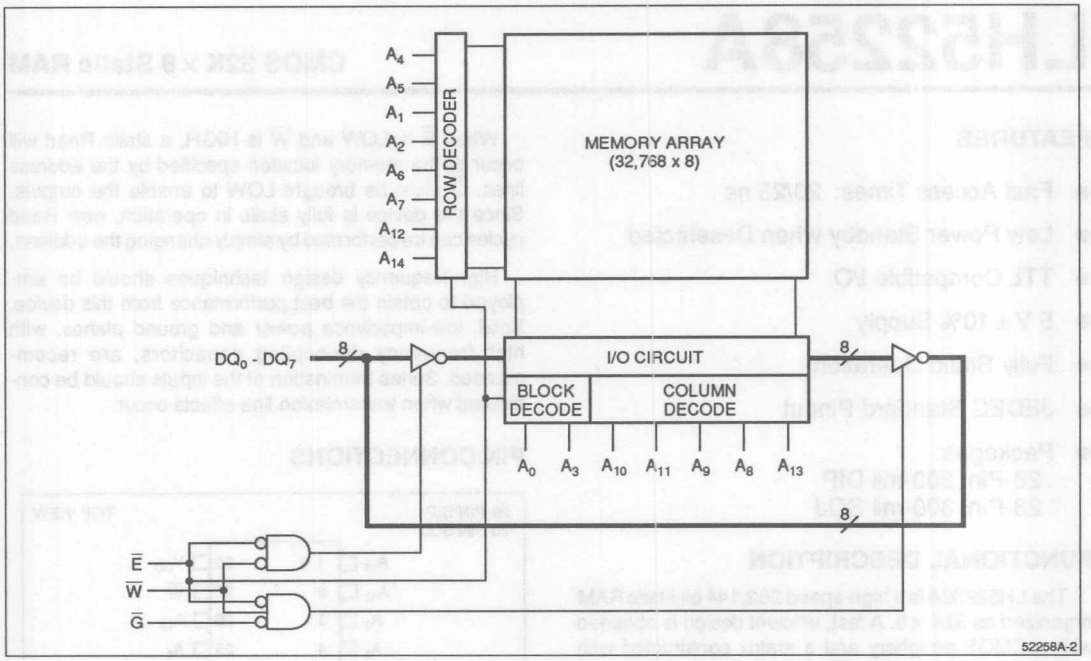


Figure 2. LH52258A Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	I_{CC}
H	X	X	Not Selected	High-Z	Standby
L	H	H	Selected	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65° to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	t_{RC} = 20 ns $\overline{G} \geq V_{IH}$, $\overline{E} \leq V_{IL}$, I_{OUT} = 0 mA, t_{CYCLE} = 20 ns		95	150	mA
I_{CC1}	Operating Current [2]	t_{RC} = 25 ns $\overline{G} \geq V_{IH}$, $\overline{E} \leq V_{IL}$, I_{OUT} = 0 mA, t_{CYCLE} = 25 ns		90	140	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC}$ − 0.2 V		0.005	1	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$		6	15	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 m A			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC}$ − 0.2 V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC}$ − 0.2 V			250	µA

NOTE:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	3 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

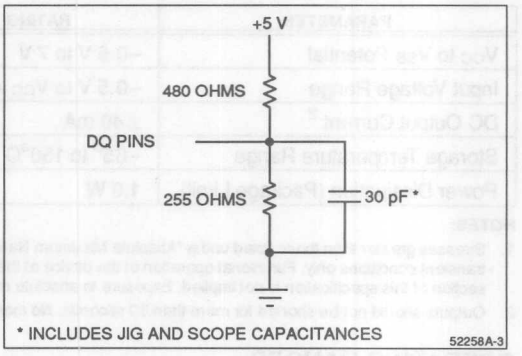


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to prevent improper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are 'Don't Care.'

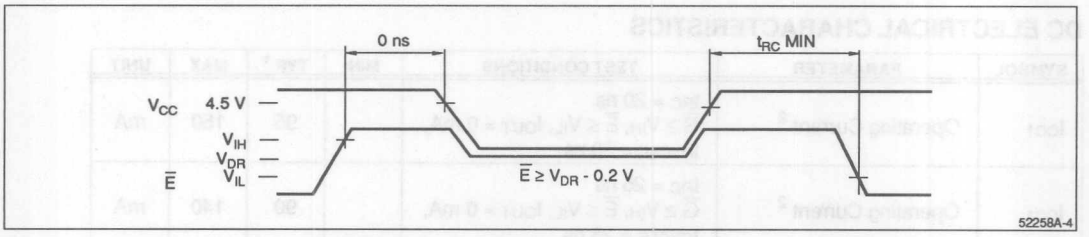


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		UNITS
		MIN	MAX	MIN	MAX	
	READ CYCLE					
t_{RC}	Read Cycle Time	20		25		ns
t_{AA}	Address Access Time		20		25	ns
t_{OH}	Output Hold from Address Change	4		4		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	4		4		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]	0	10	0	12	ns
t_{GA}	$\overline{G}$ Low to Valid Data		10		12	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	9	0	10	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		25		30	ns
	WRITE CYCLE					
t_{WC}	Write Cycle Time	20		25		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		ns
t_{AW}	Address Valid to End of Write	15		20		ns
t_{AS}	Address Setup	0		0		ns
t_{AH}	Address Hold from End of Write	0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	12		15		ns
t_{DW}	Input Data Setup Time	10		12		ns
t_{DH}	Input Data Hold Time	0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	0		0		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. The test load has 5 pF capacitances.
3. Guaranteed by design but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

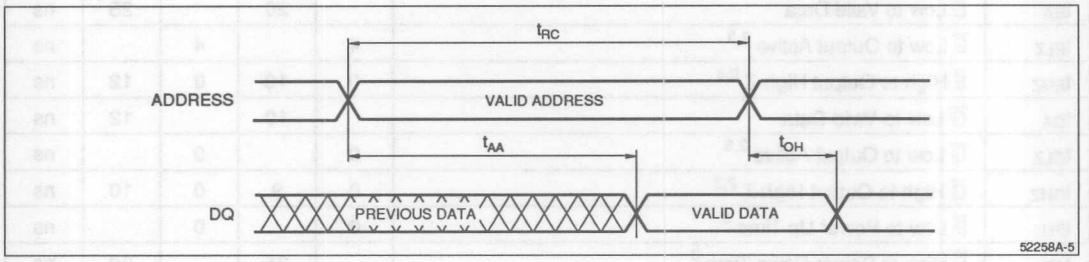


Figure 5. Read Cycle No. 1

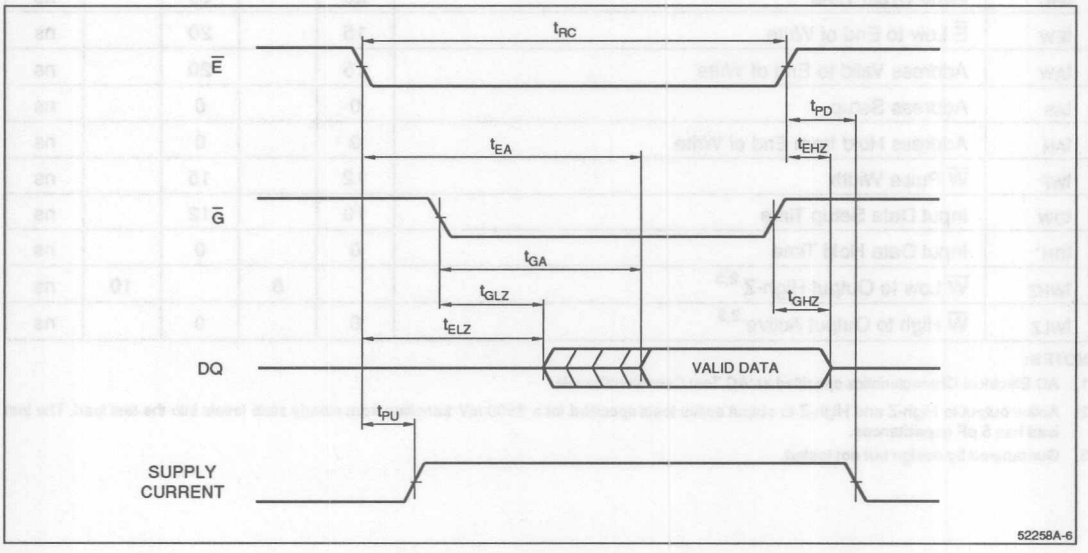


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH52258A's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

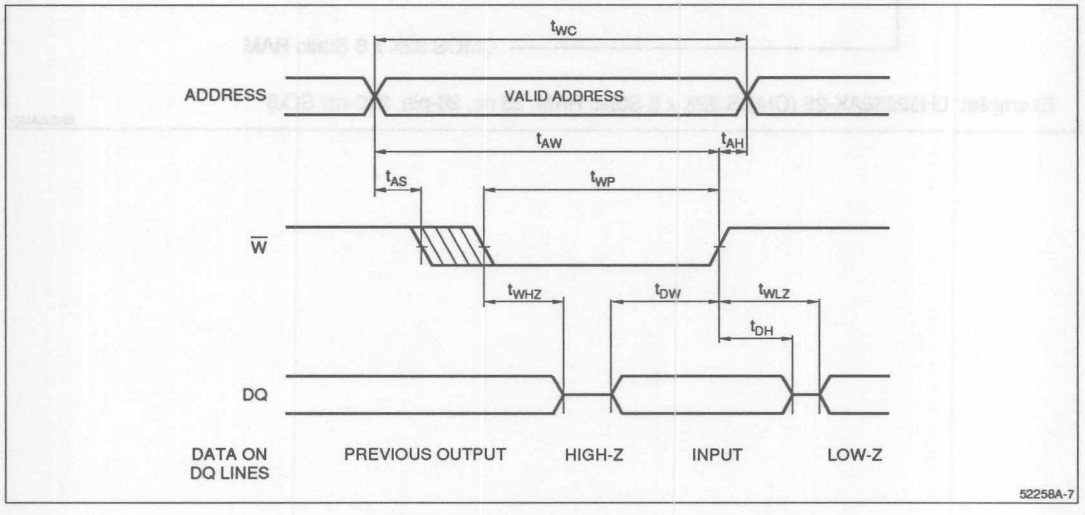


Figure 7. Write Cycle No. 1

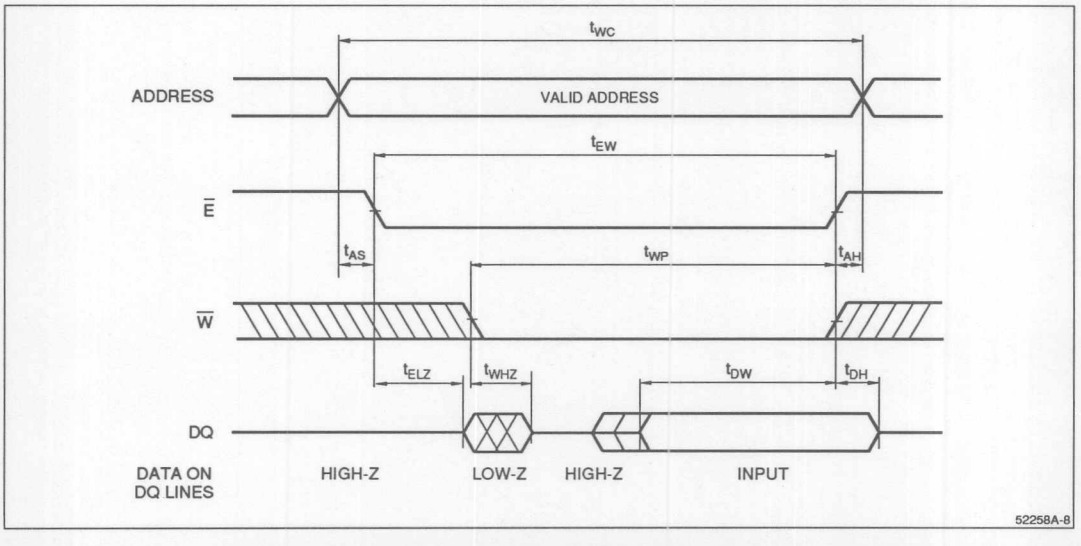
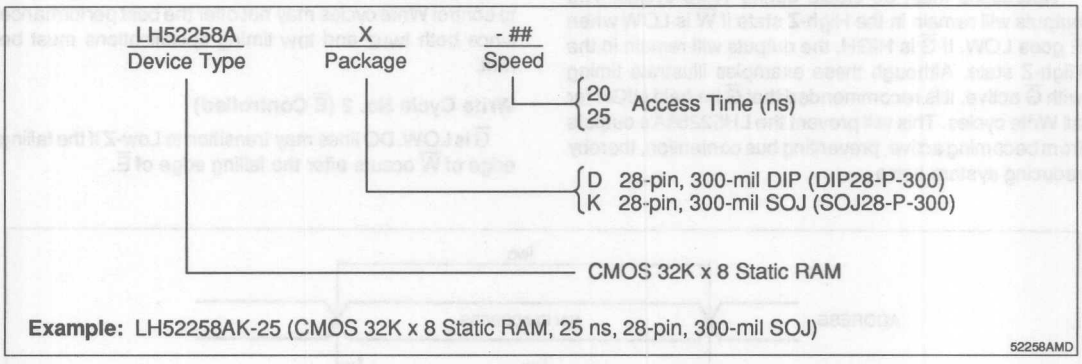


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH52258B

PRELIMINARY

CMOS 32K × 8 Static RAM

FEATURES

- Fast Access Times: 25/35 ns
- JEDEC Standard Pinout
- Space Saving 28-Pin, 300-mil DIP
- High Density 28-Pin, 300-mil SOJ
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation

PIN CONNECTIONS

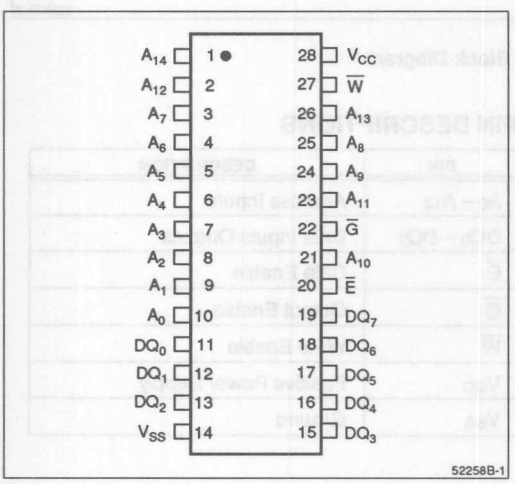


Fig. 1. Pin Connections for DIP and SOJ Packages

FUNCTIONAL DESCRIPTION

The LH52258B is a high speed 262,144 bit static RAM organized as 32K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power (I_{SB1}) drops to its lowest level if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 15 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High frequency design techniques should be employed to obtain the best performance from this device. Solid, low impedance power and ground planes, with high frequency decoupling capacitors, are desirable. Series termination of the inputs should be considered when transmission line effects occur.

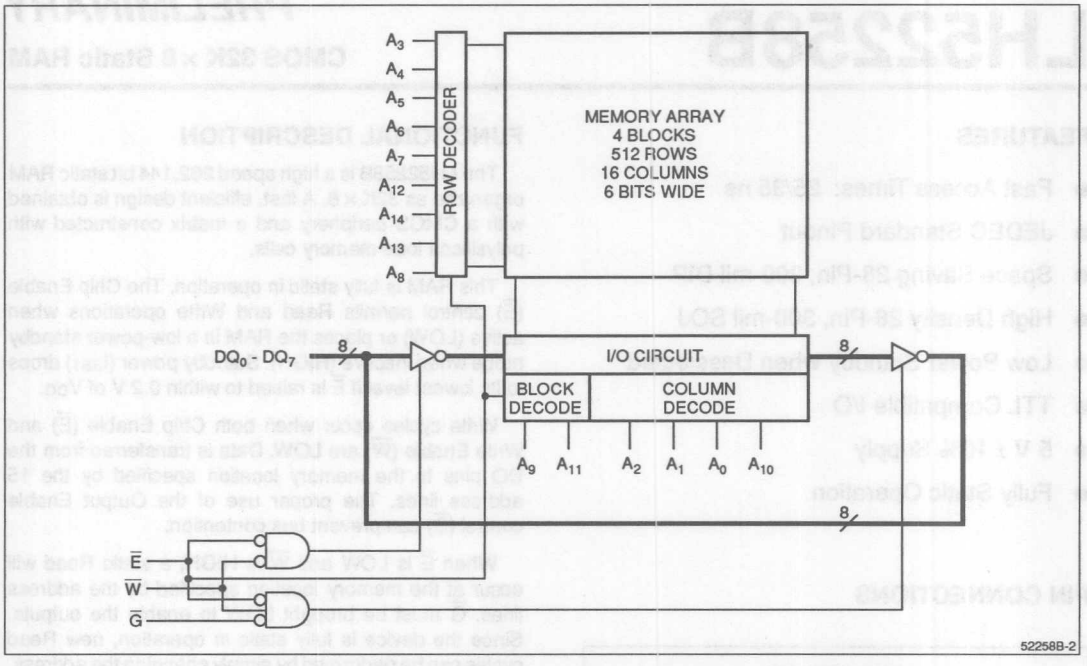


Figure 2. LH52258B Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Not Selected	High-Z	Standby
L	H	H	Selected	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{14}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{W}$	Write Enable
Vcc	Positive Power Supply
Vss	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65° to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic "1" Input Voltage	2.2		V_{CC} + 0.5	V

NOTES:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	$\overline{G} = V_{IH}$, $\overline{E} = V_{IL}$, I_{OUT} = 0 mA, T_{CYCLE} = 25 ns		90	150	mA
I_{CC1}	Operating Current [2]	$\overline{G} = V_{IH}$, $\overline{E} = V_{IL}$, I_{OUT} = 0 mA, T_{CYCLE} = 35 ns		70	130	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{IH}$, T_{CYCLE} = min. All other inputs at V_{IH}/V_{IL}		20	40	mA
I_{SB2}	Standby Current	$\overline{E} > V_{CC} - 0.2$ V All other inputs at $V_{CC} - 0.2$ V or 0.2 V		0.005	500	mA
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 m A			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			200	µA

NOTES:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open, operating at specified cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

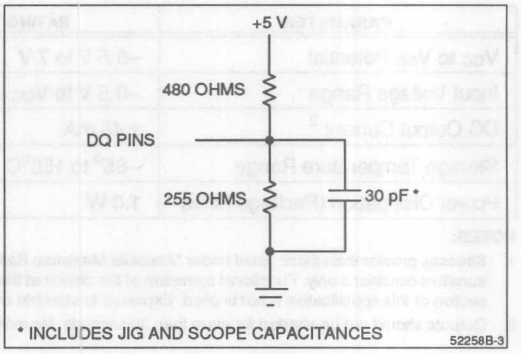


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to prevent improper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs must be ≤ 0.2 V or ≥ V_{CC} – 0.2 V.

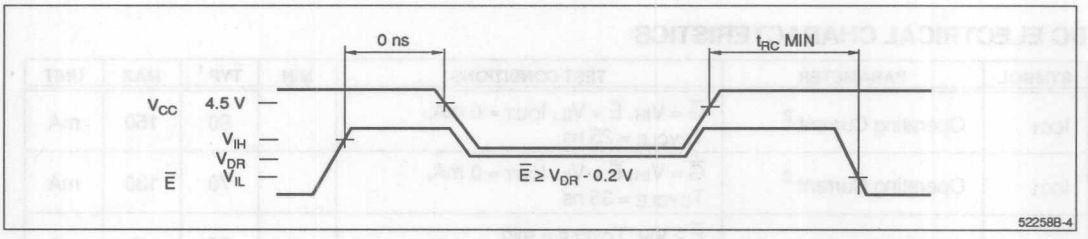


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-25		-35		UNITS
		MIN	MAX	MIN	MAX	
	READ CYCLE					
t_{RC}	Read Cycle Time	25		35		ns
t_{AA}	Address Access Time		25		35	ns
t_{OH}	Output Hold from Address Change	4		4		ns
t_{EA}	$\overline{E}$ Low to Valid Data		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	4		4		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]	0	12	0	15	ns
t_{GA}	$\overline{G}$ Low to Valid Data		12		15	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]	0	10	0	12	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		25		35	ns
	WRITE CYCLE					
t_{WC}	Write Cycle Time	25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		ns
t_{AW}	Address Valid to End of Write	15		20		ns
t_{AS}	Address Setup	0		0		ns
t_{AH}	Address Hold From End of Write	0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		ns
t_{DW}	Input Data Setup Time	12		15		ns
t_{DH}	Input Data Hold Time	0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	0		0		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. The test load has 5 pF capacitances.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

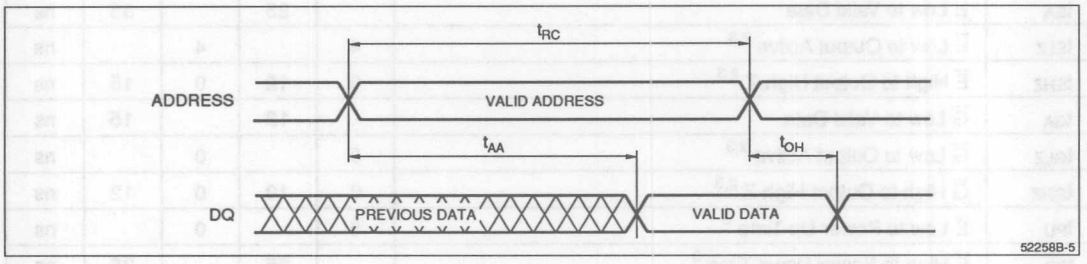


Figure 5. Read Cycle No. 1

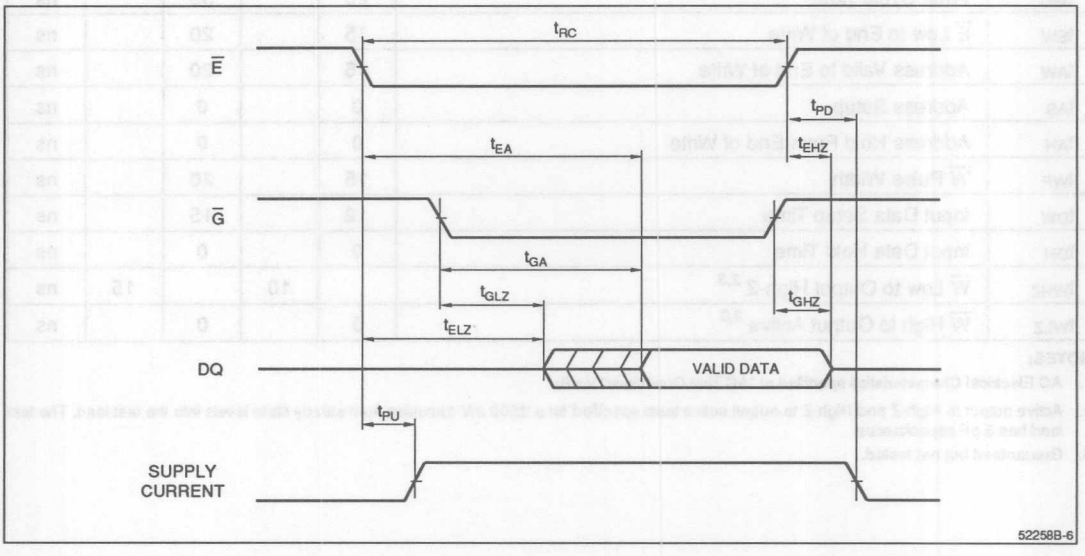


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH52258B's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

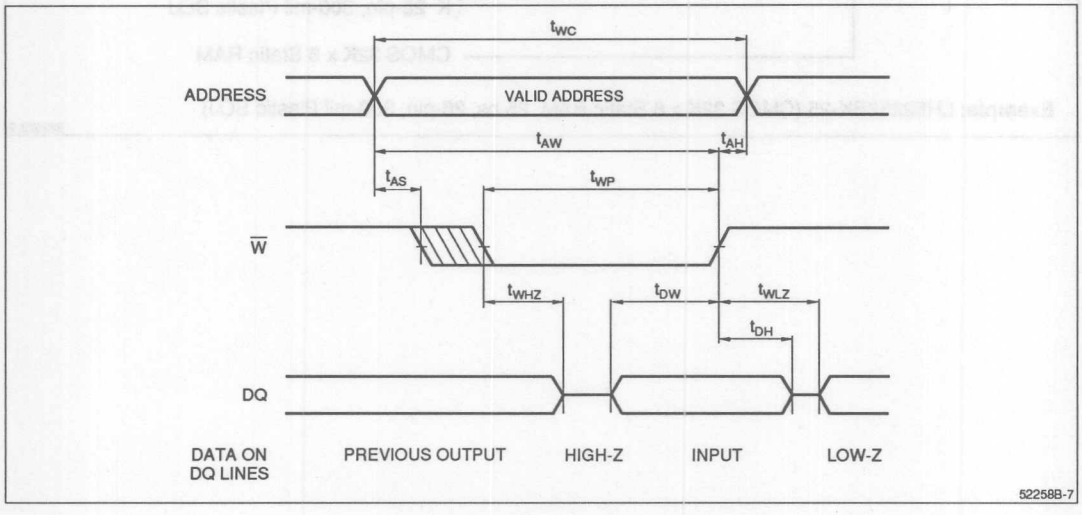


Figure 7. Write Cycle No. 1

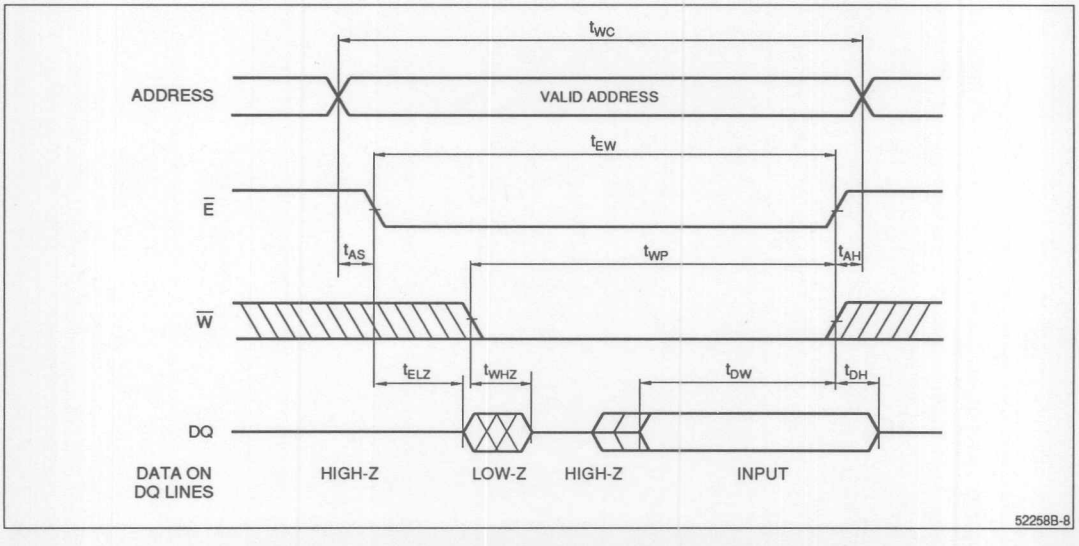
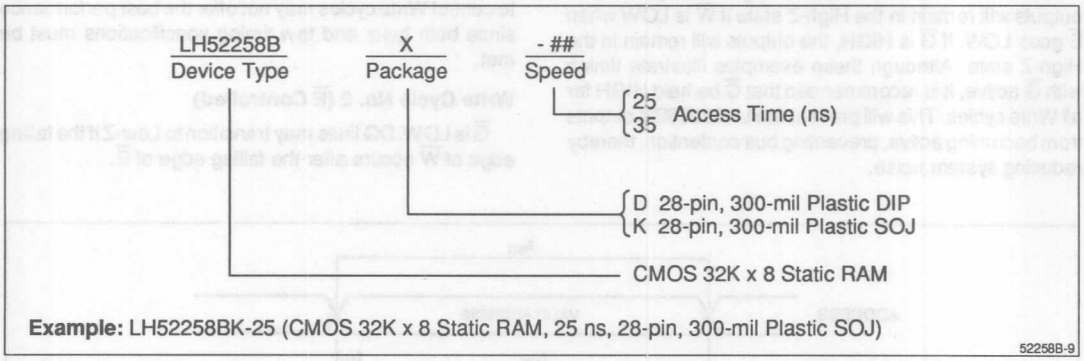


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH521002

CMOS 256K × 4 Static RAM

FEATURES

- Fast Access Times: 20/25/35 ns
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- Common I/O for Low Pin Count
- 2 V Data Retention
- JEDEC Standard Pinouts
- Package:
  28-Pin, 400-mil SOJ

FUNCTIONAL DESCRIPTION

The LH521002 is a high speed 1,048,576-bit static RAM organized as 256K × 4. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) reduces power to the chip when $\overline{E}$ is HIGH. Standby power drops to its lowest level (I_{SB1}) when $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 18 address lines.

Read cycles occur when $\overline{E}$ is LOW and $\overline{W}$ is HIGH. A Read cycle will begin upon an address transition, on a falling edge of $\overline{E}$, or on a rising edge of $\overline{W}$.

High frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

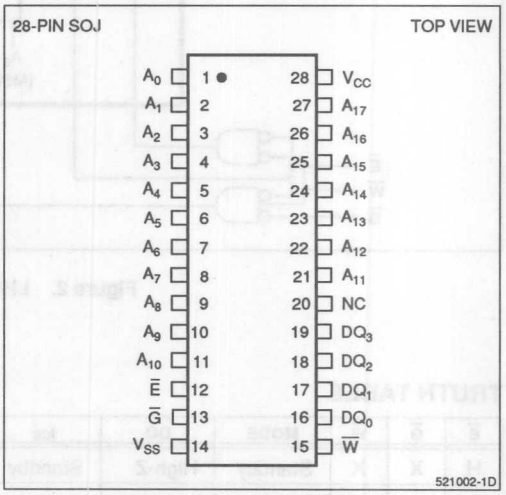


Figure 1. Pin Connections for SOJ Package

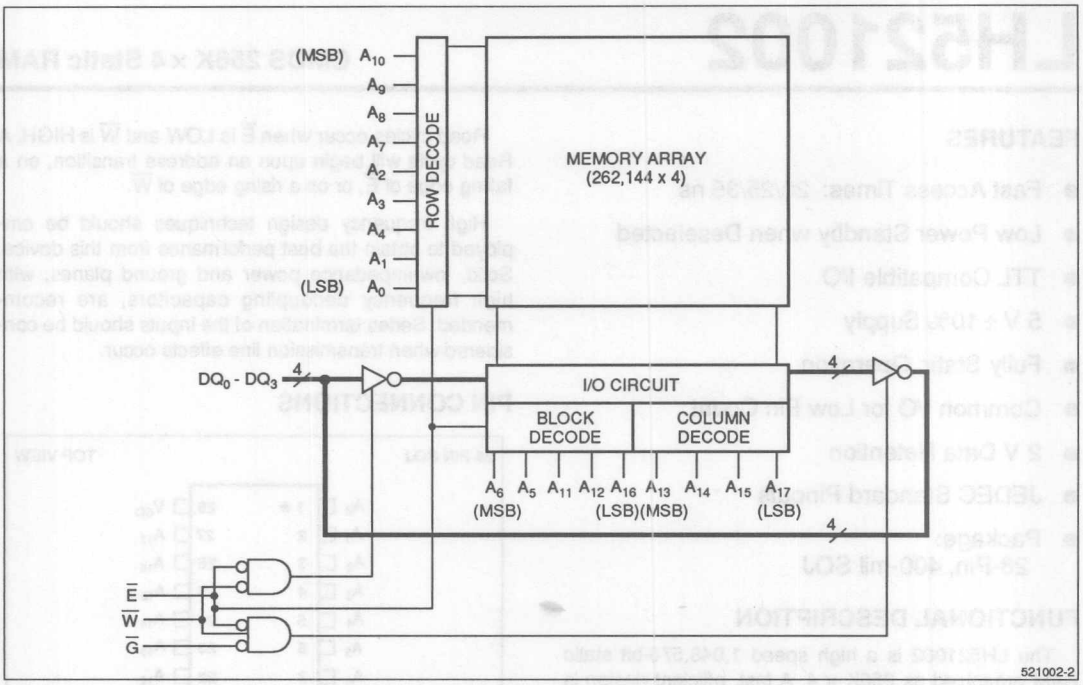


Figure 2. LH521002 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	Icc
H	X	X	Standby	High-Z	Standby
L	H	H	Selected	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{17}$	Address Inputs
$DQ_0 - DQ_3$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{W}$	Write Enable input
$\overline{G}$	Output Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5		5.5	V
V_{SS}	Supply Voltage	0		0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage [2]	2.2		V_{CC} + 0.5	V

NOTES:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	t_{CYCLE} = 20 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}		110	180	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 25 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}		100	180	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 35 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}		80	150	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.005	2	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$		8	20	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			500	µA

NOTE:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

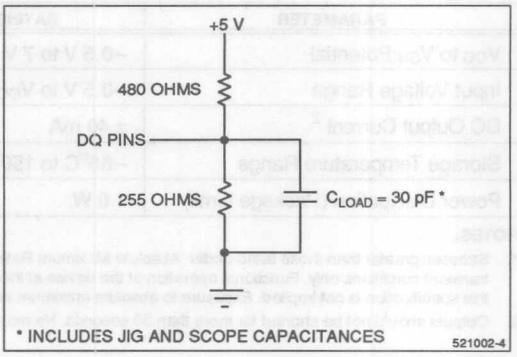


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. This parameter is sampled and not production tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are 'Don't Care.'

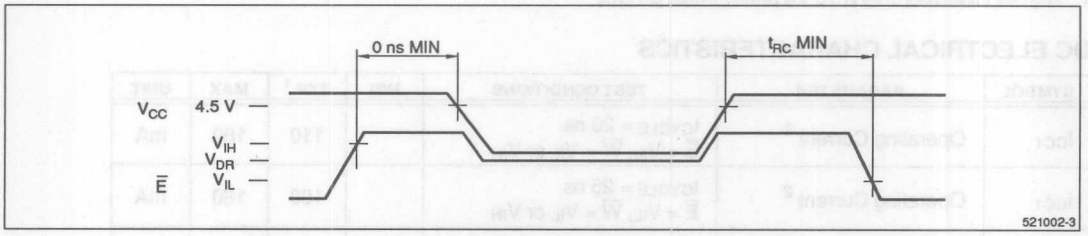


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		8		10		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		25		ns
t_{DW}	Input Data Setup Time	12		15		15		ns
t_{DH}	Input Data Hold Time	0		0		0		
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		3		3		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Following an Address transition, Data Out is guaranteed valid at t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid while $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, but may become valid as soon as t_{ELZ}. Outputs will transition from High-Z to Valid Data Out. Data Out is valid after both t_{EA} and t_{GA} are met.

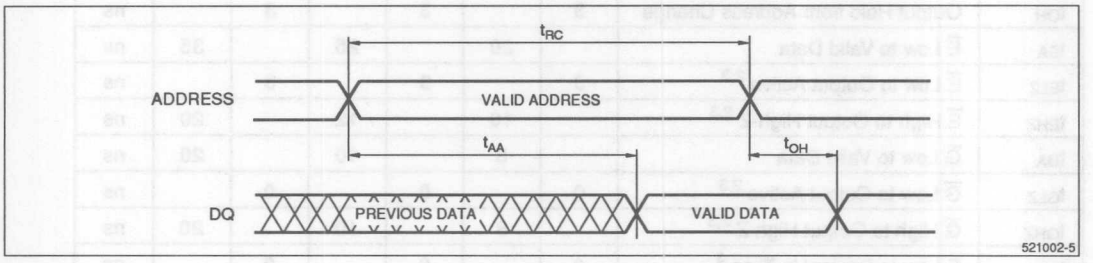


Figure 5. Read Cycle No. 1

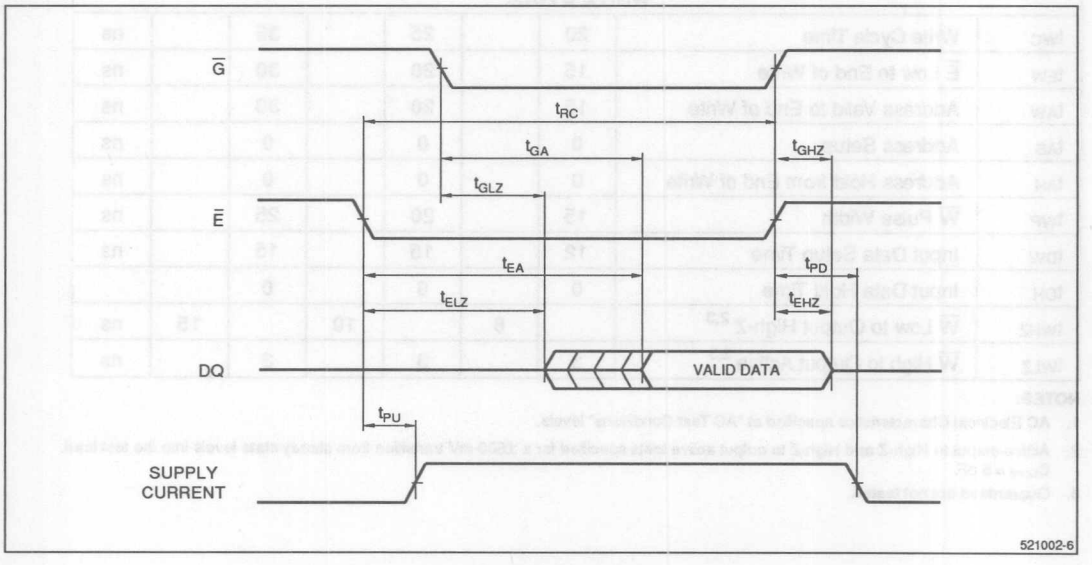


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. $\overline{E}$ or $\overline{W}$ must be HIGH during address transitions. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. Care should be taken so that the output drivers are disabled prior to placing the Input Data on the DQ lines. This will prevent bus contention, reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ and $\overline{G}$ are LOW. Using only $\overline{W}$ to control Write cycles may not offer the best device performance, since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

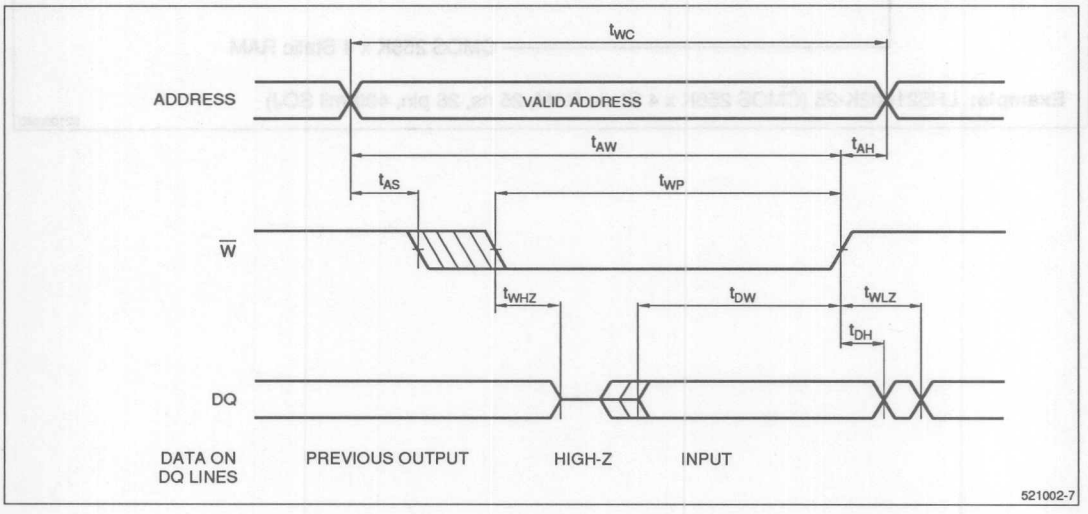


Figure 7. Write Cycle No. 1

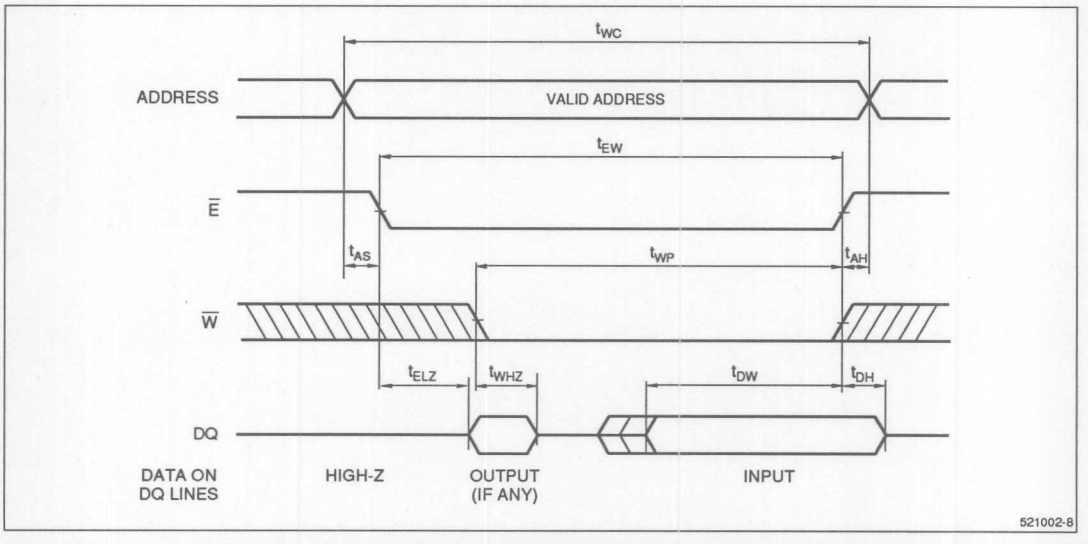
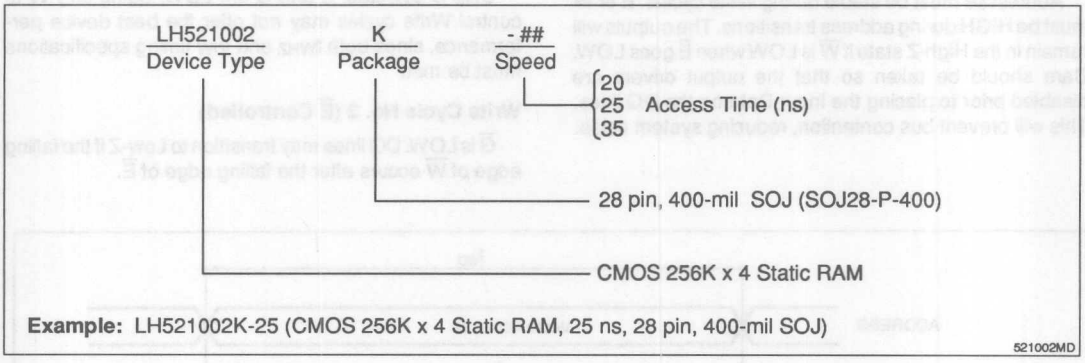


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH521007

PRELIMINARY

CMOS 128K × 8 Static RAM

FEATURES

- Fast Access Times: 20/25/35 ns
- Two Chip Enable Controls
- Low Power Standby When Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention
- Packages:
  32-Pin, 400-mil DIP
  32-Pin, 400-mil SOJ

FUNCTIONAL DESCRIPTION

The LH521007 is a high speed 1,048,576-bit static RAM organized as 128K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enables ($\overline{E}_1$, E_2) permit Read and Write operations when active ($\overline{E}_1$ = LOW and E_2 = HIGH) or place the RAM in a low-power standby mode when inactive ($\overline{E}_1$ = HIGH or E_2 = LOW). Standby power drops to its lowest level when all inputs are stable and are at CMOS levels, while the chip is in standby mode.

Write cycles occur when both Chip Enables and Write Enable are active. Data is transferred from the DQ pins to the memory location specified by the 17 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When both Chip Enables are active and $\overline{W}$ is inactive, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

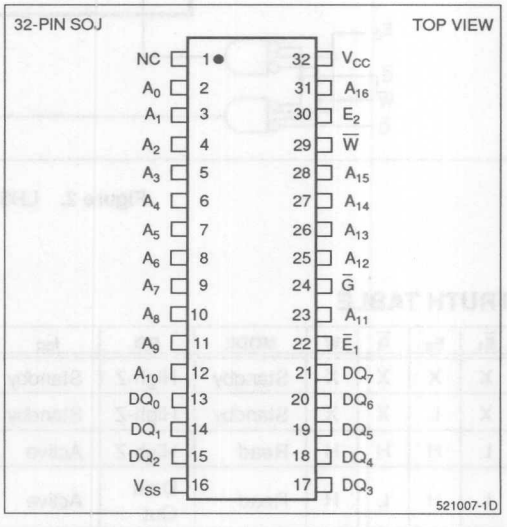


Figure 1. Pin Connections for DIP and SOJ Packages

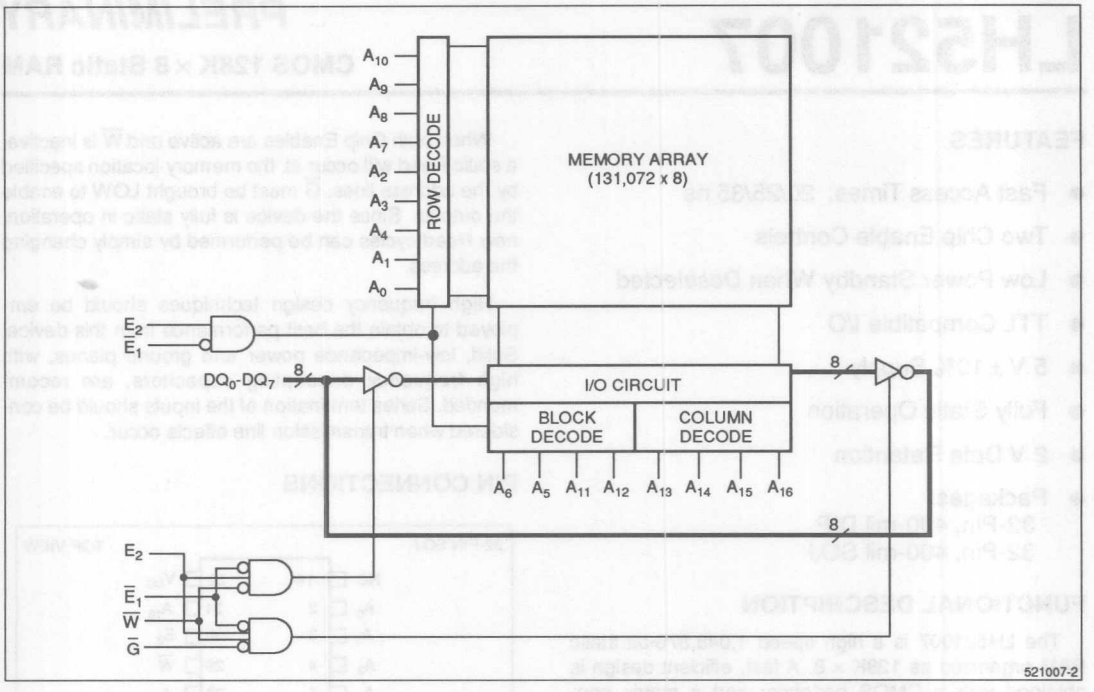


Figure 2. LH521007 Block Diagram

TRUTH TABLE

$\overline{E}_1$	E_2	$\overline{G}$	$\overline{W}$	MODE	DQ	I_{CC}
X	X	X	X	Standby	High-Z	Standby
X	L	X	X	Standby	High-Z	Standby
L	H	H	H	Read	High-Z	Active
L	H	L	H	Read	Data Out	Active
L	H	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{16}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}_1$, E_2	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	±40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	t_{CYCLE} = 20 ns		125	140	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 25 ns		100	125	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 35 ns		85	115	mA
I_{SB1}	Standby Current	$\overline{E}_1 \geq V_{IH}$ or $E_2 \leq V_{IL}$ t_{CYC} = min, I_{OUT} = 0		15	35	mA
I_{SB2}	Standby Current	$\overline{E}_1 \geq V_{CC}$ − 0.2 V or $E_2 \leq$ 0.2 V, t_{CYC} = min, I_{OUT} = 0		0.5	5	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E}_1 \geq V_{CC}$ − 0.2 V and $E_2 \leq$ 0.2 V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E}_1 \geq V_{CC}$ − 0.2 V and $E_2 \leq$ 0.2 V			500	µA

NOTES:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

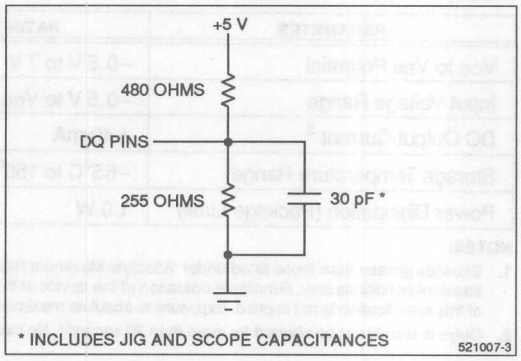


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Sample tested only.

DATA RETENTION TIMING

For data retention mode, either $\overline{E}_1 \geq V_{CC} - 0.2$ V or $E_2 \leq 0.2$ V. The other control signals must be at valid CMOS levels ($V_{CC} - 0.2$ V $\leq V_{IN} \leq 0.2$ V). The address and data buses are 'Don't Care.'

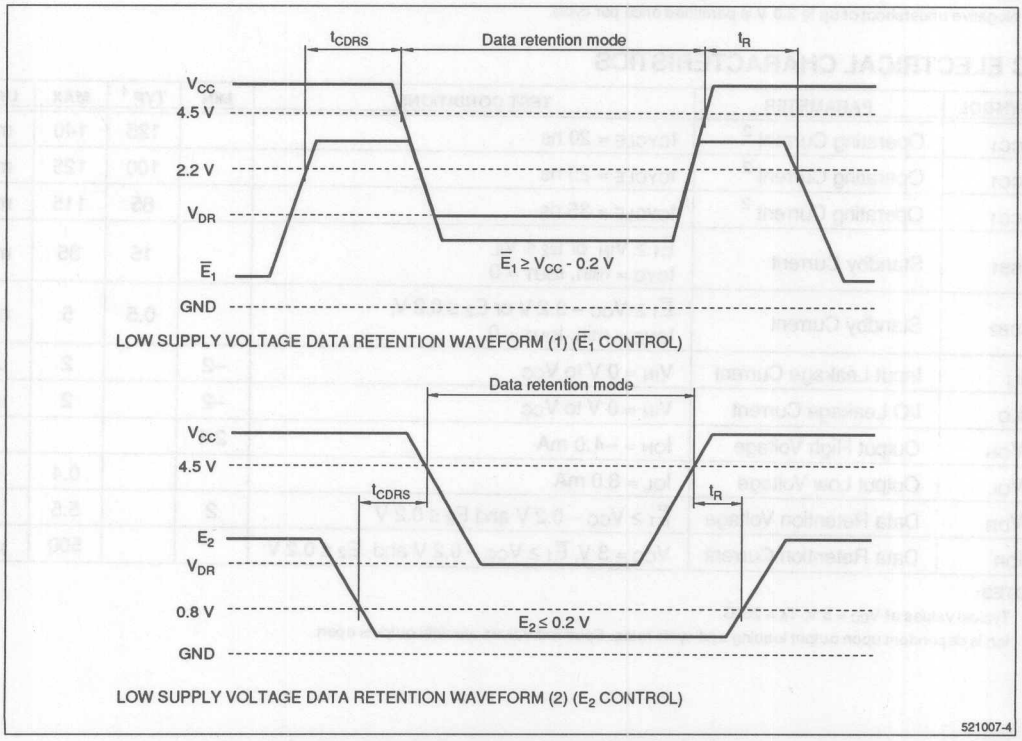


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	5		5		5		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	5		5		5		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		8		10		15	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		8		10		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [4]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [4]		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	12		15		20		ns
t_{AW}	Address Valid to End of Write	12		15		20		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	12		15		20		ns
t_{DW}	Input Data Setup Time	8		10		12		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]	0	8	0	10	0	15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	5		5		5		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Sample tested only.
4. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ and E_2 are HIGH, $\overline{E}_1$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}_1$ and E_2 are both active. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid data will be present following t_{GA} only if t_{EA} timing is met.

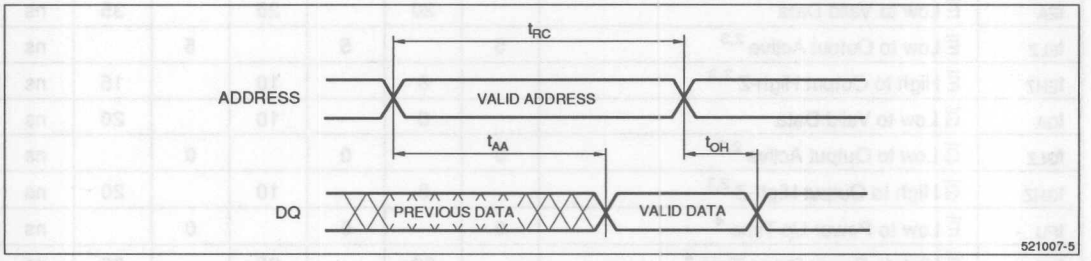


Figure 5. Read Cycle No. 1

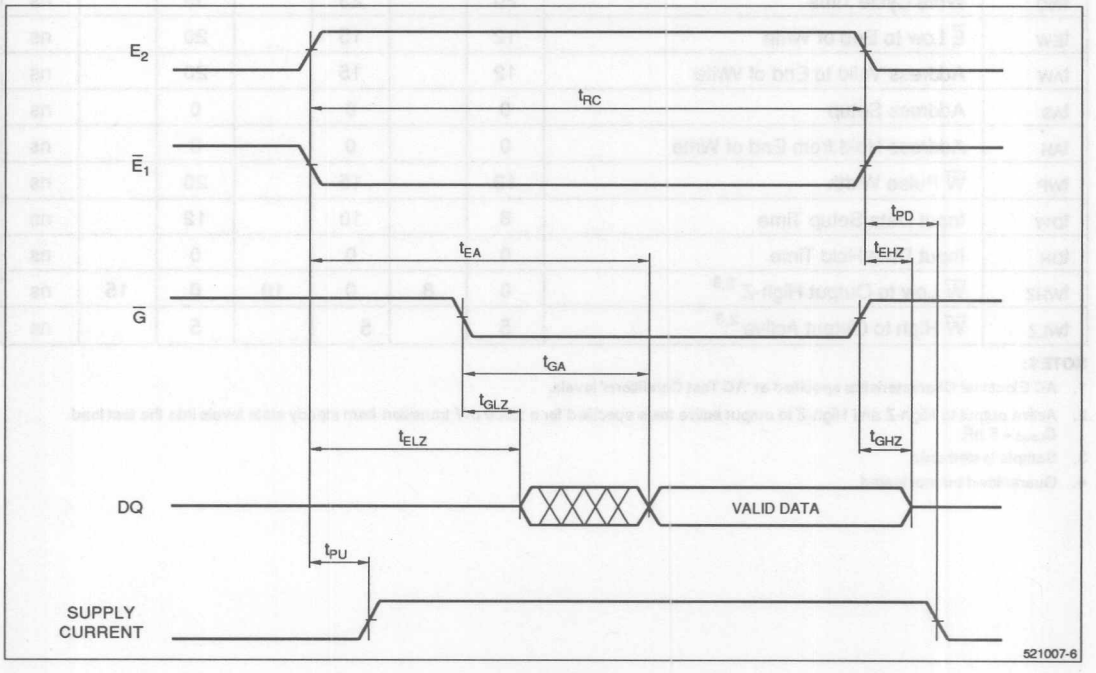


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when both $\overline{E}_1$ and E_2 are active. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}_1$ and $\overline{G}$ are LOW, E_2 is HIGH. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

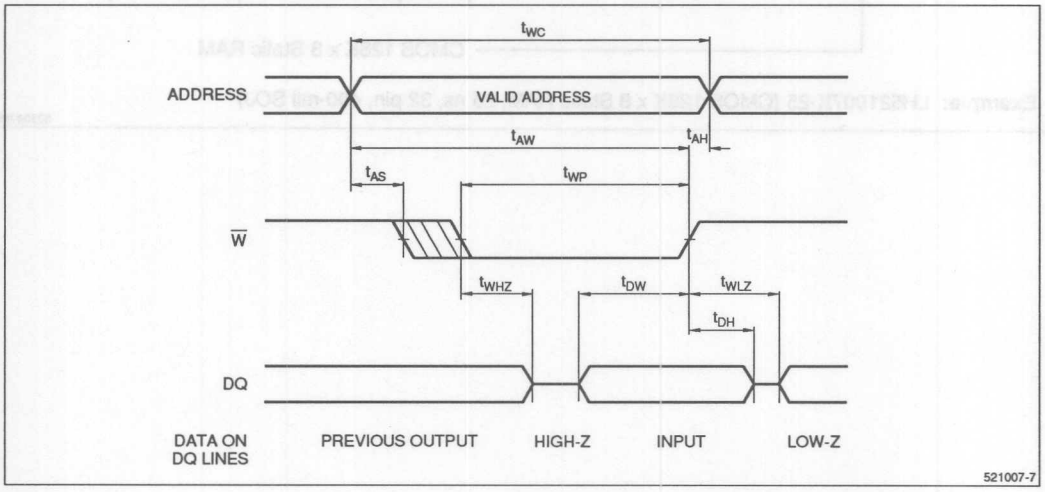


Figure 7. Write Cycle No. 1

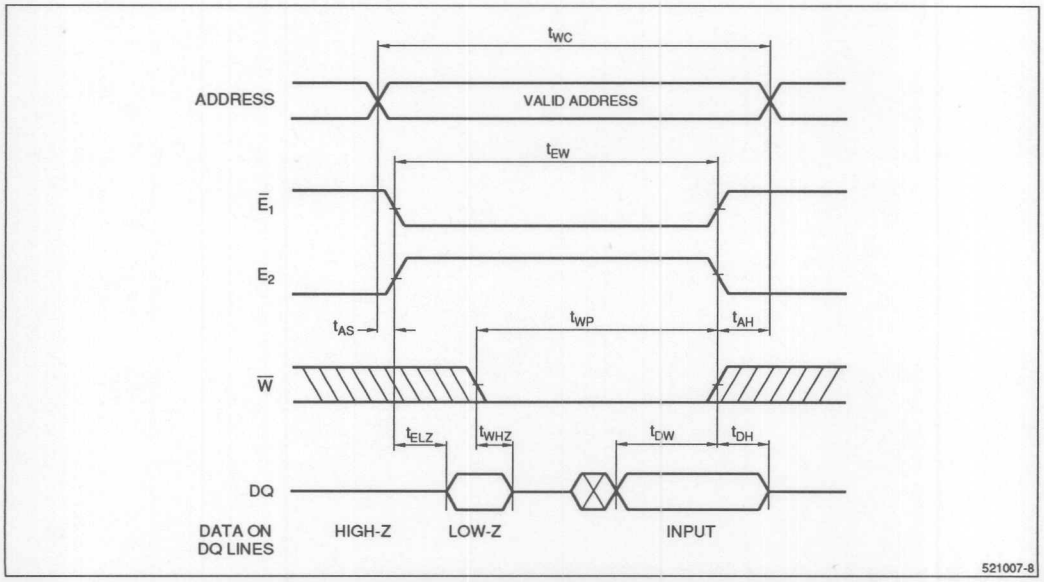
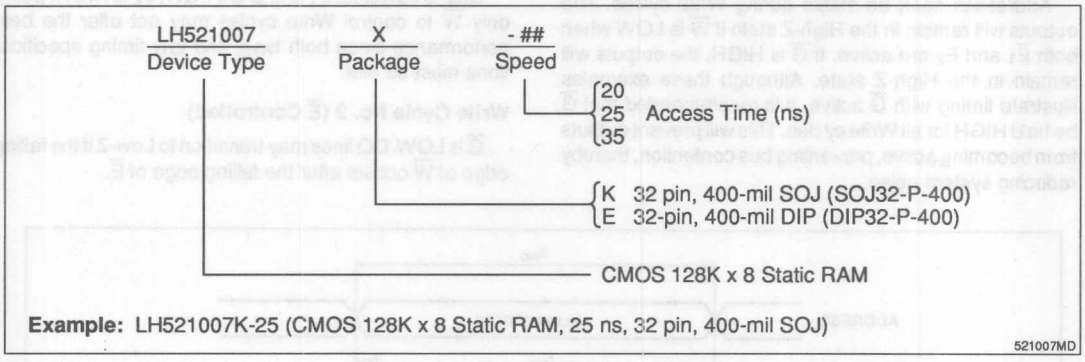


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH521008

CMOS 128K × 8 Static RAM

FEATURES

- Fast Access Times: 20/25/35 ns
- Low Power Standby when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- Fully Static Operation
- 2 V Data Retention
- JEDEC Standard Pinout
- Packages:
  32-Pin, 400-mil DIP
  32-Pin, 400-mil SOJ

FUNCTIONAL DESCRIPTION

The LH521008 is a high speed 1,048,576-bit static RAM organized as 128K × 8. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). Standby power drops to its lowest level (I_{SB1}) if $\overline{E}$ is raised to within 0.2 V of V_{CC}.

Write cycles occur when both Chip Enable ($\overline{E}$) and Write Enable ($\overline{W}$) are LOW. Data is transferred from the DQ pins to the memory location specified by the 17 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ is LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address.

High frequency design techniques should be employed to obtain the best performance from this device. Solid, low-impedance power and ground planes, with high frequency decoupling capacitors, are recommended. Series termination of the inputs should be considered when transmission line effects occur.

PIN CONNECTIONS

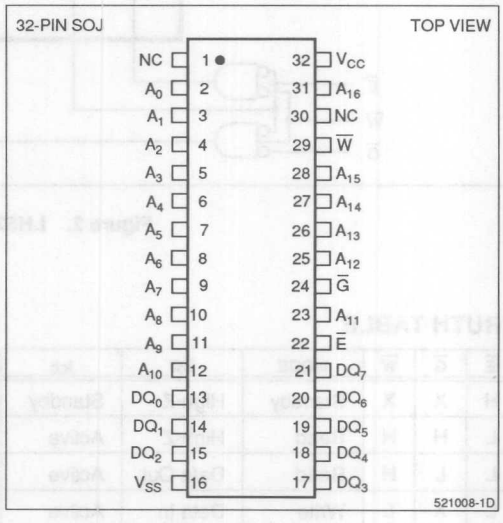


Figure 1. Pin Connections for DIP and SOJ Packages

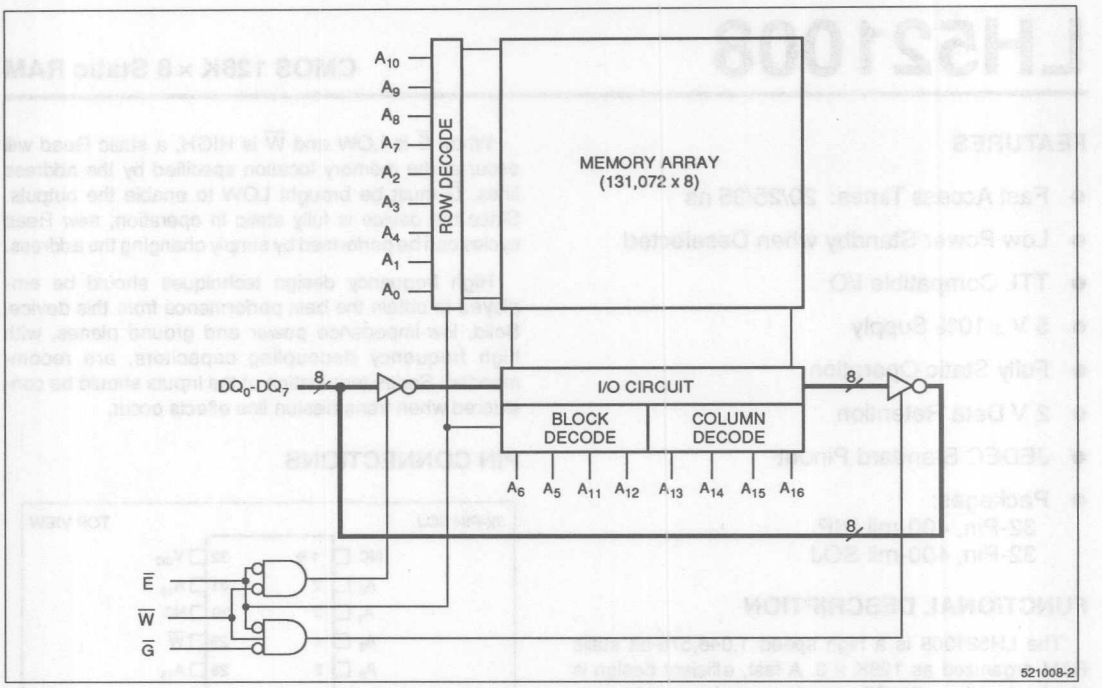


Figure 2. LH521008 Block Diagram

TRUTH TABLE

$\overline{E}$	$\overline{G}$	$\overline{W}$	MODE	DQ	I_{CC}
H	X	X	Standby	High-Z	Standby
L	H	H	Read	High-Z	Active
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	DESCRIPTION
$A_0 - A_{16}$	Address Inputs
$DQ_0 - DQ_7$	Data Inputs/Outputs
$\overline{E}$	Chip Enable input
$\overline{G}$	Output Enable input
$\overline{W}$	Write Enable input
V_{CC}	Positive Power Supply
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65° C to 150° C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP [1]	MAX	UNIT
I_{CC1}	Operating Current [2]	t_{CYCLE} = 20 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}		110	180	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 25 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}		100	180	mA
I_{CC1}	Operating Current [2]	t_{CYCLE} = 35 ns $\overline{E}$ = V_{IL}, $\overline{W}$ = V_{IL} or V_{IH}		80	150	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V		0.005	2	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$		8	20	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V
V_{DR}	Data Retention Voltage	$\overline{E} \geq V_{CC} - 0.2$ V	2		5.5	V
I_{DR}	Data Retention Current	V_{CC} = 3 V, $\overline{E} \geq V_{CC} - 0.2$ V			500	µA

NOTE:

1. Typical values at V_{CC} = 5 V, T_A = 25°C.
2. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

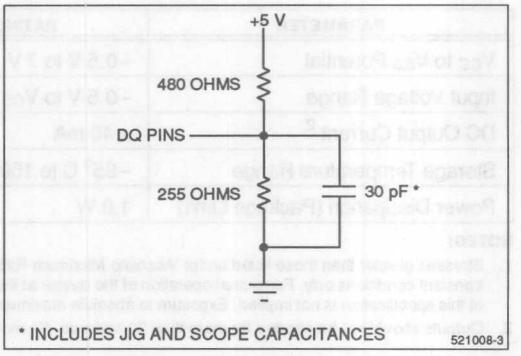


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	6 pF
C_{DQ} (I/O Capacitance)	8 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

DATA RETENTION TIMING

$\overline{E}$ must be held above the lesser of V_{IH} or V_{CC} – 0.2 V to assure proper operation when V_{CC} < 4.5 V. $\overline{E}$ must be V_{CC} – 0.2 V or greater to meet I_{DR} specification. All other inputs are 'Don't Care.'

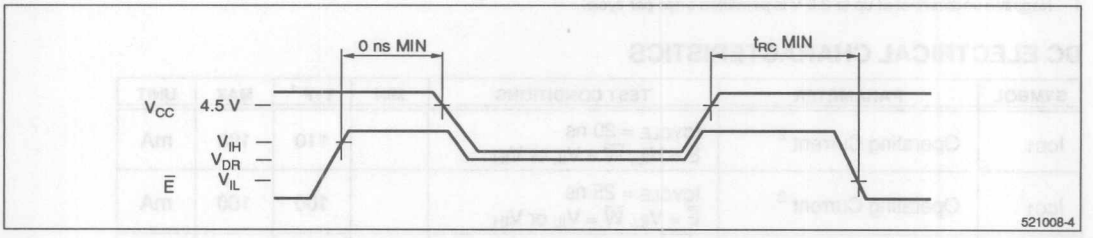


Figure 4. Data Retention Timing

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE								
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		8		10		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		8		10		20	ns
t_{PU}	$\overline{E}$ Low to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ High to Power Down Time [3]		20		25		35	ns
WRITE CYCLE								
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		25		ns
t_{DW}	Input Data Setup Time	12		15		15		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		15	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		3		3		ns

NOTES:

1. AC Electrical Characteristics specified at 'AC Test Conditions' levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$ is LOW and $\overline{G}$ is LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2

Chip is in Read Mode: $\overline{W}$ is HIGH. Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA} or t_{GA}, but may become valid as soon as t_{ELZ} or t_{GLZ}. Outputs will transition directly from High-Z to Valid Data Out. Valid data will be present when both t_{GA} and t_{EA} timing are met.

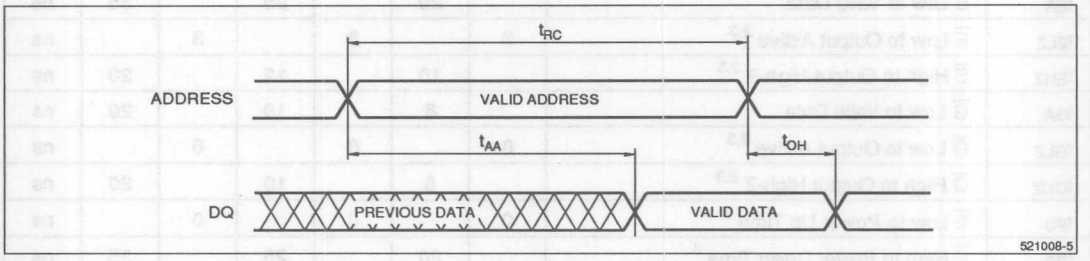


Figure 5. Read Cycle No. 1

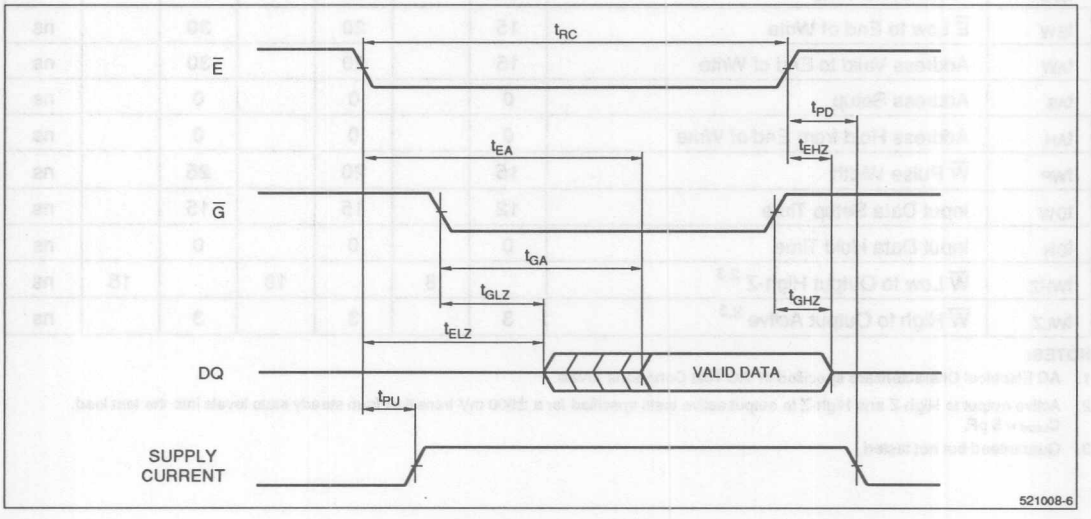


Figure 6. Read Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ goes LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 ($\overline{W}$ Controlled)

Chip is selected: $\overline{E}$ is LOW, $\overline{G}$ is LOW. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$.

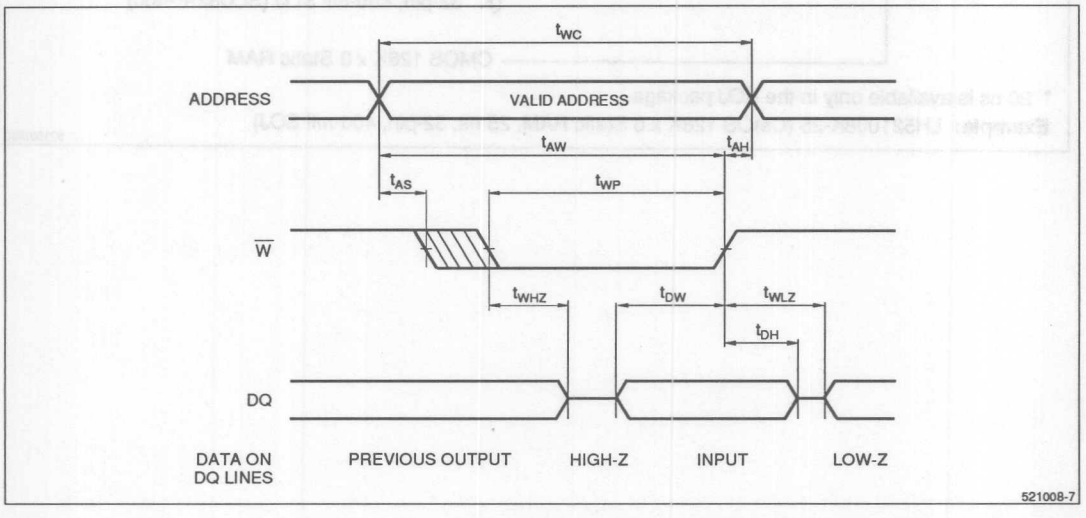


Figure 7. Write Cycle No. 1

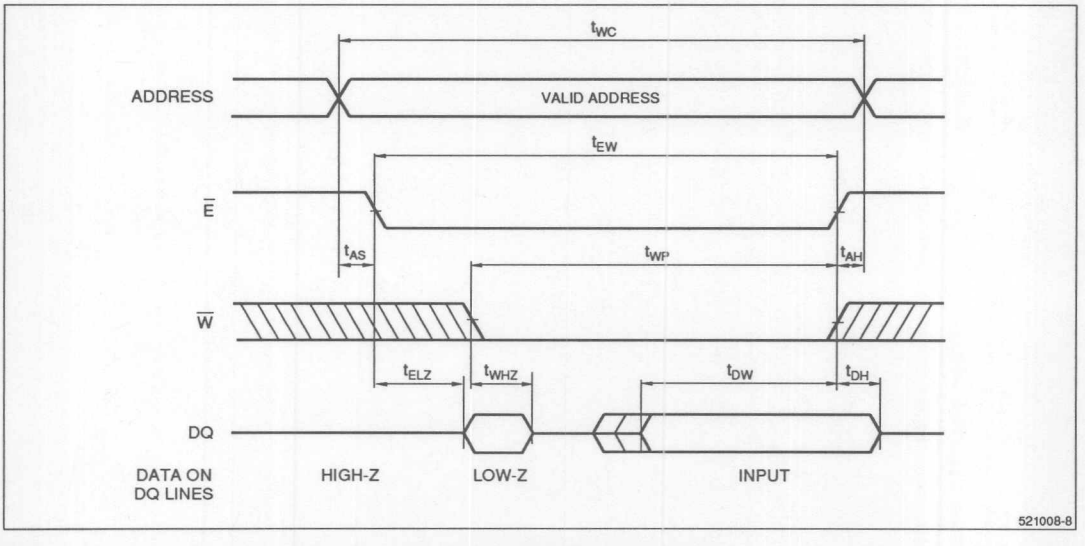
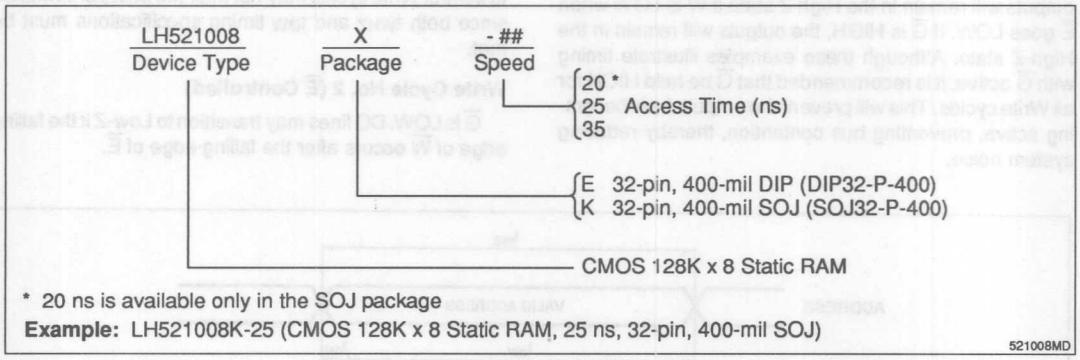


Figure 8. Write Cycle No. 2

ORDERING INFORMATION



LH521028

CMOS 64K × 18 Static RAM

FEATURES

- Fast Access Times: 20/25/35 ns
- Wide Word (18-Bits) for:
  - Improved Performance
  - Reduced Component Count
  - Nine-bit Byte for Parity
- Transparent Address Latch
- Reduced Loading on Address Bus
- Low Power Stand-by Mode when Deselected
- TTL Compatible I/O
- 5 V ± 10% Supply
- 2 V Data Retention
- JEDEC Standard Pinout
- Package:
  52-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH521028 is a high speed 1,179,648-bit CMOS SRAM organized as 64K × 18. A fast, efficient design is obtained with a CMOS periphery and a matrix constructed with polysilicon load memory cells. The LH521028 is available in a compact 52-Pin PLCC, which along with the six pairs of supply terminals, provide for reliable operation.

The control signals include Write Enable ($\overline{W}$), Chip Enable ($\overline{E}$), High and Low Byte Select ($\overline{S}_L$ and $\overline{S}_H$), Output Enable ($\overline{G}$) and Address Latch Enable (ALE). The wide word provides for reduced component count, improved density, reduced Address bus loading and improved performance. The wide word also allows for byte-parity with no additional RAM required.

This RAM is fully static in operation. The Chip Enable ($\overline{E}$) control permits Read and Write operations when active (LOW) or places the RAM in a low-power standby mode when inactive (HIGH). The Byte-select controls, $\overline{S}_H$ and $\overline{S}_L$, are also used to enable or disable Read and Write operations on the high and the low bytes. The Address Latches are transparent when ALE is HIGH (for applications not requiring a latch), and are latched when ALE is LOW. The Address Latches and the wide word help to eliminate the need for external Address bus buffers and/or latches.

Write cycles occur when Chip Enable ($\overline{E}$), $\overline{S}_H$ and/or $\overline{S}_L$, and Write Enable ($\overline{W}$) are LOW. The Byte-select signals can be used for Byte-write operations by disabling the other byte during the Write operation. Data is transferred from the DQ pins to the memory location specified by the 16 address lines. The proper use of the Output Enable control ($\overline{G}$) can prevent bus contention.

When $\overline{E}$ and either $\overline{S}_H$ or $\overline{S}_L$ are LOW and $\overline{W}$ is HIGH, a static Read will occur at the memory location specified by the address lines. $\overline{G}$ must be brought LOW to enable the outputs. Since the device is fully static in operation, new Read cycles can be performed by simply changing the address with ALE HIGH.

PIN CONNECTIONS

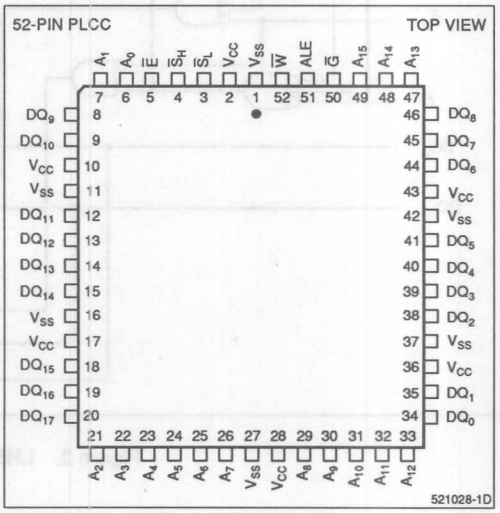


Figure 1. Pin Connections for PLCC Package

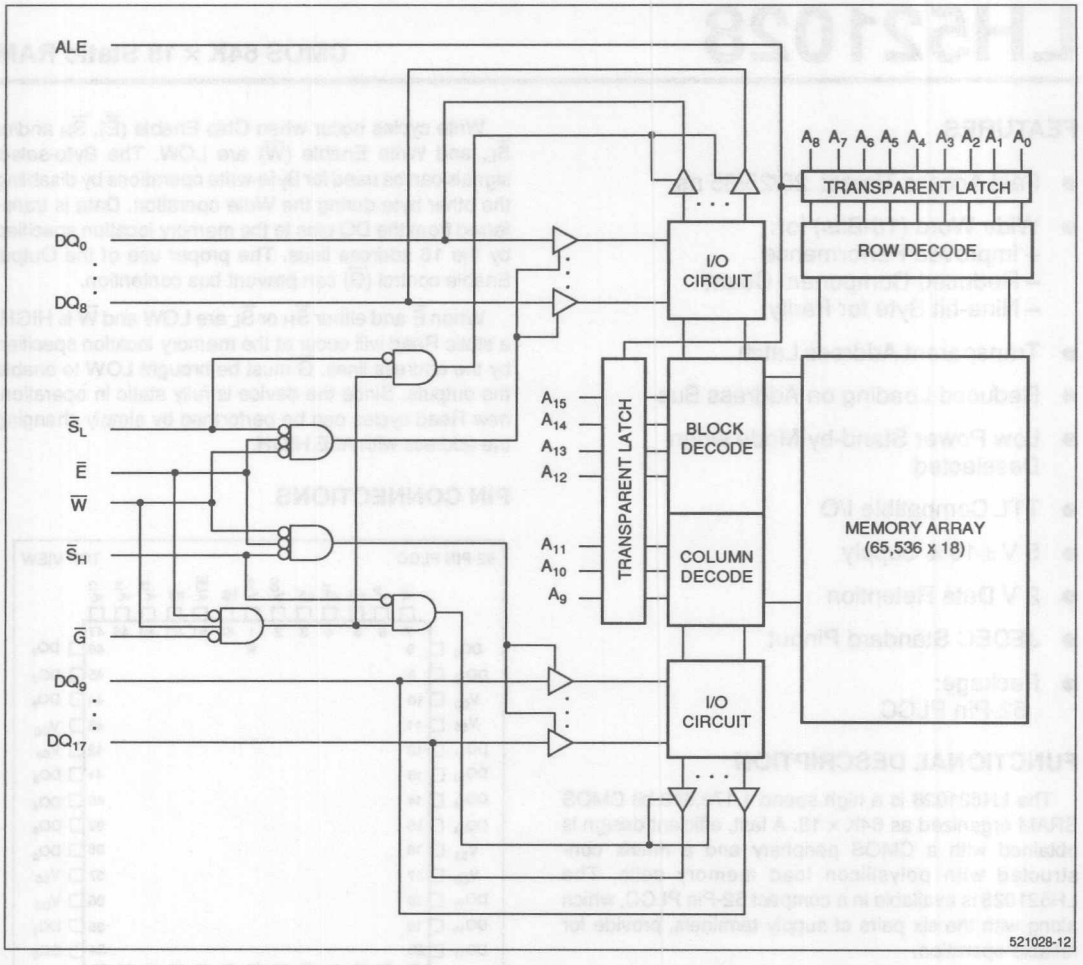


Figure 2. LH521028 Block Diagram

TRUTH TABLE

ADDRESS	$\overline{E}$	$\overline{S_H}$	$\overline{S_L}$	ALE	$\overline{G}$	$\overline{W}$	DQ_0-DQ_8	DQ_9-DQ_{17}	MODE	I_{CC}
Don't Care	H	X	X	H	X	X	High-Z	High-Z	Standby	I_{SB}
Valid	L	L	H	H	L	H	Active	High-Z	Read	I_{CC1}
Valid	L	H	L	H	L	H	High-Z	Active	Read	I_{CC1}
Valid	L	L	L	H	L	H	Active	Active	Read	I_{CC1}
Valid	L	L	L	H	H	H	High-Z	High-Z	Read	I_{CC1}
Don't Care	L	L	L	L	L	H	Data Out	Data Out	Read	I_{CC1}
Valid	L	L	H	H	X	L	Data In	Don't Care	Write, low byte	I_{CC1}
Valid	L	H	L	H	X	L	Don't Care	Data In	Write, high byte	I_{CC1}
Valid	L	L	L	H	X	L	Data In	Data In	Write, both bytes	I_{CC1}
Valid	L	H	H	H	X	L	Don't Care	Don't Care	Write, inhibited	I_{CC1}
Don't Care	L	L	L	L	X	L	Data In	Data In	Write, both bytes	I_{CC1}

NOTE:
X = Don't Care, L = LOW, H = HIGH

PIN DESCRIPTIONS

PIN	SIGNAL
1	V_{SS}
2	V_{CC}
3	$\overline{S_L}$
4	$\overline{S_H}$
5	$\overline{E}$
6	A_0
7	A_1
8	DQ_9
9	DQ_{10}
10	V_{CC}
11	V_{SS}
12	DQ_{11}
13	DQ_{12}

PIN	SIGNAL
14	DQ_{13}
15	DQ_{14}
16	V_{SS}
17	V_{CC}
18	DQ_{15}
19	DQ_{16}
20	DQ_{17}
21	A_2
22	A_3
23	A_4
24	A_5
25	A_6
26	A_7

PIN	SIGNAL
27	V_{SS}
28	V_{CC}
29	A_8
30	A_9
31	A_{10}
32	A_{11}
33	A_{12}
34	DQ_0
35	DQ_1
36	V_{CC}
37	V_{SS}
38	DQ_2
39	DQ_3

PIN	SIGNAL
40	DQ_4
41	DQ_5
42	V_{SS}
43	V_{CC}
44	DQ_6
45	DQ_7
46	DQ_8
47	A_{13}
48	A_{14}
49	A_{15}
50	$\overline{G}$
51	ALE
52	$\overline{W}$

PIN DEFINITIONS

V_{CC} Positive Supply Voltage Terminals

V_{SS} Reference Terminals

$A_0 - A_{15}$ Address Bus Input

The Address bus is decoded to select one 18-bit word out of the total 64K words for Read and Write operations.

$\overline{E}$ Chip Enable Active LOW Input

Chip Enable is used to enable the device for Read and Write operations. When HIGH, both Read and Write operations are disabled and the device is in a reduced power state. When LOW, a Read or Write operation is enabled.

$\overline{W}$ Write Enable Active LOW Input

Write Enable is used to select either Read or Write operations when the device is enabled. When Write Enable is HIGH and the device is Enabled, a Read operation is selected. When Write Enable is LOW and the device is enabled, a Write operation is selected. A Byte-write operation is available by using the Byte-select controls.

$\overline{S}_H$, $\overline{S}_L$ Select High Select Low Active LOW Inputs

The Select High and Select Low signals, in conjunction with the Chip Enable and Write Enable signals, allow the selection of the individual bytes for Read and Write operations. When High, the Select signal will deselect its byte and prevent Read or Write operations. When the Select signal is LOW and Chip Enable is LOW, a Read or Write operation is performed at the location determined by the contents of the Address bus. When Chip Enable is HIGH, the Select signals are Don't Care. Select Low ($\overline{S}_L$) is assigned to $DQ_0 - DQ_8$ and Select High ($\overline{S}_H$) is assigned to $DQ_9 - DQ_{17}$.

ALE Address Latch Enable Active High Input

The Address Latch Enable signal is used to control the Transparent latches on the Address bus. The Latches are transparent when HIGH and are latched when LOW. If not required, Address Latch Enable may be tied HIGH, leaving the Address bus in a transparent condition.

$DQ_0 - DQ_{17}$ Data Bus Input/Output

$DQ_0 - DQ_8$ comprise the Low byte, selected by $\overline{S}_L$, and $DQ_9 - DQ_{17}$ comprise the High Data byte, selected by $\overline{S}_H$. The Data Bus is in a high impedance input mode during Write operations and standby. The Data bus is in a low-impedance output mode during Read operations.

$\overline{G}$ Output Enable Active LOW Input

The Output Enable signal is used to control the output buffers on the Data Input/Output bus. When $\overline{G}$ is HIGH, all output buffers are forced to a high impedance condition. When $\overline{G}$ is LOW, the output buffers will become active only during a Read operation ($\overline{E}$ and $\overline{S}_H$ / $\overline{S}_L$ are LOW, $\overline{W}$ is HIGH).

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
V_{CC} to V_{SS} Potential	−0.5 V to 7 V
Input Voltage Range	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	2 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGES

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
T_A	Temperature, Ambient	0		70	°C
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{SS}	Supply Voltage	0	0	0	V
V_{IL}	Logic '0' Input Voltage [1]	−0.5		0.8	V
V_{IH}	Logic '1' Input Voltage	2.2		V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of up to 3.0 V is permitted once per cycle.

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC1}	Operating Current [1]	t_{CYCLE} = minimum			300	mA
I_{SB1}	Standby Current	$\overline{E} \geq V_{CC} - 0.2$ V $V_{IN} \geq V_{CC} - 0.2$ V or $V_{IN} \leq 0.2$ V f = 0			4	mA
I_{SB2}	Standby Current	$\overline{E} \geq V_{IH}$ t_{CYCLE} = minimum			50	mA
I_{LI}	Input Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
I_{LO}	I/O Leakage Current	V_{IN} = 0 V to V_{CC}	−2		2	µA
V_{OH}	Output High Voltage	I_{OH} = −4.0 mA	2.4			V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA			0.4	V

NOTE:

1. I_{CC} is dependent upon output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times	5 ns
Input and Output Timing Ref. Levels	1.5 V
Output Load, Timing Tests	Figure 3

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	5 pF
C_{DQ} (I/O Capacitance)	7 pF

NOTES:

1. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{Bias} = 0 V and V_{CC} = 5.0 V.
2. Guaranteed but not tested.

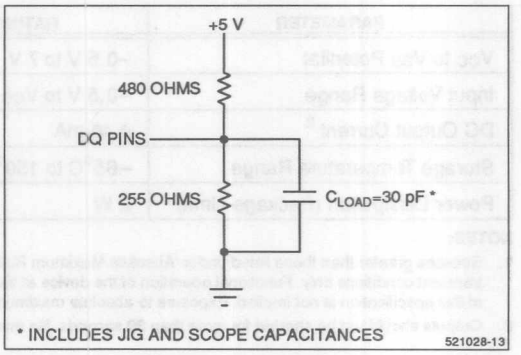


Figure 3. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	DESCRIPTION	-20		-25		-35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
	READ CYCLE							
t_{RC}	Read Cycle Timing	20		25		35		ns
t_{AA}	Address Access Time		20		25		35	ns
t_{ASL}	Address Setup to Latch Enable	3		3		3		ns
t_{AHL}	Address Hold from Latch Enable	5		6		6		ns
t_{LEA}	Latch Enable to Data Valid		22		27		37	ns
t_{LHM}	Latch Enable High Pulse Width	5		6		6		ns
t_{OH}	Output Hold from Address Change	3		3		3		ns
t_{LH}	Output Hold from Latch High	3		3		3		ns
t_{EA}	$\overline{E}$ Low to Valid Data		20		25		35	ns
t_{ELZ}	$\overline{E}$ Low to Output Active [2,3]	3		3		3		ns
t_{EHZ}	$\overline{E}$ High to Output High-Z [2,3]		10		12		20	ns
t_{SA}	$\overline{S}$ Low to Valid Data		10		12		20	ns
t_{SLZ}	$\overline{S}$ Low to Output Active [2,3]	2		3		3		ns
t_{SHZ}	$\overline{S}$ High to Output High-Z [2,3]		10		12		20	ns
t_{GA}	$\overline{G}$ Low to Valid Data		9		12		20	ns
t_{GLZ}	$\overline{G}$ Low to Output Active [2,3]	0		0		0		ns
t_{GHZ}	$\overline{G}$ High to Output High-Z [2,3]		8		10		20	ns
t_{RCS}	Read Setup from $\overline{W}$ High	0		0		0		ns
t_{RCH}	Read Hold from $\overline{W}$ Low	0		0		0		ns
t_{PU}	$\overline{E}$ LOW to Power Up Time [3]	0		0		0		ns
t_{PD}	$\overline{E}$ HIGH to Power Down Time [3]		20		25		35	ns
t_{WA}	Access Time From Write Enable HIGH		25		28		35	ns
	WRITE CYCLE							
t_{WC}	Write Cycle Time	20		25		35		ns
t_{EW}	$\overline{E}$ Low to End of Write	15		20		30		ns
t_{SW}	$\overline{S}$ LOW to End of Write	15		20		30		ns
t_{AW}	Address Valid to End of Write	15		20		30		ns
t_{AS}	Address Setup to Start of Write	0		0		0		ns
t_{AH}	Address Hold from End of Write	0		0		0		ns
t_{ASL}	Address Setup to Latch Enable	3		3		3		ns
t_{AHL}	Address Hold from Latch Enable	4		4		5		ns
t_{LHW}	Latch Hold from $\overline{W}$ High	0		0		0		ns
t_{LHM}	Latch Enable HIGH Pulse Width	5		6		6		ns
t_{WP}	$\overline{W}$ Pulse Width	15		20		30		ns
t_{DW}	Input Data Setup Time	12		13		15		ns
t_{DH}	Input Data Hold Time	0		0		0		ns
t_{WHZ}	$\overline{W}$ Low to Output High-Z [2,3]		8		10		14	ns
t_{WLZ}	$\overline{W}$ High to Output Active [2,3]	3		3		3		ns

NOTES:

1. AC Electrical Characteristics specified at "AC Test Conditions" levels.
2. Active output to High-Z and High-Z to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{Load} = 5 pF.
3. Guaranteed but not tested.

TIMING DIAGRAMS – READ CYCLE

Read Cycle No. 1: (Unlatched Address Controlled Read)

Chip is in Read Mode: ALE is HIGH (transparent mode), $\overline{E}$ and $\overline{G}$ are LOW. Read cycle timing is referenced from when all addresses are stable until the first address transition. Following a $\overline{W}$-controlled Write cycle, t_{WA} and t_{AA} must both be satisfied to ensure valid data. Cross-hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

Read Cycle No. 2: (Unlatched Chip Enable Controlled Read)

Chip is in Read Mode: ALE is HIGH (transparent mode). Read cycle timing is referenced from when $\overline{E}$, $\overline{S}$, and $\overline{G}$ are stable until the first address transition. Cross-hatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid.

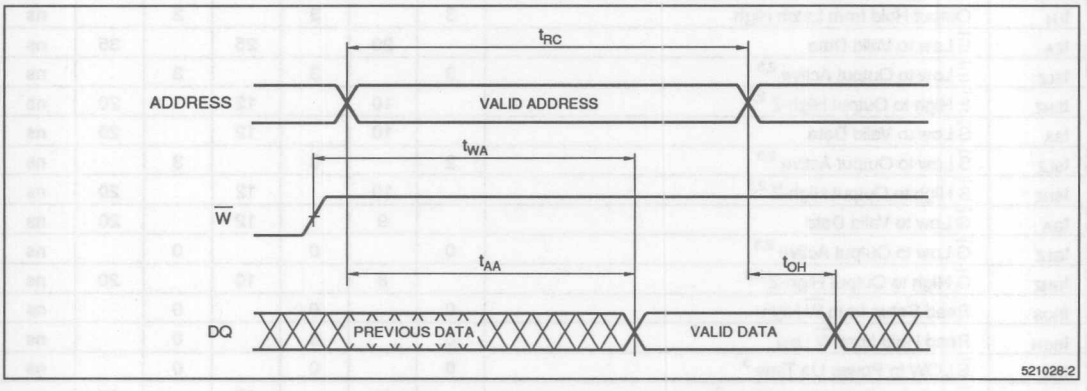


Figure 4. Read Cycle No. 1

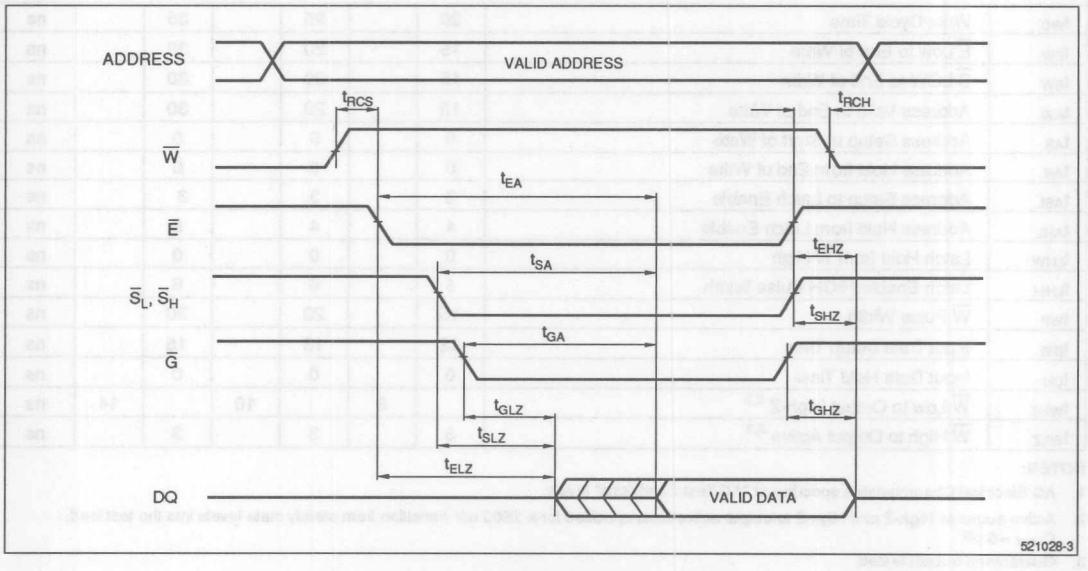


Figure 5. Read Cycle No. 2

TIMING DIAGRAMS – READ CYCLE (cont'd)

Read Cycle No. 3 (Latched Address Controlled Read)

Chip is in Read Mode: $\overline{W}$ is HIGH, $\overline{E}$, $\overline{S}_H$, $\overline{S}_L$ and $\overline{G}$ are LOW. Both t_{AA} and t_{LEA} must be met before valid data is available. If the address is valid prior to the rising edge of ALE, then the access time is t_{LEA}. If the address is valid after ALE is HIGH (or if ALE is tied HIGH) then the access time is t_{AA}. Crosshatched portion of Data Out implies that data lines are in the Low-Z state but the data is not guaranteed to be valid until t_{AA}.

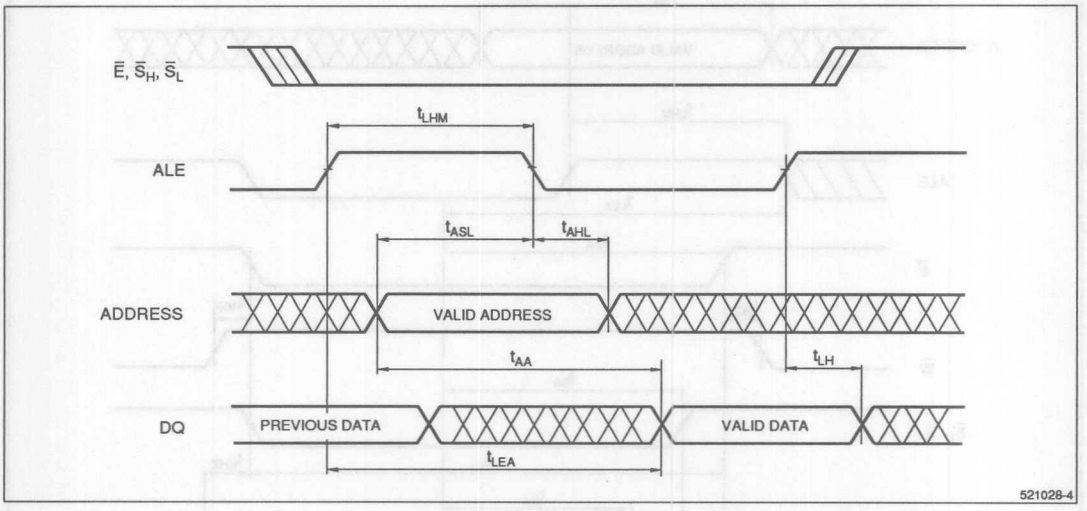


Figure 6. Read Cycle No. 3

TIMING DIAGRAMS – READ CYCLE (cont'd)

Read Cycle No. 4

Chip is in Read Mode: Timing illustrated for the case when addresses are valid before $\overline{E}$ goes LOW. Data Out is not specified to be valid until t_{EA}, t_{SA} and t_{GA}, but may become active as early as t_{ELZ}, t_{SLZ} or t_{GLZ}.

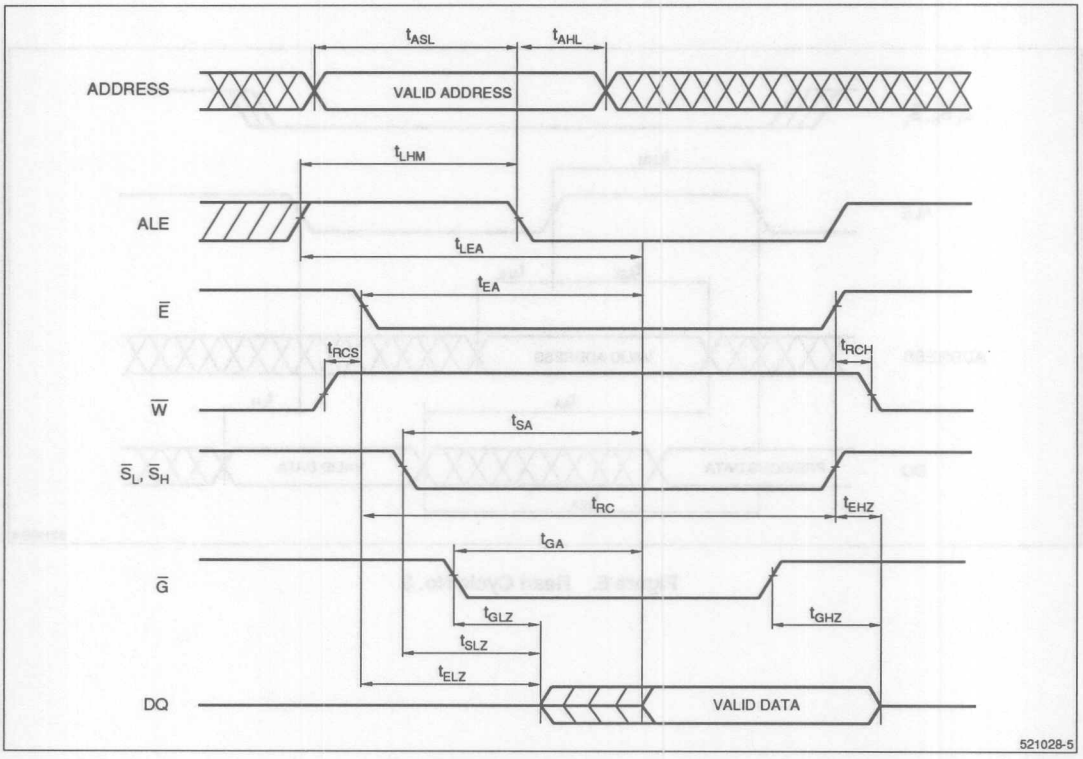


Figure 7. Read Cycle No. 4

TIMING DIAGRAMS – WRITE CYCLE

Addresses must be stable during unlatched Write cycles. The outputs will remain in the High-Z state if $\overline{W}$ is LOW when $\overline{E}$ and $\overline{S}_H$ / $\overline{S}_L$ go LOW. If $\overline{G}$ is HIGH, the outputs will remain in the High-Z state. Although these examples illustrate timing with $\overline{G}$ active, it is recommended that $\overline{G}$ be held HIGH for all Write cycles. This will prevent the LH521028's outputs from becoming active, preventing bus contention, thereby reducing system noise.

Write Cycle No. 1 (Unlatched $\overline{W}$ Controlled Write)

Chip is selected: $\overline{E}$, $\overline{G}$, and $\overline{S}_H$ / $\overline{S}_L$ are LOW, ALE is High. Using only $\overline{W}$ to control Write cycles may not offer the best performance since both t_{WHZ} and t_{DW} timing specifications must be met.

Write Cycle No. 2 ($\overline{E}$, $\overline{S}_L$, $\overline{S}_H$ Controlled Write)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edge of $\overline{E}$, $\overline{S}_H$/$\overline{S}_L$ if $\overline{G}$ is LOW.

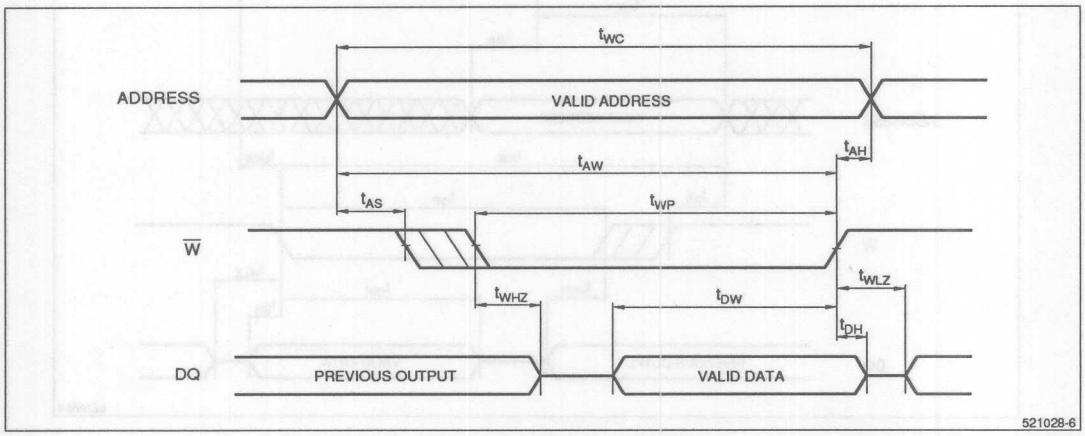


Figure 8. Write Cycle No. 1

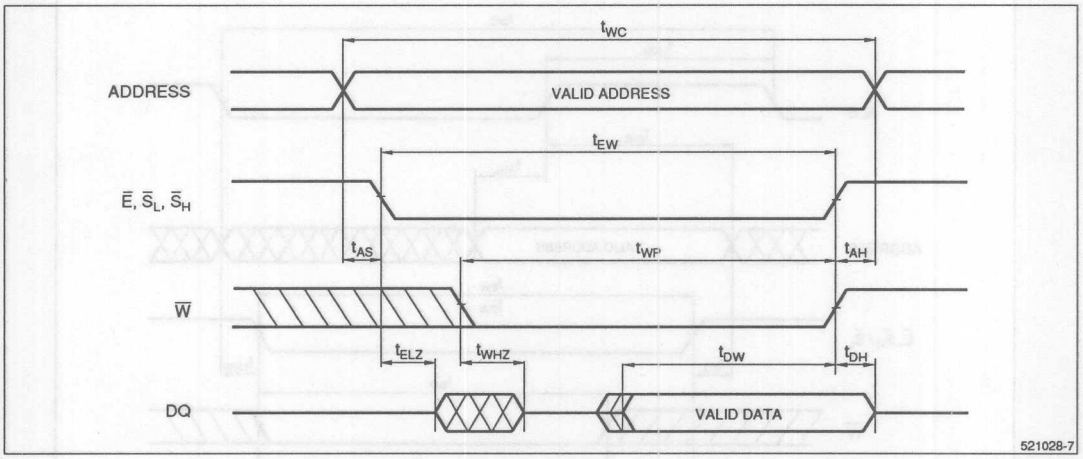


Figure 9. Write Cycle No. 2

TIMING DIAGRAMS – WRITE CYCLE (cont'd)

Write Cycle No. 3 (Latched $\overline{W}$ Controlled Write)

Chip is selected: $\overline{E}$, $\overline{G}$, and $\overline{S}_H$ / $\overline{S}_L$ are LOW.

Write Cycle No. 4 ($\overline{E}$ Controlled)

$\overline{G}$ is LOW. DQ lines may transition to Low-Z if the falling edge of $\overline{W}$ occurs after the falling edges of $\overline{E}$ and $\overline{S}_H/\overline{S}_L$.

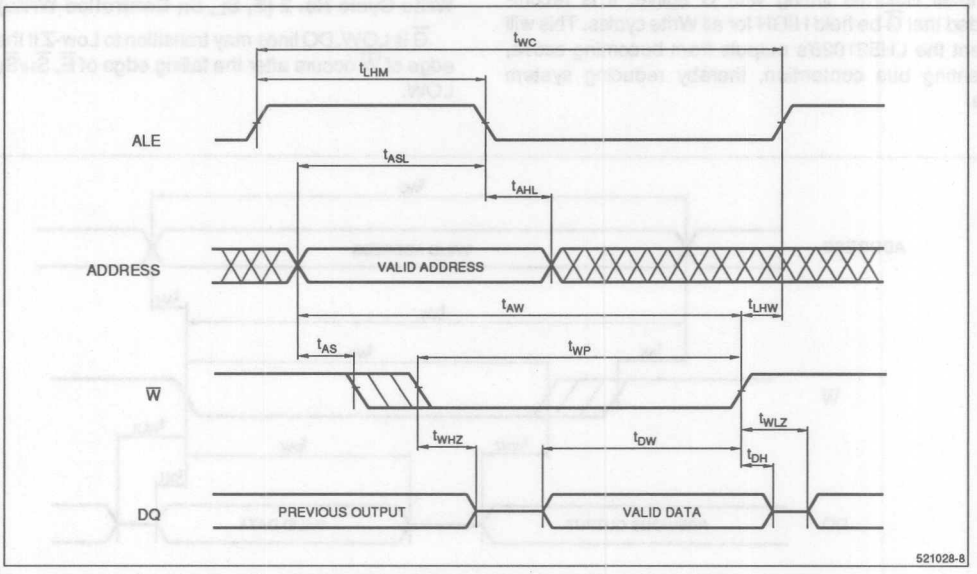


Figure 10. Write Cycle No. 3

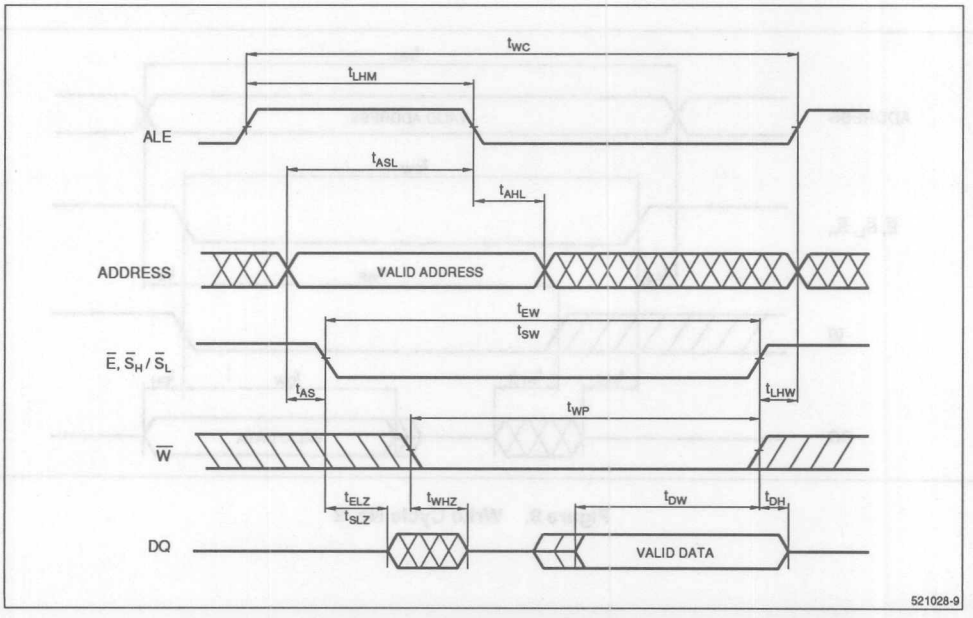


Figure 11. Write Cycle No. 4

BYTE OPERATIONS

Byte Read Description (Figure 12)

To read individual bytes, the device must be enabled ($\overline{E}$ is LOW), $\overline{W}$ must be HIGH, the outputs must be enabled ($\overline{G}$ is LOW) and the addresses must be either stable or latched with ALE. Figure 12 is one example of the byte read capabilities of this device. The example shows two read operations. The first is a read of the high byte of the current memory location and the second is a read of the low byte of the memory location.

(1) At the beginning of the cycle both $\overline{S}_L$ and $\overline{S}_H$ are HIGH.

(2) $\overline{S}_H$ goes LOW initiating a Read on the upper byte $DQ_{H(9\text{-}17)}$. $\overline{S}_L$ remains HIGH keeping the lower byte $DQ_{L(0\text{-}8)}$ disabled and in a high-impedance mode.

(3) $\overline{S}_L$ goes LOW activating $DQ_{L(0\text{-}8)}$. Valid data is available in t_{SA} following $\overline{S}_L$ going LOW.

(4) When $\overline{S}_H$ goes HIGH, $DQ_{H(9\text{-}17)}$ remains valid for t_{SHZ} before returning to a high-impedance condition.

(5) Finally, the Read for the lower byte is terminated by deasserting $\overline{S}_L$ (HIGH). $DQ_{L(0\text{-}8)}$ remains active for t_{SHZ} following $\overline{S}_L$ going HIGH.

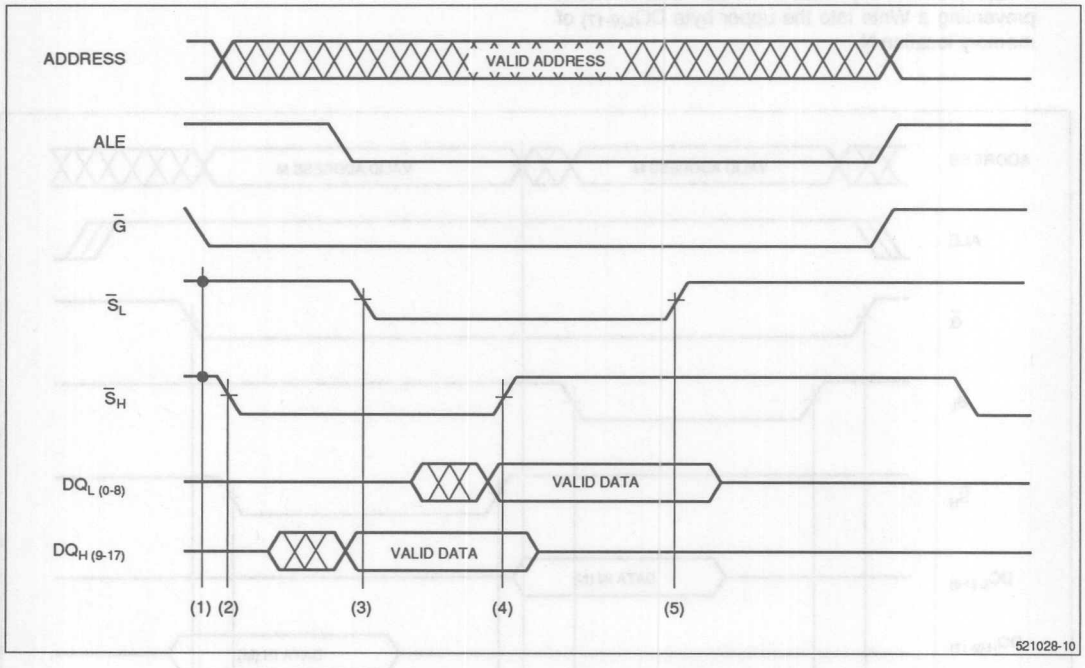


Figure 12. Byte Read: ($\overline{E}$ is LOW and $\overline{W}$ is HIGH)

BYTE OPERATIONS (cont'd)

Byte Write Description (Figure 13)

To do individual byte-write operations, the device must be enabled ($\overline{E}$ is LOW, $\overline{G}$ is don't care) and addresses must be either stable or latched. Figure 13 is one example of the byte-write capabilities of this device. The diagram shows two write operations with unlatched addresses. The first is a write to the low byte of memory location N and the second is a write to the high byte of memory location M.

(1) $\overline{W}$ goes LOW while $\overline{S}_L$ and $\overline{S}_H$ remain HIGH.

(2) $\overline{S}_L$ goes LOW initiating a Write into the lower byte $DQ_{L(0-8)}$ of memory location N. $\overline{S}_H$ remains HIGH preventing a Write into the upper byte $DQ_{L(9-17)}$ of memory location N.

(3) $\overline{S}_L$ now goes HIGH terminating the Write operation on the lower byte of memory location N.

(4) Address N is changed to M.

(5) The Write operation is now initiated on the upper byte $DQ_{H(9-17)}$ by bringing $\overline{S}_H$ LOW. $\overline{S}_L$ remains HIGH preventing a Write operation from occurring in the lower byte $DQ_{L(0-8)}$ of memory location N+ 1.

(6) $\overline{S}_H$ now goes HIGH terminating the Write operation on the upper byte of address M.

(7) $\overline{W}$ goes HIGH, ending the Write operation.

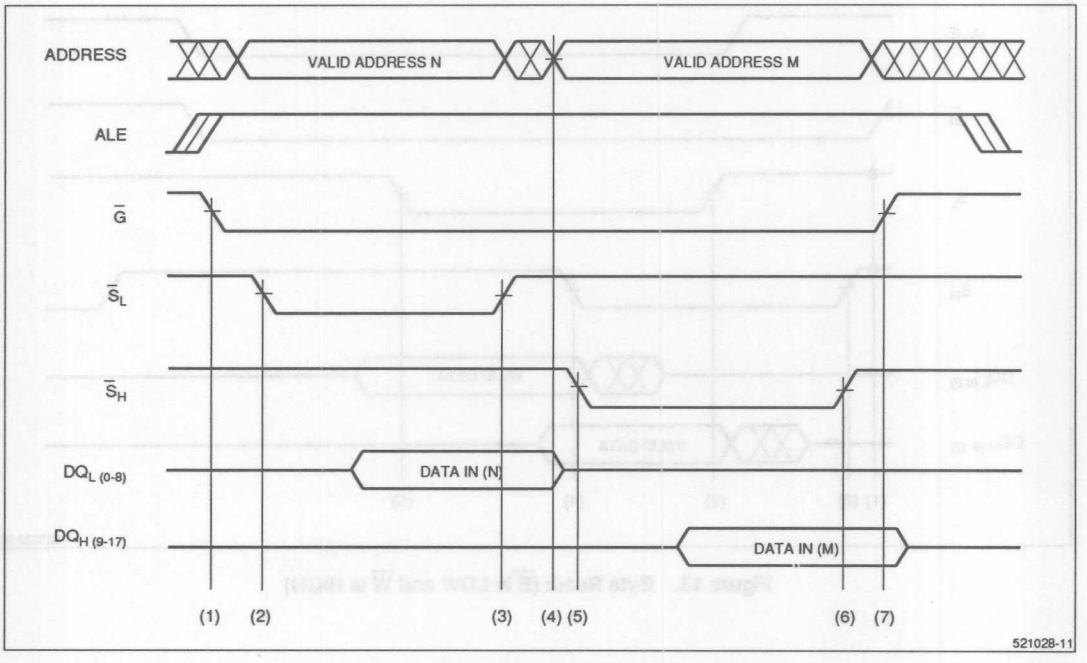
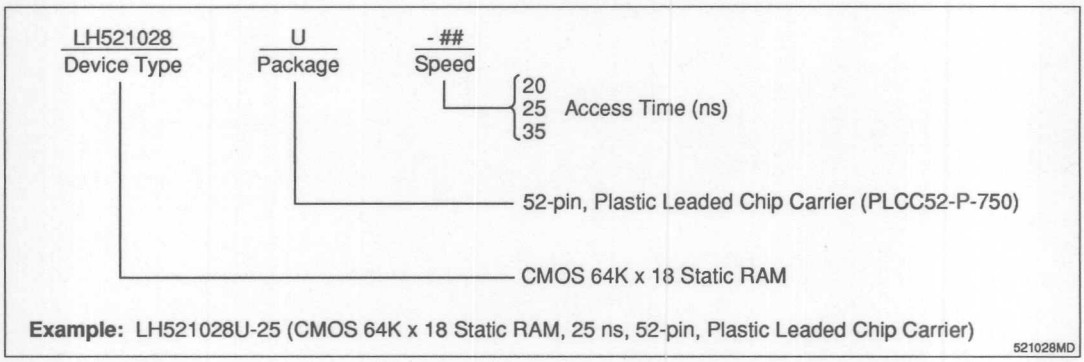


Figure 13. Byte Write: ($\overline{E}$ is LOW)

ORDERING INFORMATION



GENERAL INFORMATION – 1

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PACKAGING – 7

MASK-PROGRAMMABLE ROMs

	Density	Organization	Page
LH53259	256K	32K × 8	4-1
LH53515	512K	64K × 8	4-7
LH53H1000	1M	64K × 16	4-13
LH53H0900	1M	128K × 8	4-18
LH530800A	1M	128K × 8	4-23
LH531000B	1M	128K × 8	4-29
LH532000B	2M	256K × 8/128K × 16	4-35
LH532100B	2M	256K × 8	4-40
LH534000B	4M	512K × 8/256K × 16	4-44
LH534100B	4M	512K × 8	4-49
LH534500A	4M	512K × 8/256K × 16	4-54
LH534600	4M	512K × 8/256K × 16	4-60
LH538000	8M	1M × 8/512K × 16	4-65
LH538100	8M	1M × 8	4-71
LH538500A	8M	1M × 8/512K × 16	4-76
LH5316000	16M	2M × 8/1M × 16	4-83
LH5316500	16M	2M × 8/1M × 16	4-89
LH5332000	32M	4M × 8/2M × 16	4-95

LH53259

CMOS 256K (32K × 8) Mask-Programmable ROM

FEATURES

- 32,768 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 110 mW (MAX.)
  Standby: 82.5 µW (MAX.)
- Programmable output enable
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  44-pin, 10 × 10 mm^2 QFP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH53259 is a mask-programmable ROM organized as 32,768 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

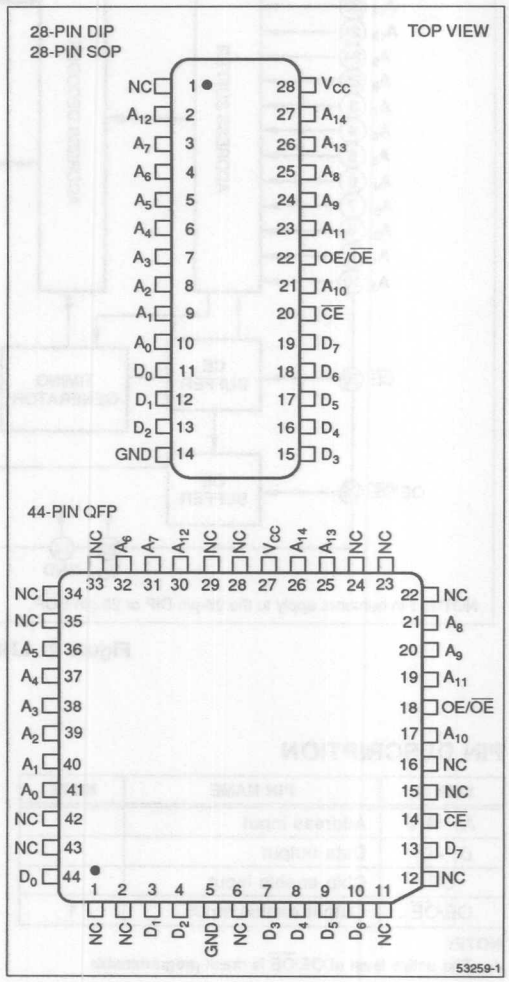


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

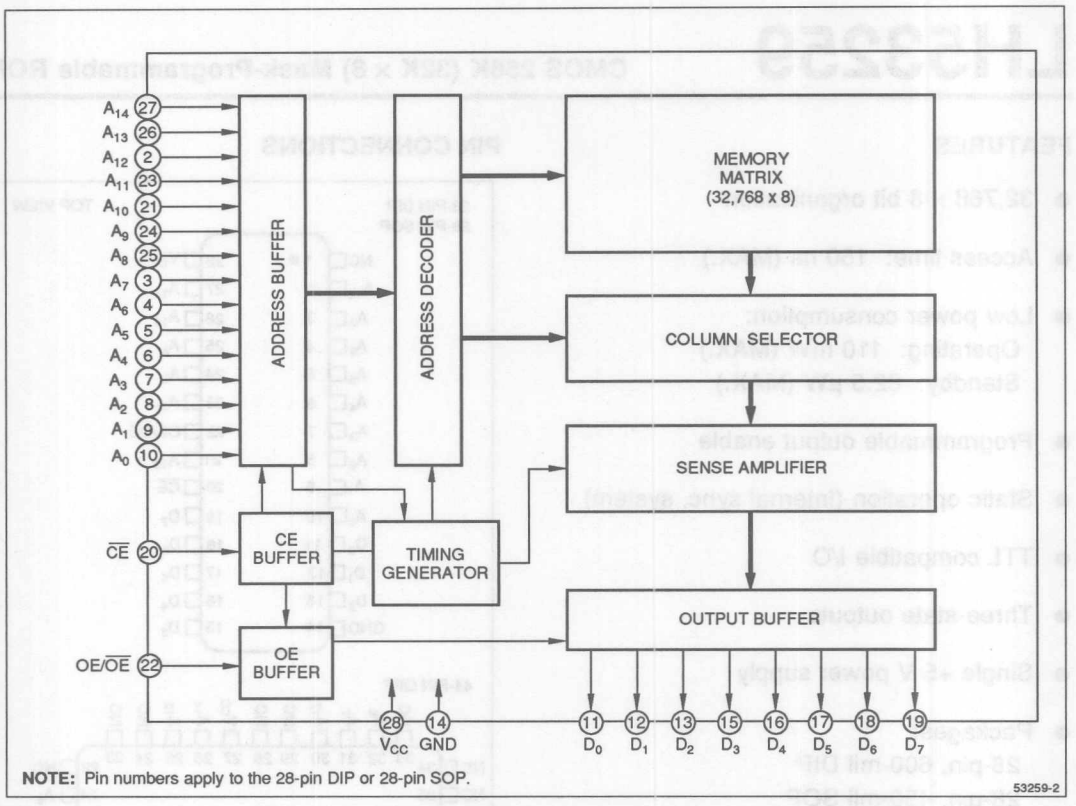


Figure 2. LH53259 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{14}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip enable input	
OE/$\overline{OE}$	Output enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	
NC	Non connection	

NOTE:
1. The active level of OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	Non selected	High-Z	Standby	1
L	L/H			Operating	
	H/L	Selected	D_{OUT}		

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			20	mA	2
	I_{CC2}	t_{RC} = 1 µs			15		
	I_{CC3}	t_{RC} = 150 ns			15	mA	3
	I_{CC4}	t_{RC} = 1 µs			10		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			15	µA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH} or OE = VIL
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
$\overline{CE}$ to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

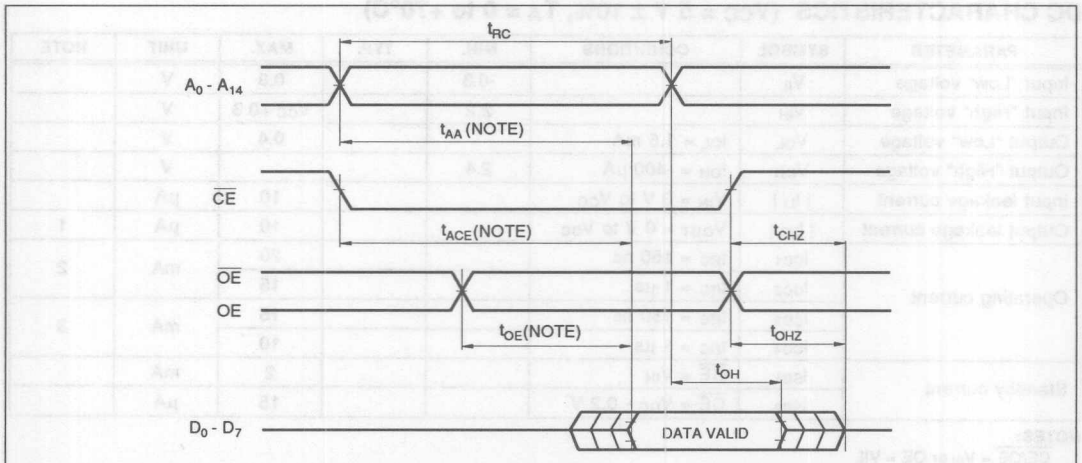
NOTE:
1. This is the time required for the output to become high impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTE: Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address inputs, chip enable and output enable, respectively have been met.

Figure 3. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

To ensure valid data immediately after power up and once the supply is stable, perform one of the following operations:

1. If the Chip Enable ($\overline{CE}$) was high during power up, switch the $\overline{CE}$ input from HIGH to LOW. (t_{ACE}) or
2. Change one or more addresses if the $\overline{CE}$ input was LOW at power up. (t_{AA})

The valid data will be output at t_{ACE} or t_{AA} following a transition from the above operations (1) or (2).

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

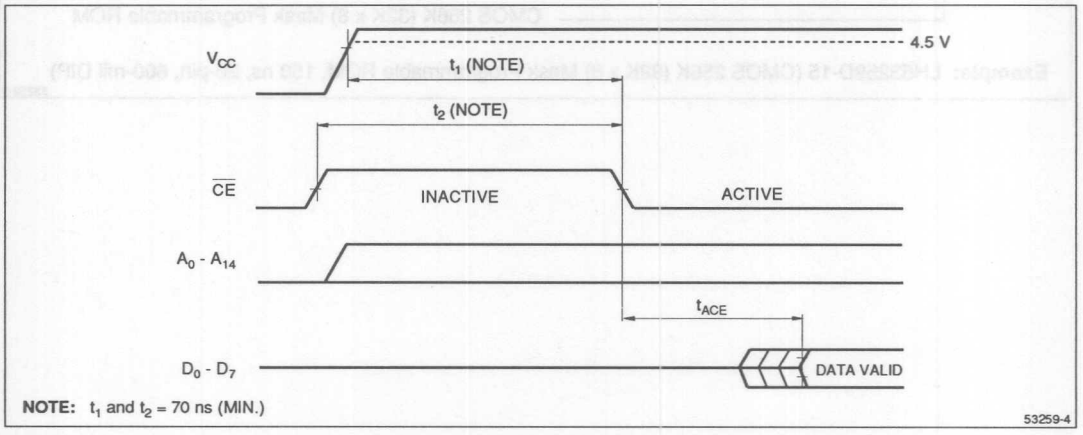


Figure 4. Power On With $\overline{CE}$ Inactive

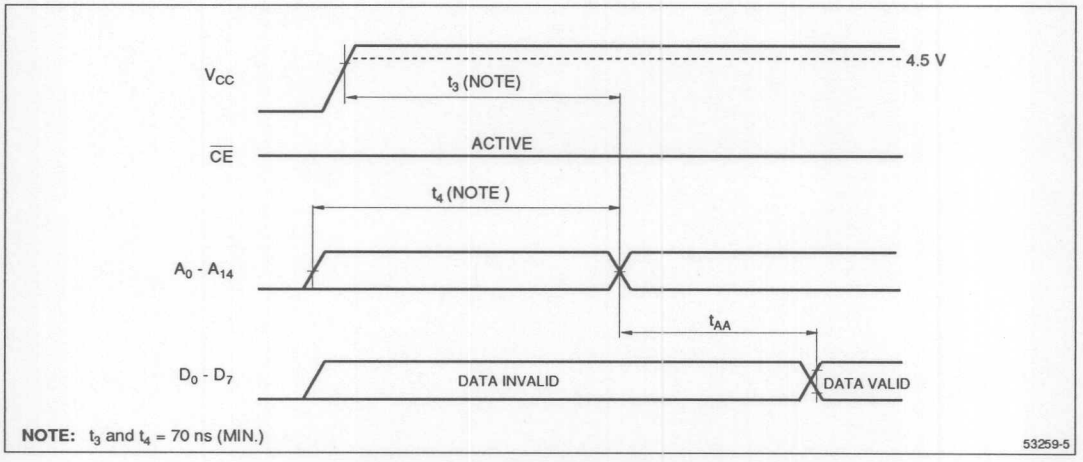
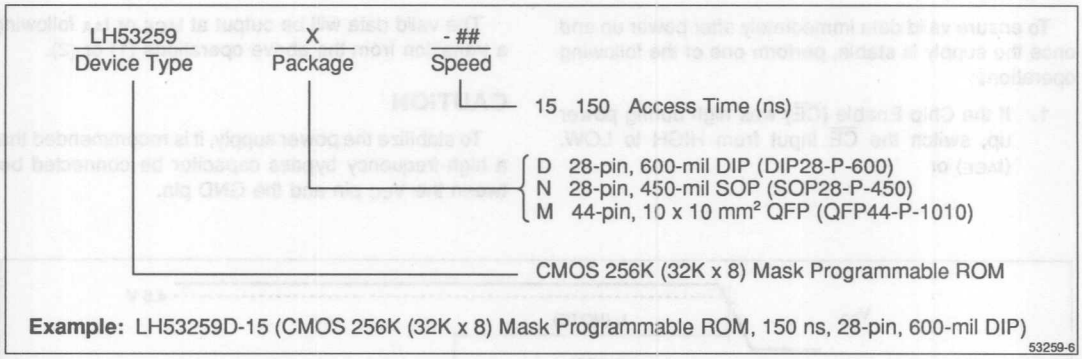


Figure 5. Power On With $\overline{CE}$ Active

ORDERING INFORMATION



Example: LH53259D-15 (CMOS 256K (32K x 8) Mask Programmable ROM, 150 ns, 28-pin, 600-mil DIP)

53259-6

LH53515

CMOS 512K (64K × 8) Mask-Programmable ROM

FEATURES

- 65,536 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 195 mW (MAX.)
  Standby: 550 µW (MAX.)
- Programmable output enable
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  32-pin, 525-mil SOP
  44-pin, 10 × 10 mm^2 QFP
- JEDEC standard EPROM pinout (DIP)

PIN CONNECTIONS

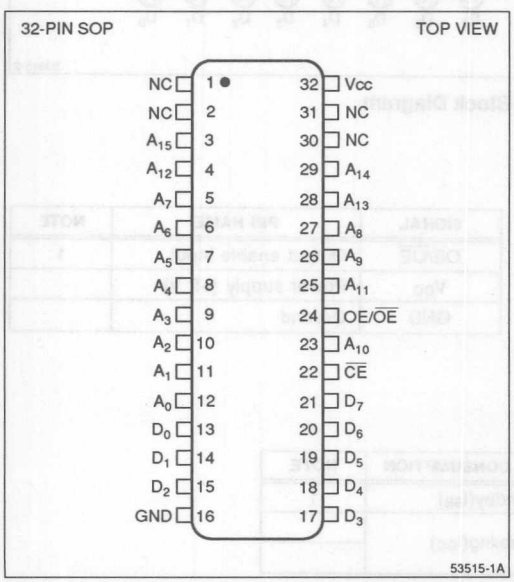


Figure 1. Pin Connections for SOP Package

DESCRIPTION

The LH53515 is a mask-programmable ROM organized as 65,536 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

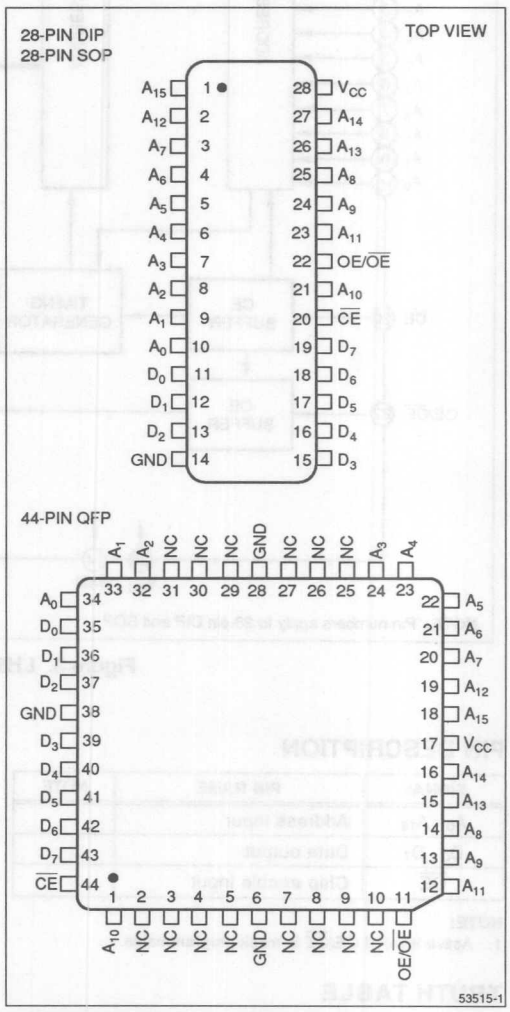


Figure 2. Pin Connections for DIP, SOP, and QFP Packages

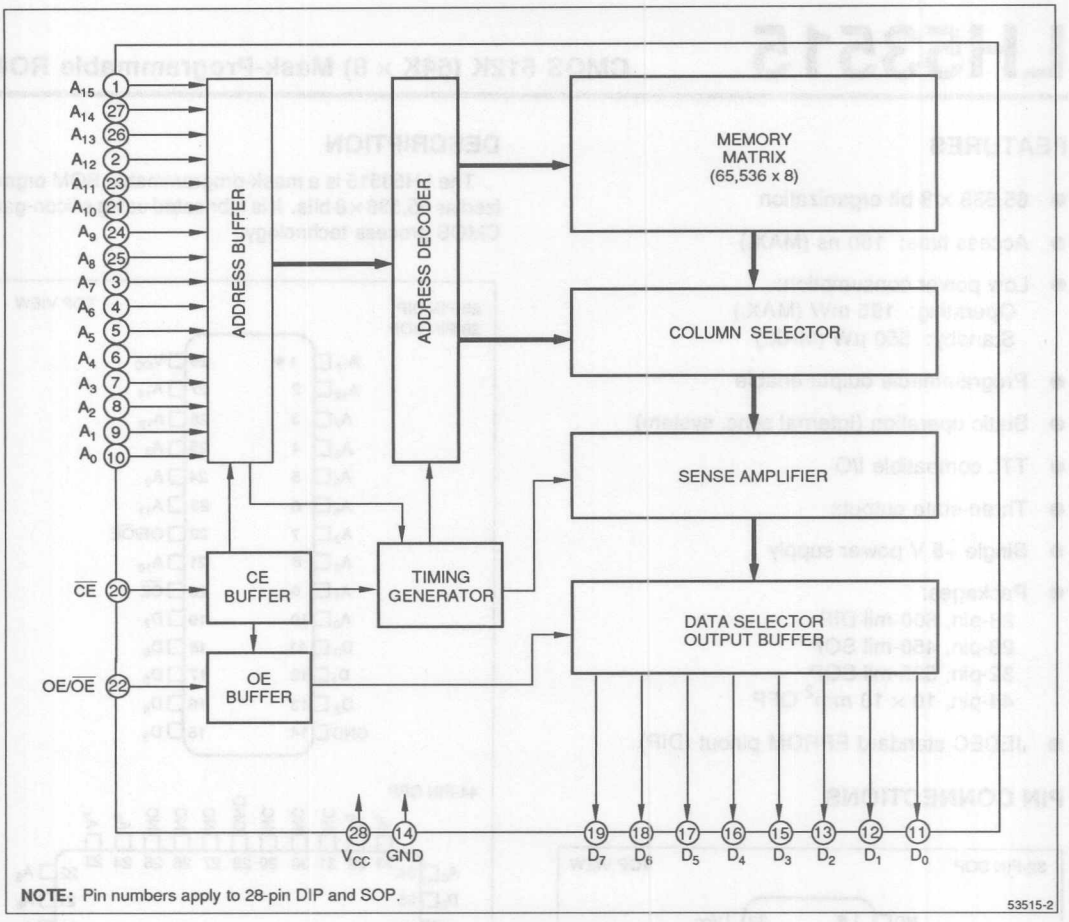


Figure 3. LH53515 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{15}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active level of OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	CURRENT CONSUMPTION	NOTE
H	X	Non selected	High-Z	Standby(I_{SB})	1
L	L/H			Operating(I_{CC})	
	H/L	Selected	D_{OUT}		

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	1
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	1
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE = V_{IL} or $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}		150			ns	
Address access time	t_{AA}				150	ns	
Chip enable access time	t_{ACE}				150	ns	
Output enable time	t_{OE}		10		80	ns	
Output hold time	t_{OH}		5			ns	
$\overline{CE}$ to output in High-Z	t_{CHZ}				70	ns	1
OE to output in High-Z	t_{OHZ}				70	ns	1

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

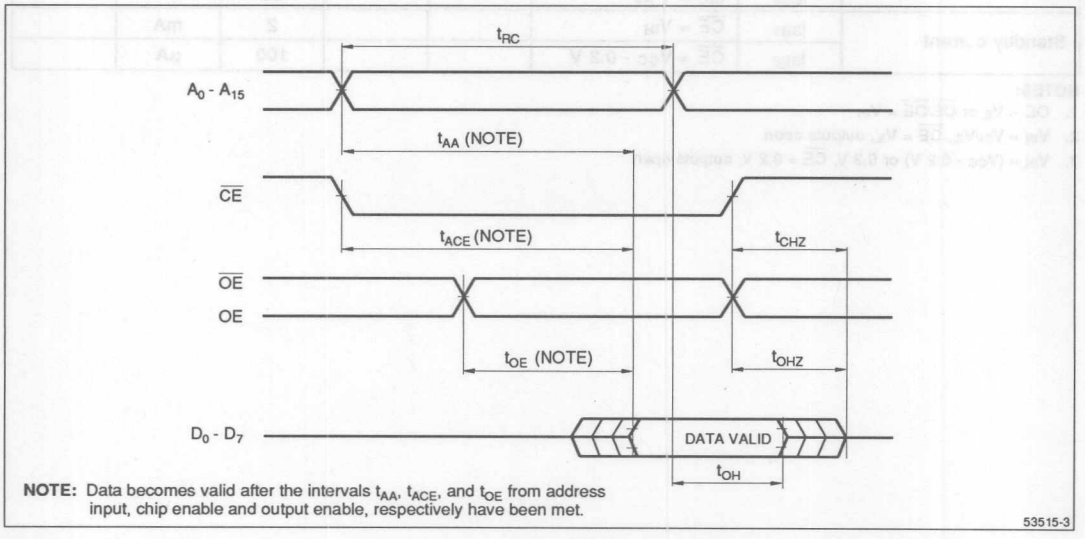


Figure 4. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

To ensure valid data immediately after power up and once the supply is stable, perform one of the following operations:

1. If the Chip Enable ($\overline{CE}$) was high during power up, switch the $\overline{CE}$ input from HIGH to LOW. (t_{ACE}) or
2. Change one or more addresses A_2 - A_{15} if the $\overline{CE}$ input was LOW at power up. (t_{AA})

The valid data will be output at t_{ACE} or t_{AA} following a transition from the above operations (1) or (2).

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

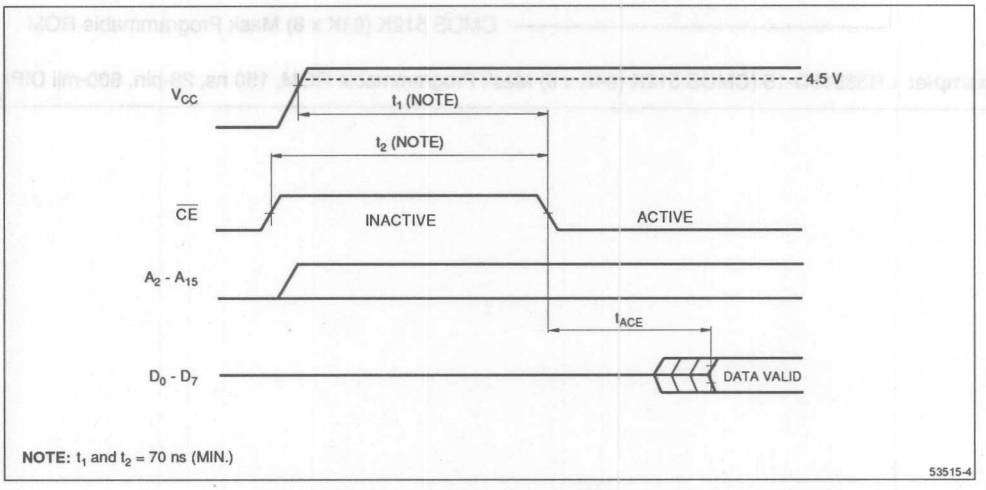


Figure 5. Power On With $\overline{CE}$ Inactive

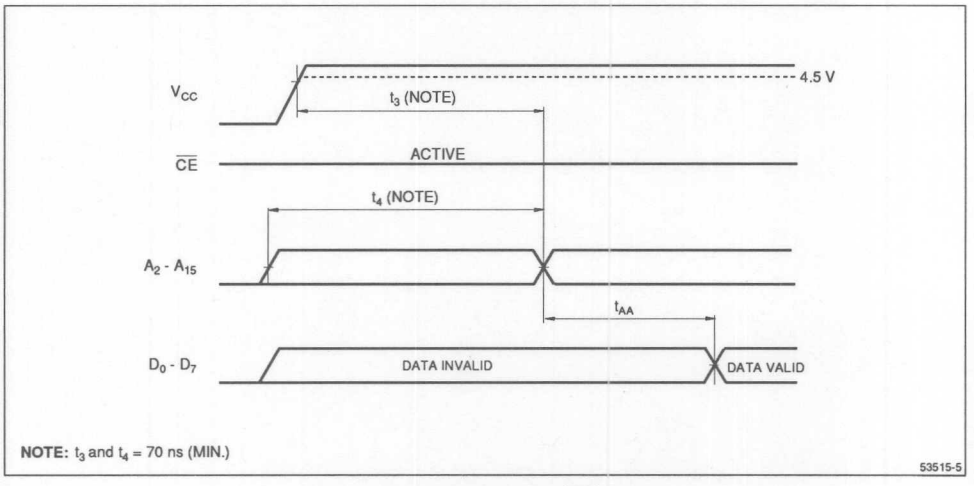
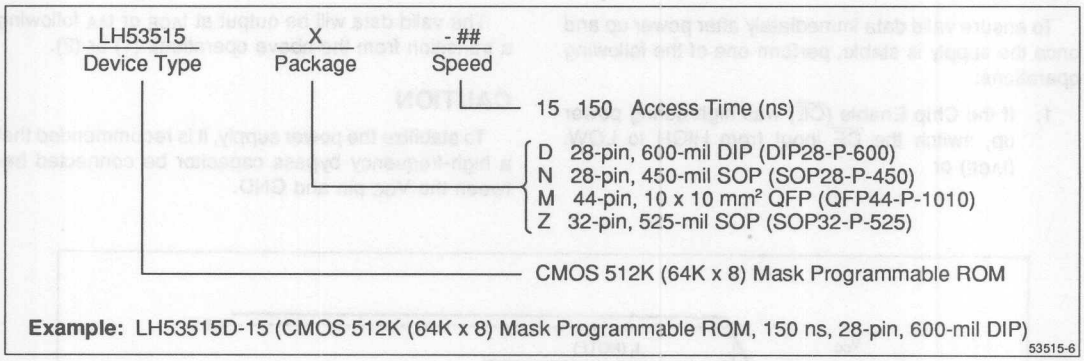


Figure 6. Power On With $\overline{CE}$ Active

ORDERING INFORMATION



Example: LH53515D-15 (CMOS 512K (64K x 8) Mask Programmable ROM, 150 ns, 28-pin, 600-mil DIP)

53515-6

LH53H1000

PRELIMINARY

CMOS 1M (64K × 16) Mask-Programmable ROM

FEATURES

- 65,536 × 16 bit organization
- Access time: 55 ns (MAX.)
- Power consumption:
  Operating: 660 mW (MAX.)
  Standby: 440 mW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH53H1000 is a high speed mask-programmable ROM organized as 65,536 × 16 bits (1,048,576 bits). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

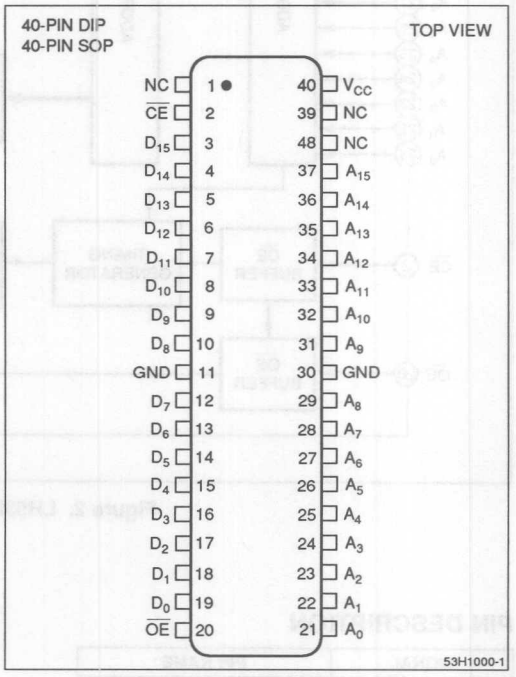


Figure 1. Pin Connections for DIP and SOP Packages

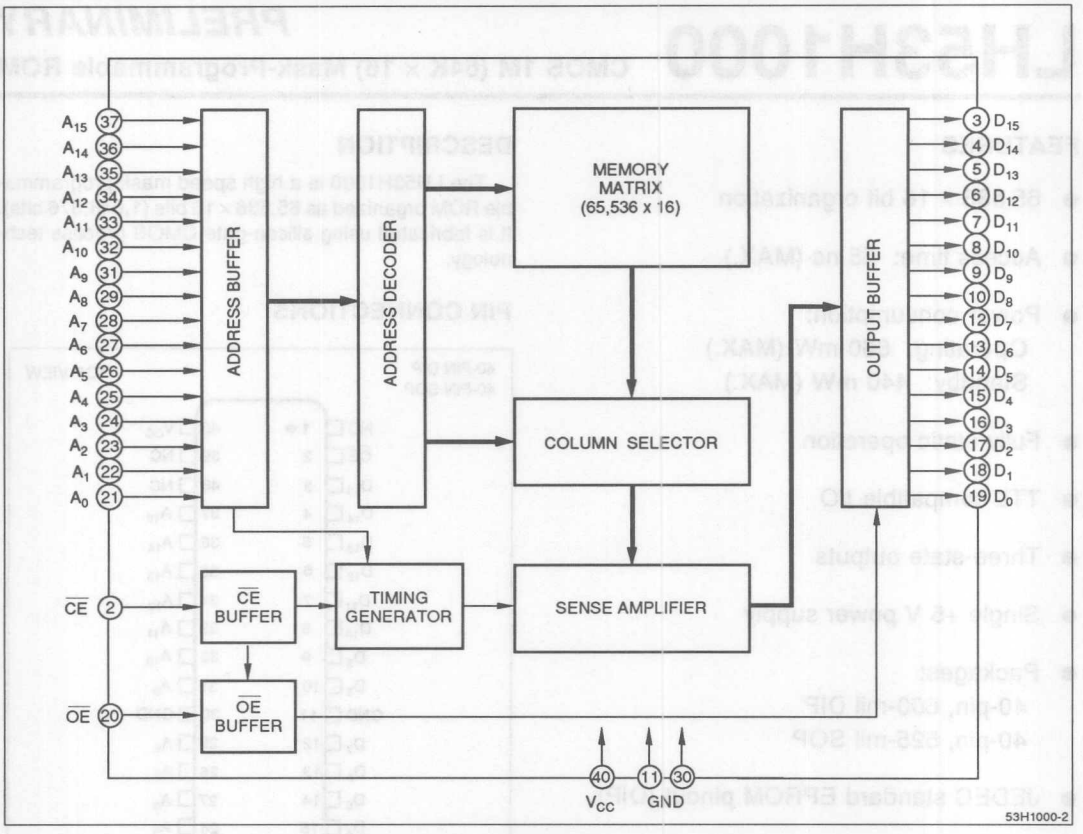


Figure 2. LH53H1000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{15}	Address input
D_0 - D_{15}	Data output
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	MODE	D_0 - D_{15}	SUPPLY CURRENT	NOTE
H	X	Non selected	High-Z	Standby (I_{SB})	1
L	H	Non selected	High-Z	Operating (I_{CC})	
L	L	Selected	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 3.2 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V or V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V or V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 55 ns			120	mA	2
	I_{CC2}	t_{RC} = 55 ns			110		3
Standby current	I_{SB}	$\overline{CE}$ = V_{IH}			2	mA	

NOTES:
1. $\overline{CE}$ or $\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	55			ns	
Address access time	t_{AA}			55	ns	
Chip enable time	t_{ACE}			55	ns	
Output enable delay time	t_{OE}			25	ns	
Output hold time	t_{OH}	0			ns	
CE to output in High-Z	t_{CHZ}			25	ns	1
OE to output in High-Z	t_{OHZ}			25	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0 V to 3.0 V
Input rise/fall time	5 ns
Input reference level	1.5 V
Output load condition	1TTL + 30 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

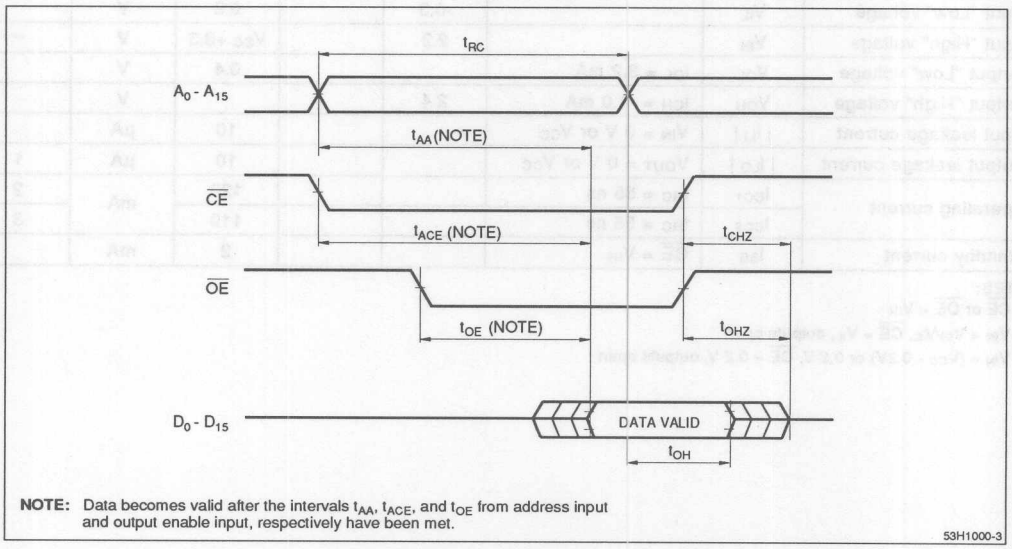
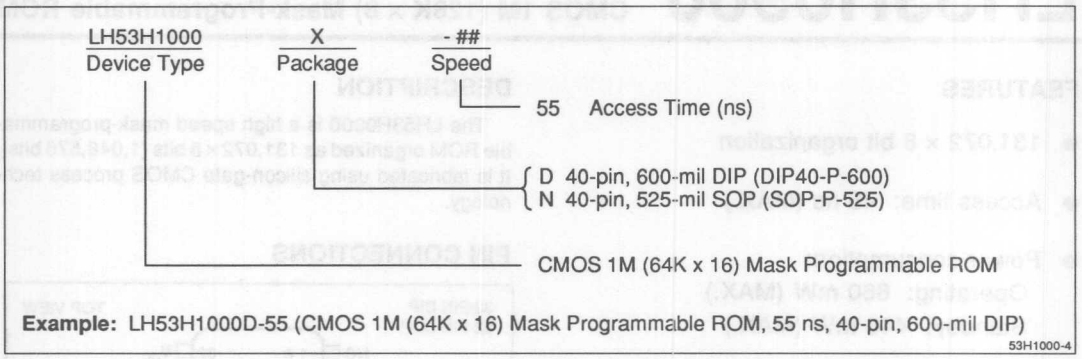


Figure 3. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

ORDERING INFORMATION



Example: LH53H1000D-55 (CMOS 1M (64K x 16) Mask Programmable ROM, 55 ns, 40-pin, 600-mil DIP)

53H1000-4

LH53H0900

PRELIMINARY

CMOS 1M (128K × 8) Mask-Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 45 ns (MAX.)
- Power consumption:
  Operating: 660 mW (MAX.)
  Standby: 440 mW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH53H0900 is a high speed mask-programmable ROM organized as 131,072×8 bits (1,048,576 bits). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

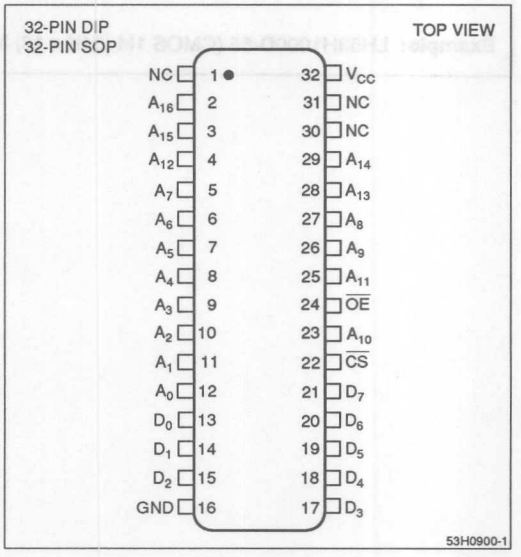


Figure 1. Pin Connections for DIP and SOP Packages

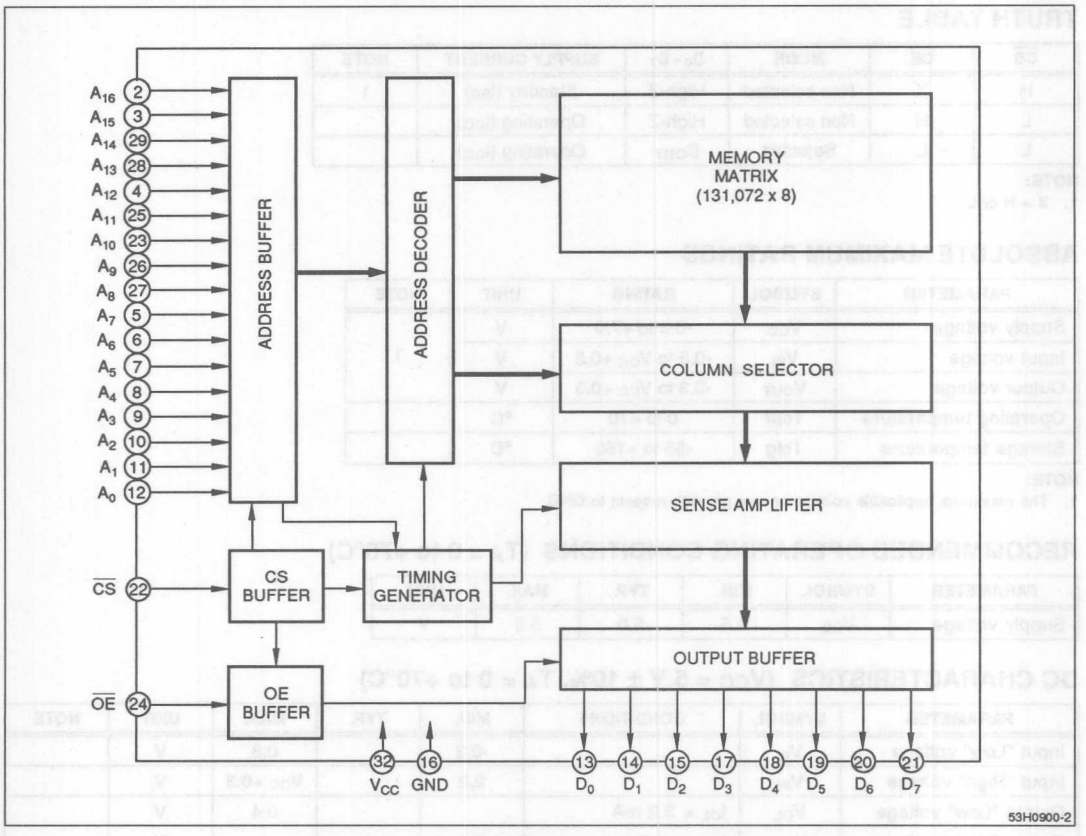


Figure 2. LH53H0900 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{16}	Address input
D_0 - D_7	Data output
$\overline{CS}$	Chip Select input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
H	X	Non selected	High-Z	Standby (I_{SB})	1
L	H	Non selected	High-Z	Operating (I_{CC})	
L	L	Selected	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 3.2 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -1.0 mA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V or V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V or V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 45 ns			120	mA	2
Standby current	I_{SB}	$\overline{CS}$ = V_{IH}			80	mA	

NOTES:
1. $\overline{CS}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CS}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	45			ns	
Address access time	t_{AA}			45	ns	
Chip select time	t_{ACS}			45	ns	
Output enable time	t_{OE}			20	ns	
Output hold time	t_{OH}	0			ns	
CE to output in High-Z	t_{CHZ}			20	ns	1
OE to output in High-Z	t_{OHZ}			20	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0 V to 3.0 V
Input rise/fall time	5 ns
Input reference level	1.5 V
Output load condition	1TTL + 30 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

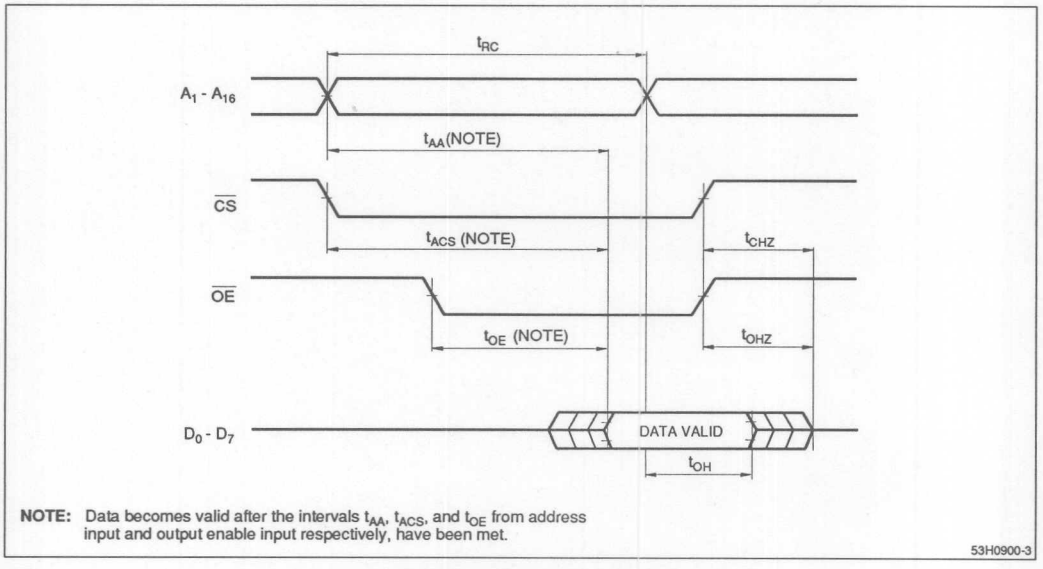
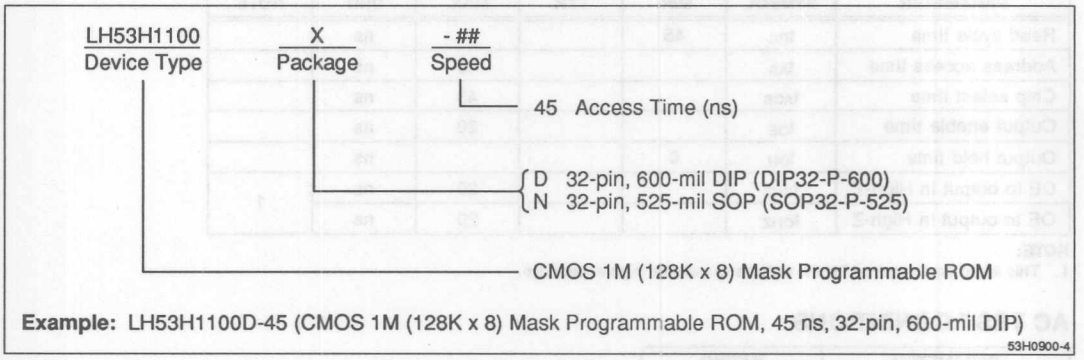


Figure 3. Timing Diagram

CAUTION

To stablize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

ORDERING INFORMATION



LH530800A CMOS 1M (128K × 8) Mask-Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 193 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
  44-pin, 10 × 10 mm^2 QFP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH530800A is a mask-programmable ROM organized as 131,072 × 8 bits (1,048,576 bits). It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

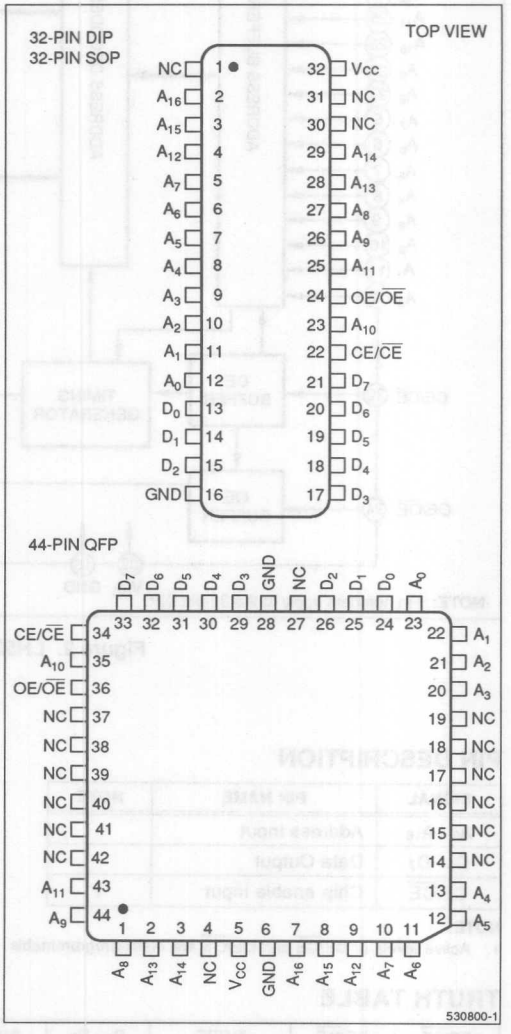


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

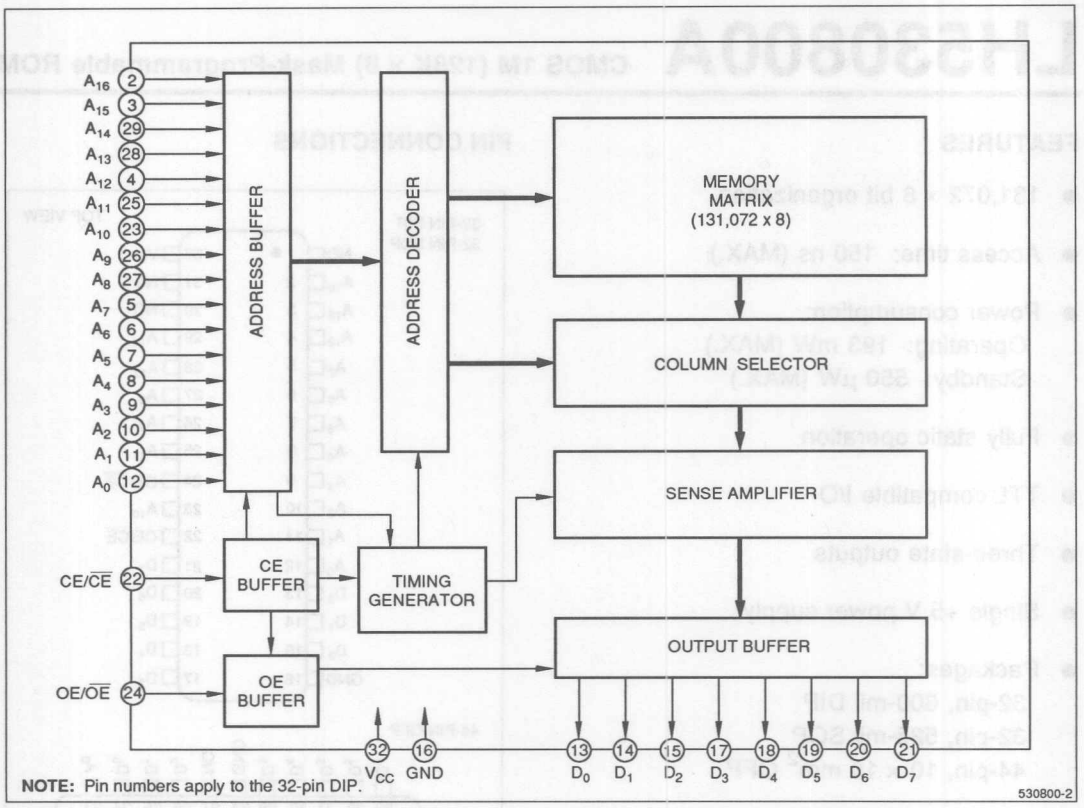


Figure 2. LH530800A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data Output	
CE/$\overline{CE}$	Chip enable input	1

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output enable input	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active levels of CE/$\overline{CE}$ and OE/$\overline{OE}$ are mask-programmable.

TRUTH TABLE

CE/$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT	NOTE
L/H	X	Non selected	High-Z	Standby (I_{SB})	1
H/L	L/H	Non selected	High-Z	Operating (I_{CC})	
H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})	

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} + 0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		
Standby current	I_{SB1}	$CE = V_{IL}$, $\overline{CE} = V_{IH}$			2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V, CE = 0.2 V			100	µA	

NOTES:
1. $\overline{CE}/\overline{OE} = V_{IH}$ or $CE/OE = V_{IL}$
2. $V_{IN} = V_{IH}/V_{IL}$, $\overline{CE} = V_{IL}$, $CE = V_{IH}$, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, CE = V_{CC} - 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable time	t_{ACE}			150	ns	
Output enable time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

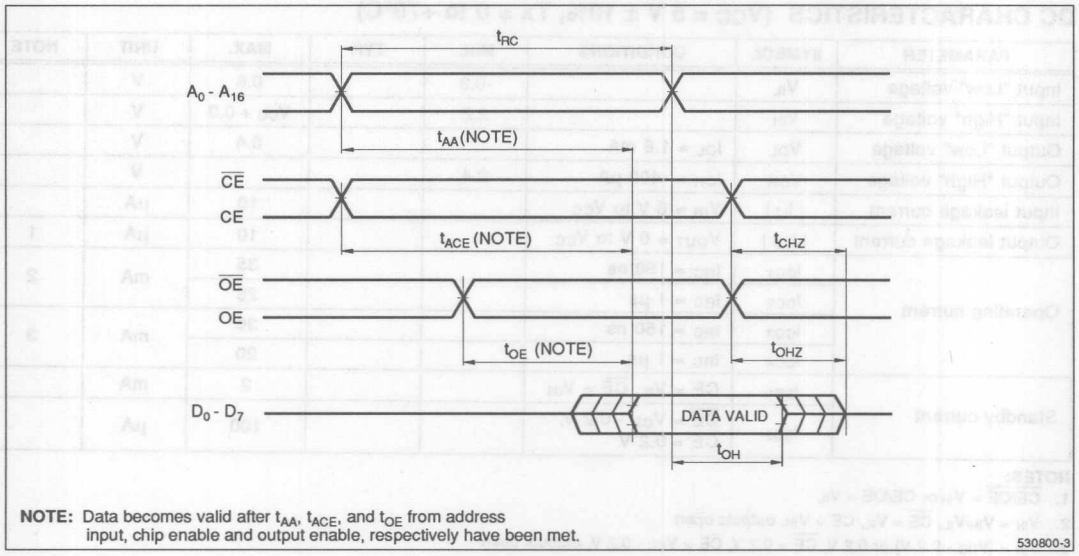


Figure 3. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

To ensure valid data immediately after power up and once the supply is stable, perform one of the following operations:

1. If the Chip Enable ($\overline{CE}$) was high during power up, switch the $\overline{CE}$ input from HIGH to LOW. (t_{ACE}) or
2. Change one or more addresses if the $\overline{CE}$ input was LOW at power up. (t_{AA})

The valid data will be output at t_{ACE} or t_{AA} following a transition from the above operations (1) or (2).

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

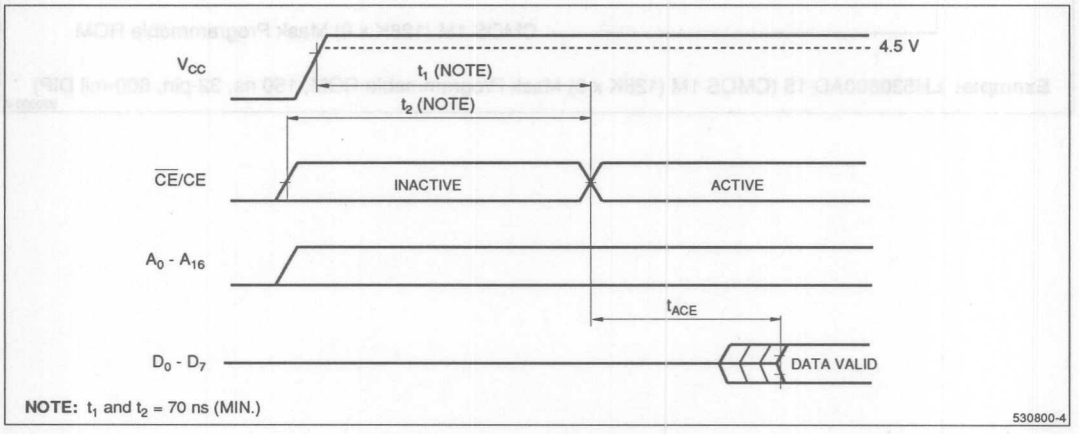


Figure 4. Power On With $\overline{CE}$ Inactive

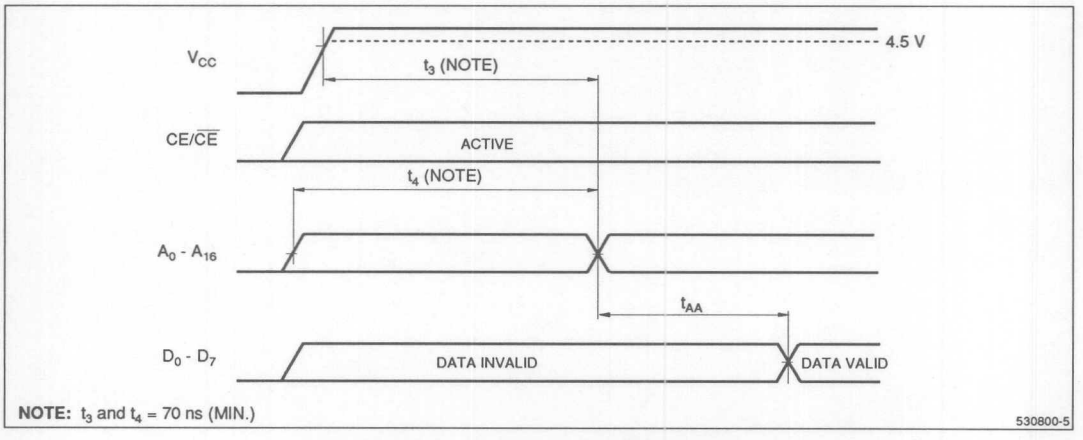
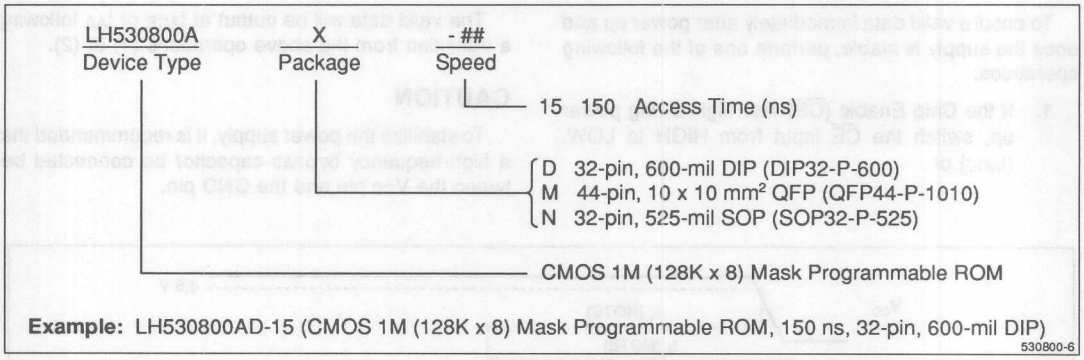


Figure 5. Power On With $\overline{CE}$ Active

ORDERING INFORMATION



LH531000B CMOS 1M (128K × 8) Mask-Programmable ROM

FEATURES

- 131,072 × 8 bit organization
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 192.5 mW (MAX.)
  Standby: 550 µW (MAX.)
- Programmable CE/$\overline{CE}$ or OE/$\overline{OE}$
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP
  44-pin, 14 × 14 mm^2 QFP
- Mask ROM specific pinout

DESCRIPTION

The LH531000B is a mask-programmable ROM organized as 131,072 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

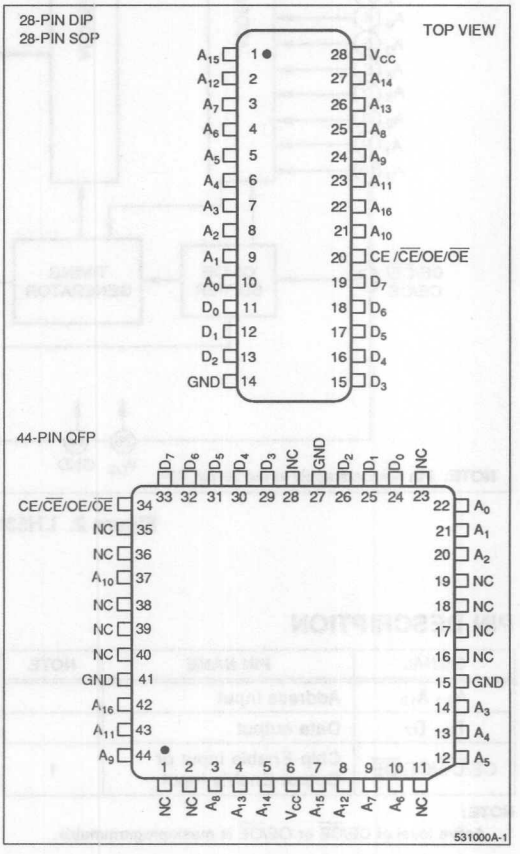


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

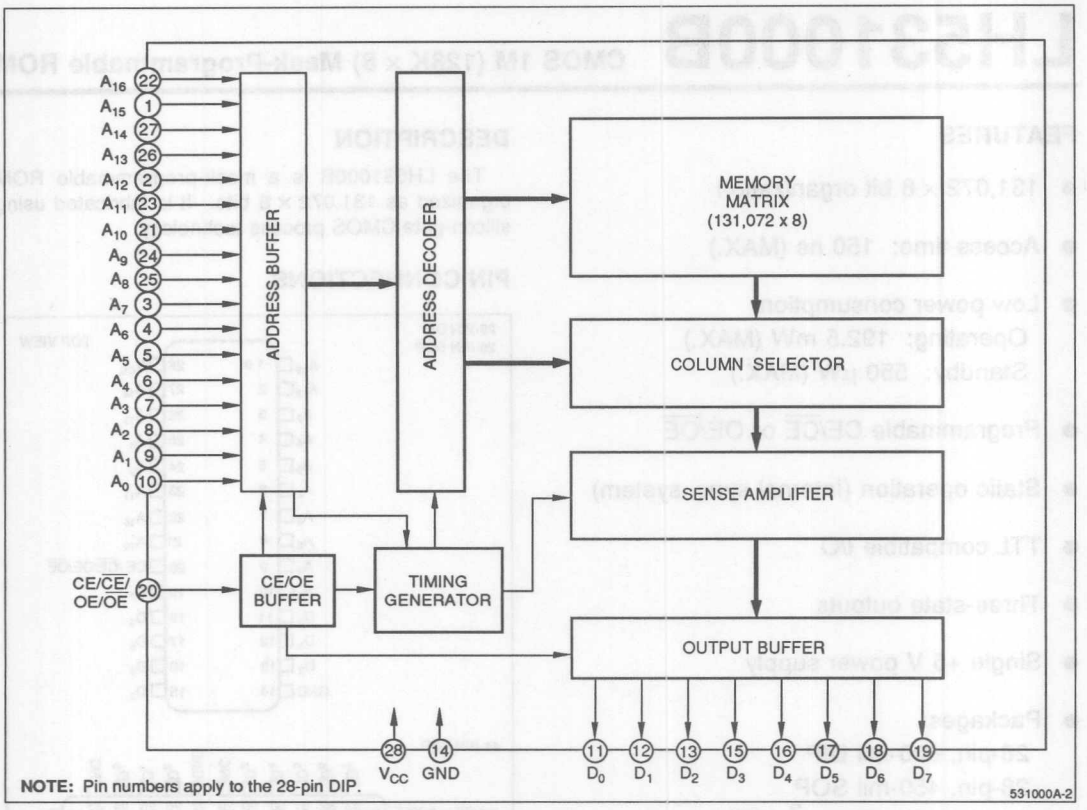


Figure 2. LH531000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{16}	Address input	
D_0 - D_7	Data output	
CE/$\overline{CE}$/OE/$\overline{OE}$	Chip Enable input or Output Enable input	1

SIGNAL	PIN NAME	NOTE
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. Active level of CE/$\overline{CE}$ or OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

PIN 20 (DIP/SOP) or PIN 34 (QFP)	CE/$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT
CE type	H/L	—	Selected	D_{OUT}	Operating (I_{CC})
	L/H	—	Non selected	High-Z	Standby (I_{SB})
OE type	—	H/L	Selected	D_{OUT}	Operating (I_{CC})
	—	L/H	Non selected	High-Z	

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			35	mA	2
	I_{CC2}	t_{RC} = 1 µs			25		
	I_{CC3}	t_{RC} = 150 ns			30	mA	3
	I_{CC4}	t_{RC} = 1 µs			20		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}, CE = V_{IL}			2	mA	4
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V, CE = 0.2 V			100	µA	

NOTES:
1. CE/$\overline{OE}$ = V_{IL}, $\overline{CE}$/$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, CE = V_{IH}, $\overline{CE}$ = V_{IL} (CE type), outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V. CE = V_{CC} - 0.2 V, $\overline{CE}$ = 0.2 V (CE type), outputs open
4. CE type only

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}		150			ns	
Address access time	t_{AA}				150	ns	
Chip enable access time	t_{ACE}	CE type			150	ns	
Output enable time	t_{OE}	OE type	10		80	ns	
Output hold time	t_{OH}		5			ns	
CE to output in High-Z	t_{CHZ}	CE type			70	ns	1
OE to output in High-Z	t_{OHZ}	OE type			70	ns	

NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

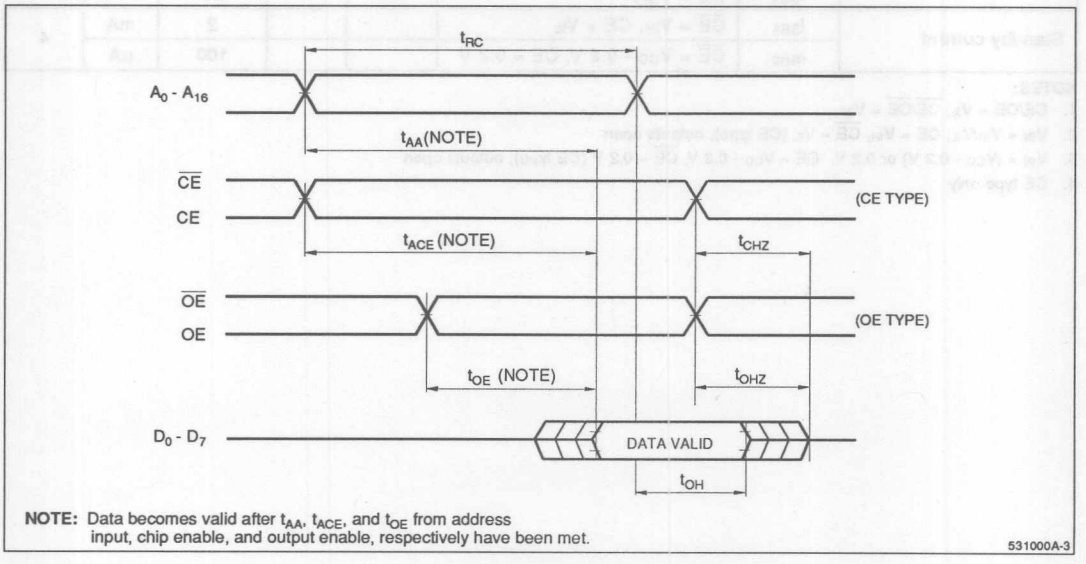


Figure 3. Timing Diagram

OPERATION IMMEDIATELY AFTER POWER UP

To ensure valid data immediately after power up and once the supply is stable, perform one of the following operations:

$\overline{CE}$ or CE Type

1. If the Chip Enable ($\overline{CE}$) was high during power up, switch the $\overline{CE}$ input from HIGH to LOW. (t_{ACE}) or
2. Change one or more addresses if the $\overline{CE}$ input was LOW at power up. (t_{AA})

$\overline{OE}$ or OE Type

1. Change one or more addresses at power up.

The valid data will be output at t_{ACE} or t_{AA} following a transition from the above operations (1) or (2).

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

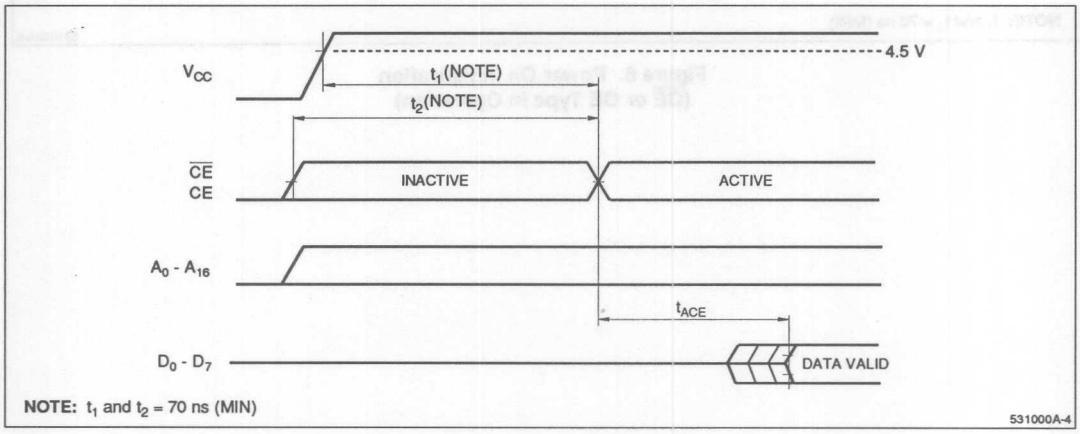


Figure 4. Power On With CE/$\overline{CE}$ Inactive ($\overline{CE}$ or CE Type in Operation)

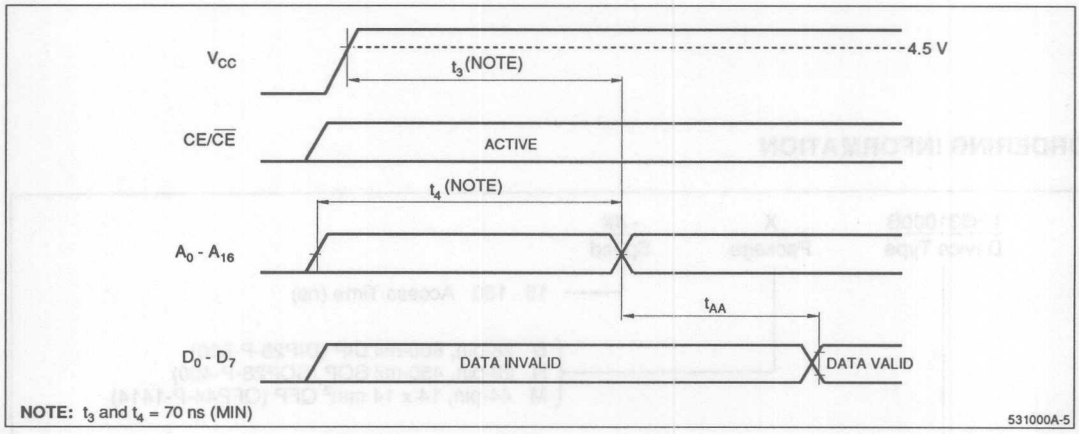


Figure 5. Power On With CE/$\overline{CE}$ Active ($\overline{CE}$ or CE Type in Operation)

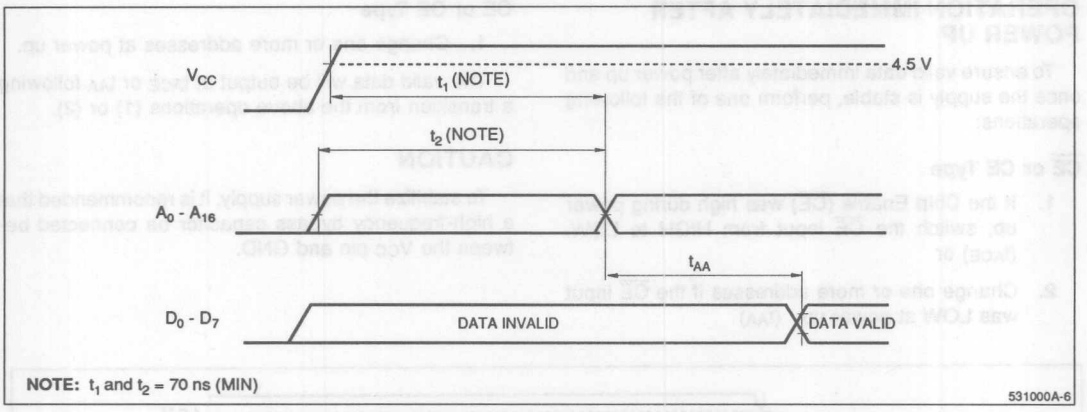
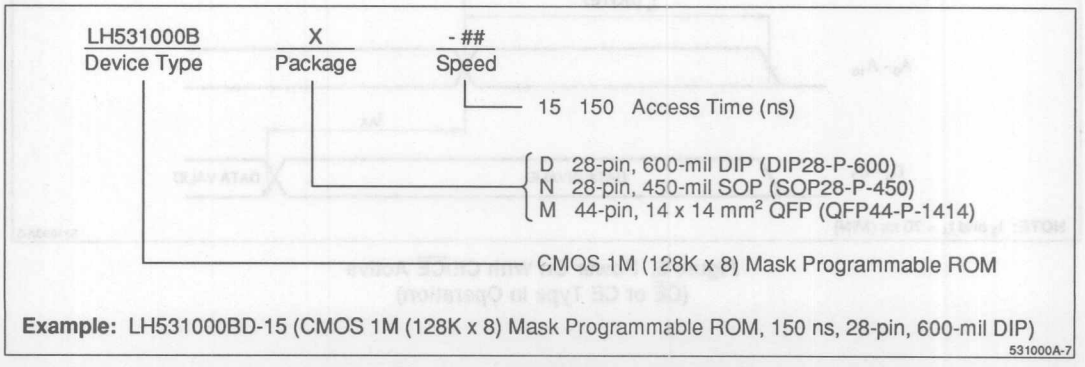


Figure 6. Power On Initialization (OE or OE Type in Operation)

ORDERING INFORMATION



LH532000B

CMOS 2M (256K × 8 / 128K × 16) Mask-Programmable ROM

FEATURES

- Selectable memory organization:
  262,144 × 8 bit (byte mode)
  131,072 × 16 bit (word mode)
- $\overline{BYTE}$ input pin selects bit configuration
- Access time: 120/150 ns (MAX.)
- Low power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Programmable OE/$\overline{OE}$ and $OE_1/\overline{OE_1}$/DC
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
  44-pin, 14 × 14 mm^2 QFP
  44-pin, 10 × 10 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH532000B is a 2M bit mask-programmable ROM with two programmable memory organizations, byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

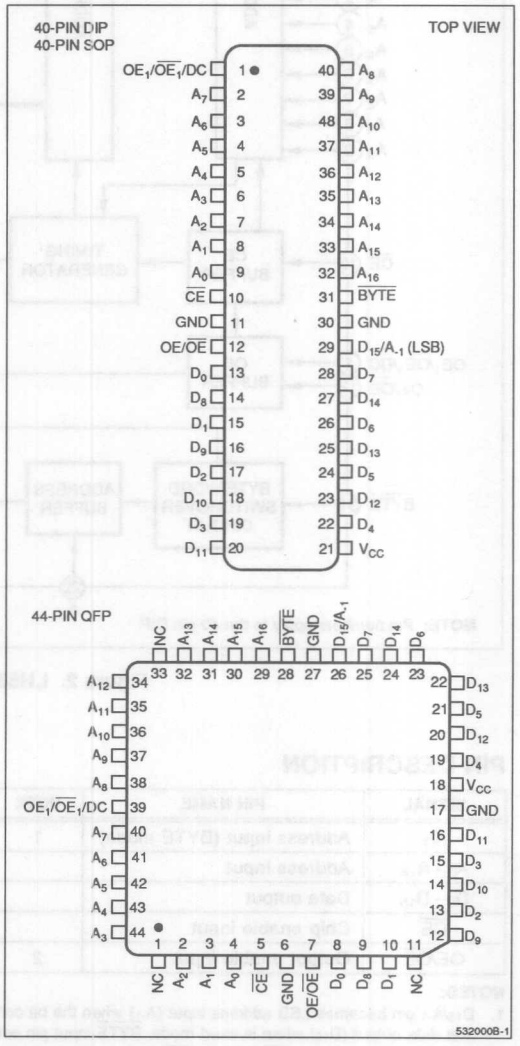


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

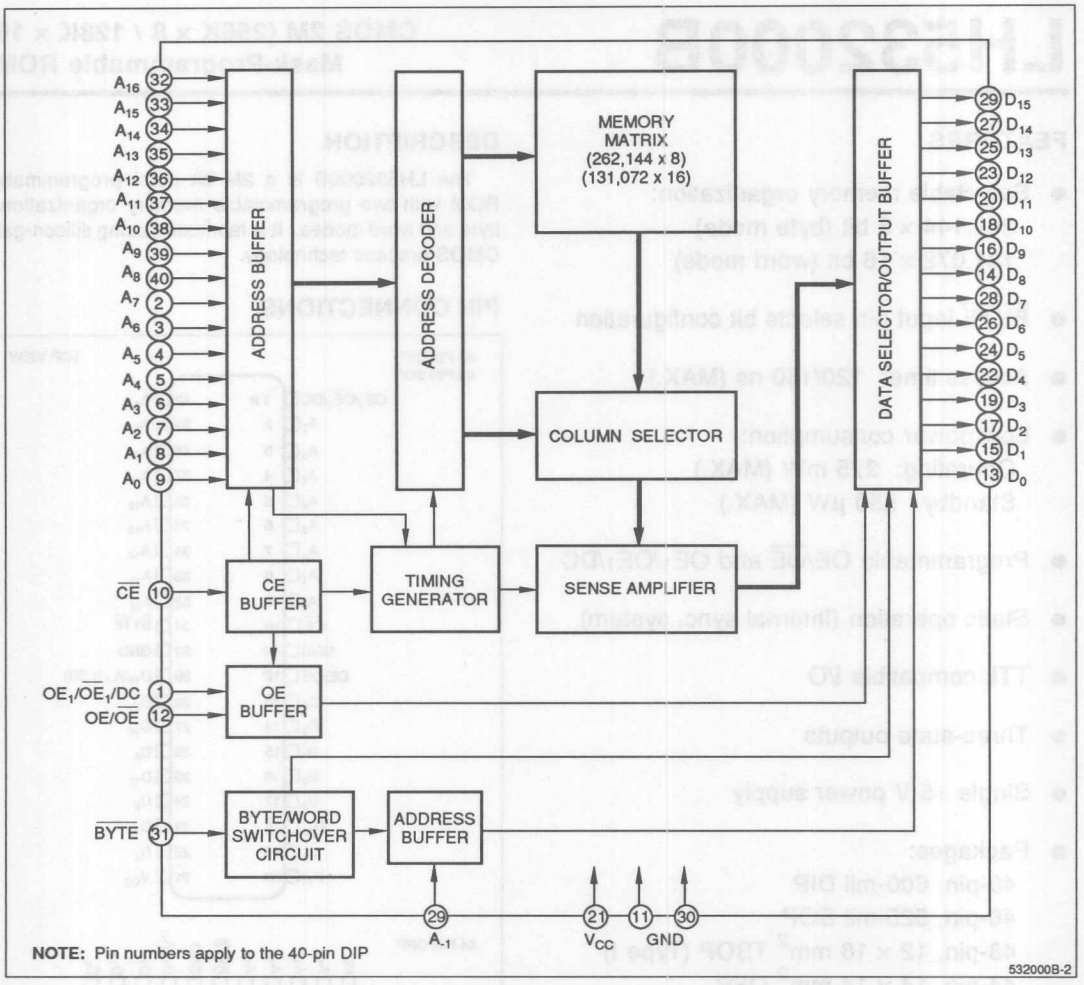


Figure 2. LH532000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (BYTE mode)	1
A_0 - A_{16}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip enable input	
OE/$\overline{OE}$	Output enable input	2

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE_1}/DC$	Output enable input or Don't care	2
$\overline{BYTE}$	$\overline{BYTE}$/WORD switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. BYTE input pin selects bit configuration.
2. The active levels of OE/$\overline{OE}$ and $OE_1/\overline{OE_1}$/DC are mask-programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	$OE/\overline{OE}$	$OE_1/\overline{OE_1}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	L/H	X	X	X	Non selected	High-Z		Operating (I_{CC})
L	X	L/H	X	X	Non selected	High-Z		Operating (I_{CC})
L	H/L	H/L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	H/L	H/L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	H/L	H/L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTE:
1. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = t_{RC} (MIN.)			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = t_{RC} (MIN.)			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE/OE_1 = V_{IL}, $\overline{CE}/\overline{OE}/\overline{OE_1}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		150		ns	
Address access time	t_{AA}		120		150	ns	
Chip enable access time	t_{ACE}		120		150	ns	
Output enable delay time	t_{OE}		55	10	70	ns	
Output hold time	t_{OH}	5		10		ns	
CE to output in High-Z	t_{CHZ}		55		70	ns	1
OE to output in High-Z	t_{OHZ}		55		70	ns	

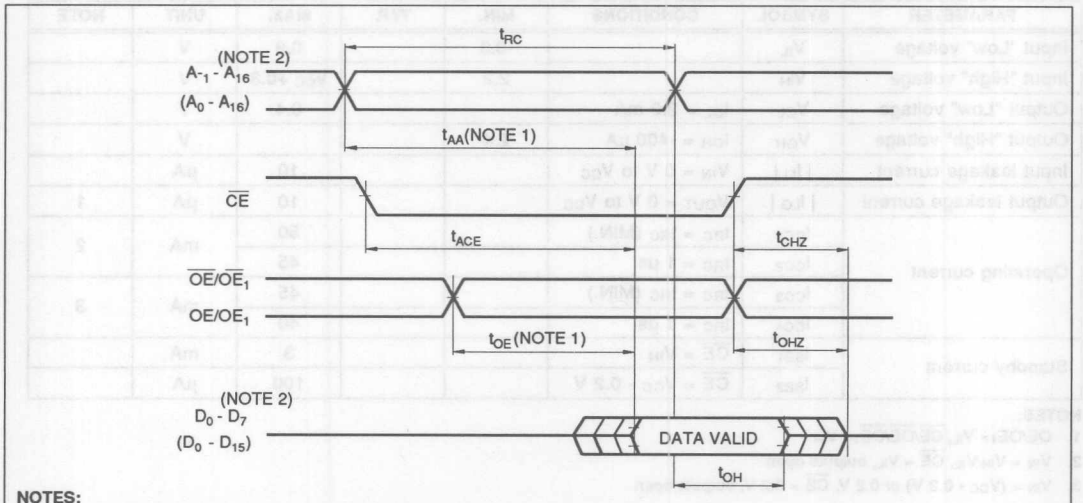
NOTE:
1. This is the time required for the output to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

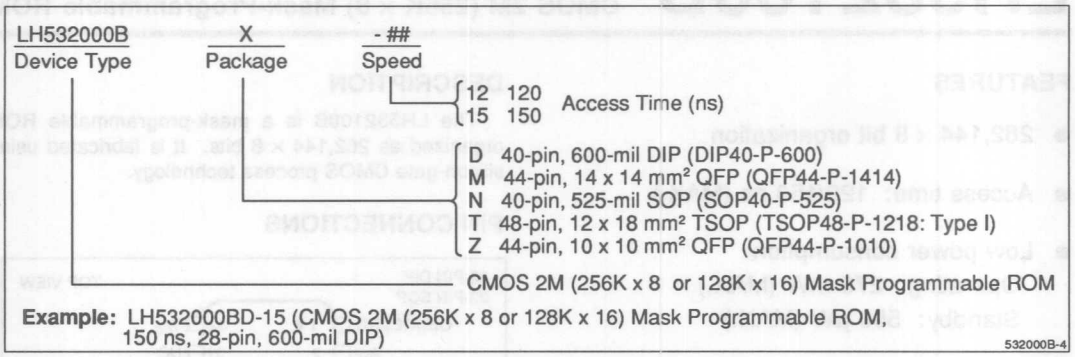


NOTES:
1. Data becomes valid after t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively have been met.
2. Applied to byte mode. Signals in parentheses apply to word mode.

532000B-3

Figure 3. Timing Diagram

ORDERING INFORMATION



LH532100B CMOS 2M (256K × 8) Mask-Programmable ROM

FEATURES

- 262,144 × 8 bit organization
- Access time: 120/150 ns (MAX.)
- Low power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation (Internal sync. system)
- Mask-programmable OE/$\overline{OE}$ and $OE_1/\overline{OE_1}$
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH532100B is a mask-programmable ROM organized as 262,144 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

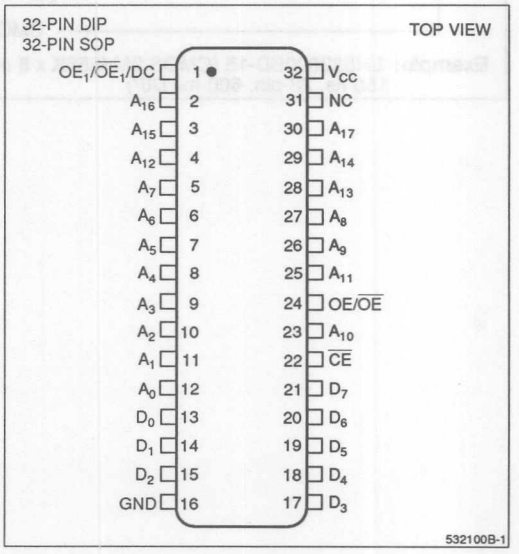


Figure 1. Pin Connections for DIP and SOP Packages

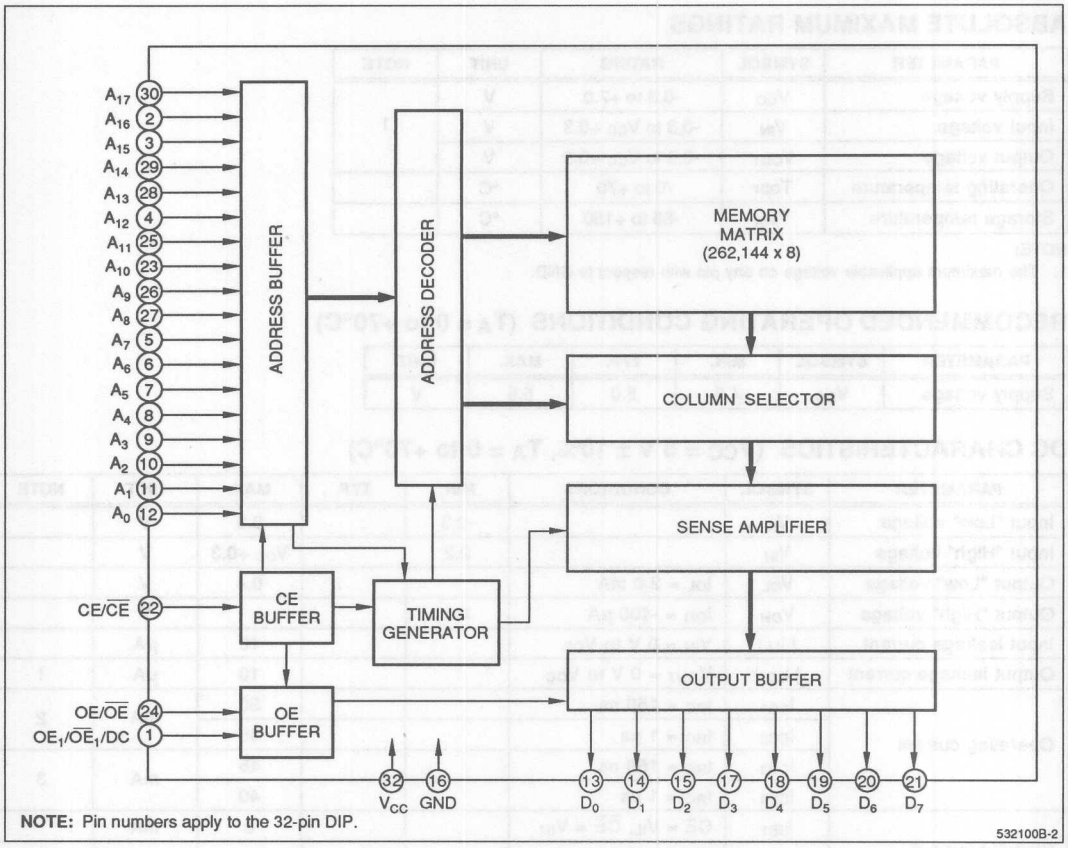


Figure 2. LH532100B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{17}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip Enable input	
OE/$\overline{OE}$	Output Enable input	1

SIGNAL	PIN NAME	NOTE
OE$_1$/$\overline{OE}_1$/DC	Output Enable input/ Don't Care connection	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. Active levels of OE/$\overline{OE}$ and OE$_1$/$\overline{OE}_1$/DC are mask-programmable. Selecting DC allows the outputs to be active for both high and low levels applied to this pin. It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	OE$_1$/$\overline{OE}_1$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	X	Non selected	High-Z	Standby (I_{SB})
L	L/H	X	Non selected	High-Z	Operating (I_{CC})
L	X	L/H	Non selected	High-Z	Operating (I_{CC})
L	H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:

X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 150 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	CE = V_{IL}, $\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	CE = 0.2 V, $\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}/\overline{OE_1}$ = V_{IH} or OE/OE_1 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	120		150		ns	
Address access time	t_{AA}		120		150	ns	
Chip enable access time	t_{ACE}		120		150	ns	
Output enable delay time	t_{OE}		50	10	70	ns	
Output hold time	t_{OH}	5		10		ns	
CE to output in High-Z	t_{CHZ}		50		70	ns	1
OE to output in High-Z	t_{OHZ}		50		70	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

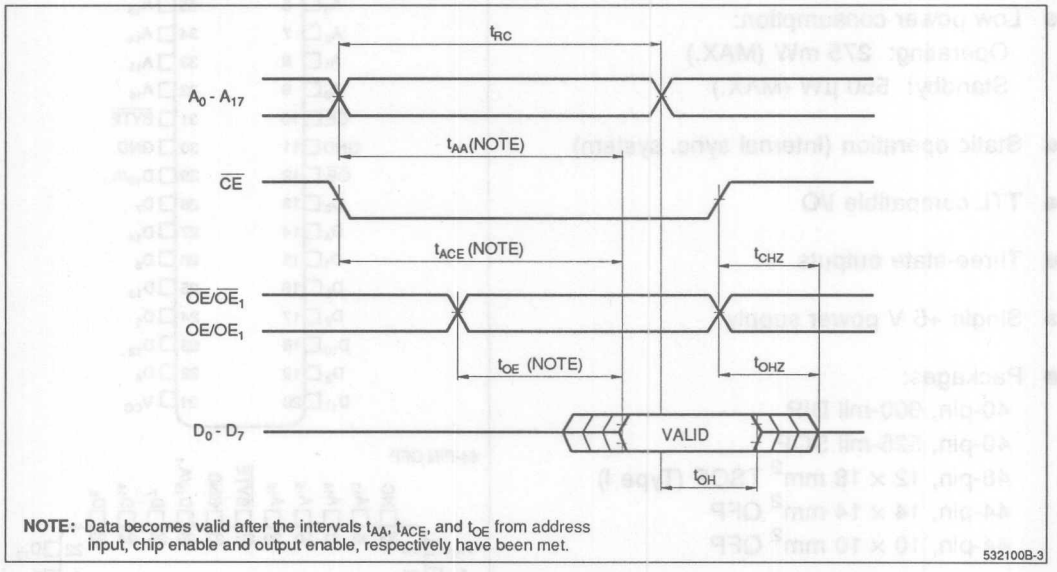
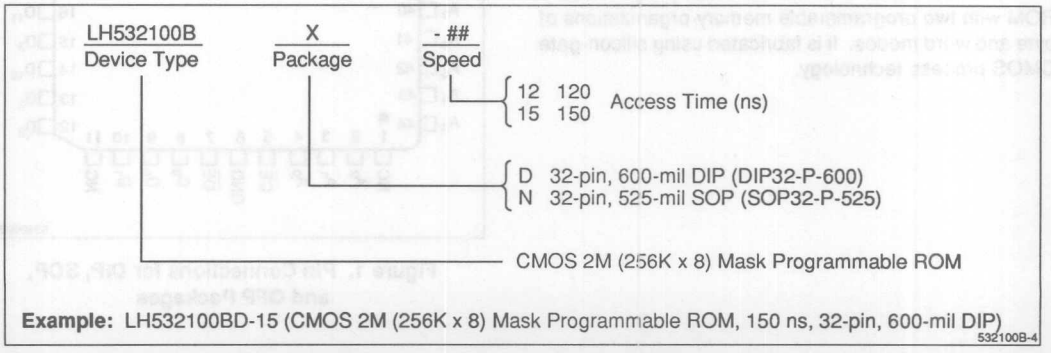


Figure 3. Timing Diagram

ORDERING INFORMATION



LH534000B

CMOS 4M (512K × 8 / 256K × 16)
Mask-Programmable ROM

FEATURES

- Memory organization selection:
  524,288 × 8 bit (byte mode)
  262,144 × 16 bit (word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Low power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation (Internal sync. system)
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
  44-pin, 14 × 14 mm^2 QFP
  44-pin, 10 × 10 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH534000B is a 4M bit mask-programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

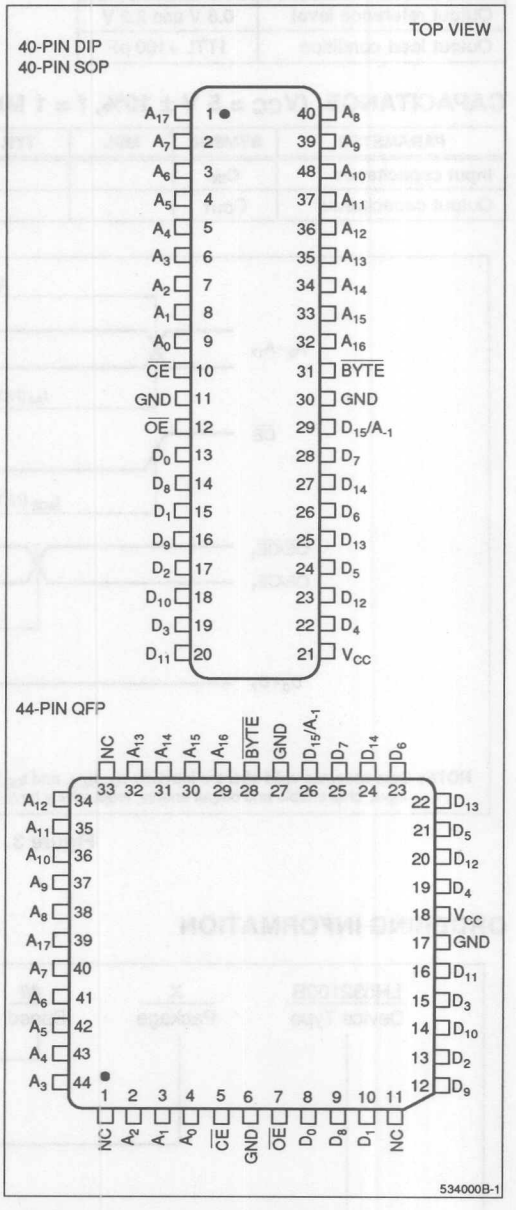


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

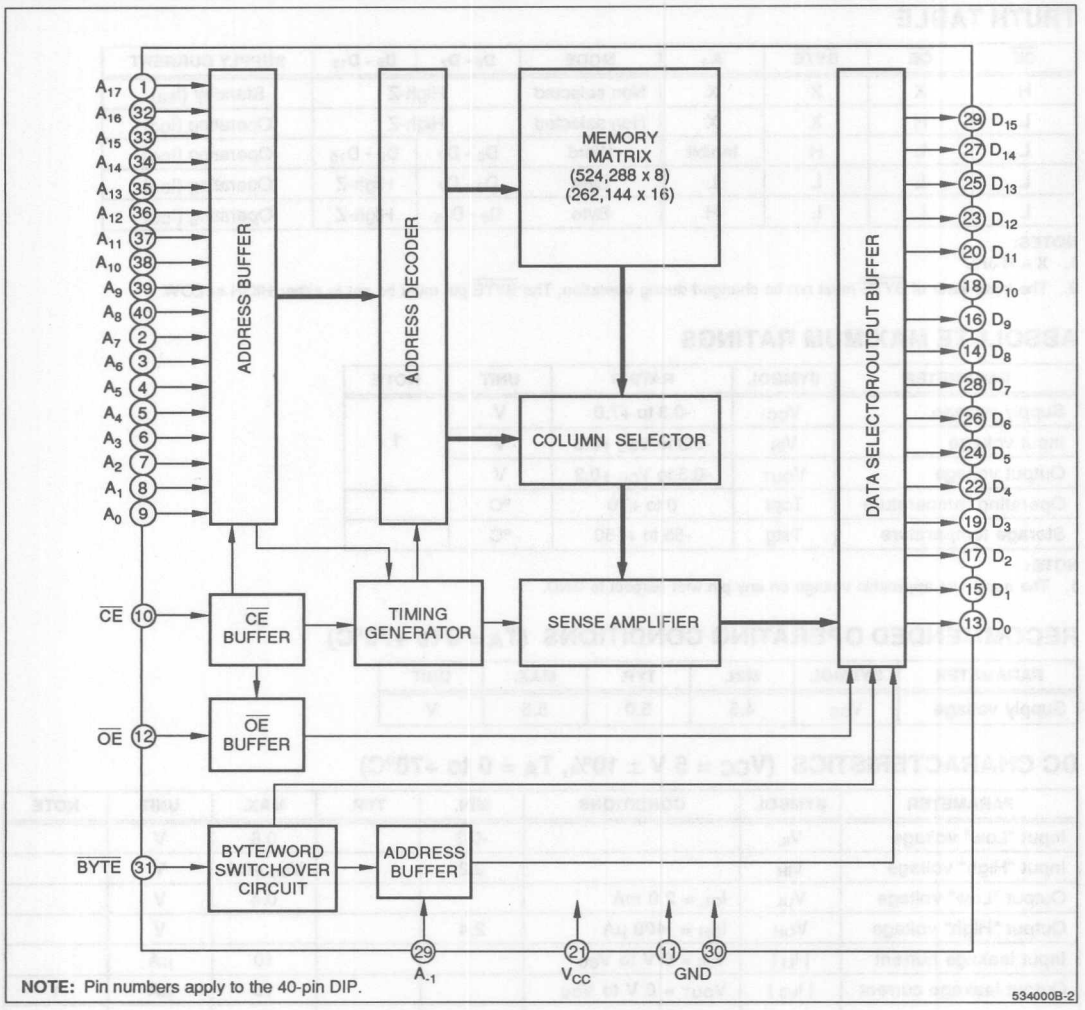


Figure 2. LH534000B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (BYTE mode)	1
A_0 - A_{17}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Chip enable input	
$\overline{BYTE}$	Byte/word mode switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	H	X	X	Non selected	High-Z		Operating (I_{CC})
L	L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTES:
1. X = H or L
2. The input state of $\overline{BYTE}$ must not be changed during operation. The $\overline{BYTE}$ pin must be set to either HIGH or LOW.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 200 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE = V_{IL}, $\overline{CE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
Chip enable access time	t_{ACE}			200	ns	
Output enable delay time	t_{OE}			80	ns	
Output hold time	t_{OH}	10			ns	
CE to output in High-Z	t_{CHZ}			80	ns	1
OE to output in High-Z	t_{OHZ}			80	ns	

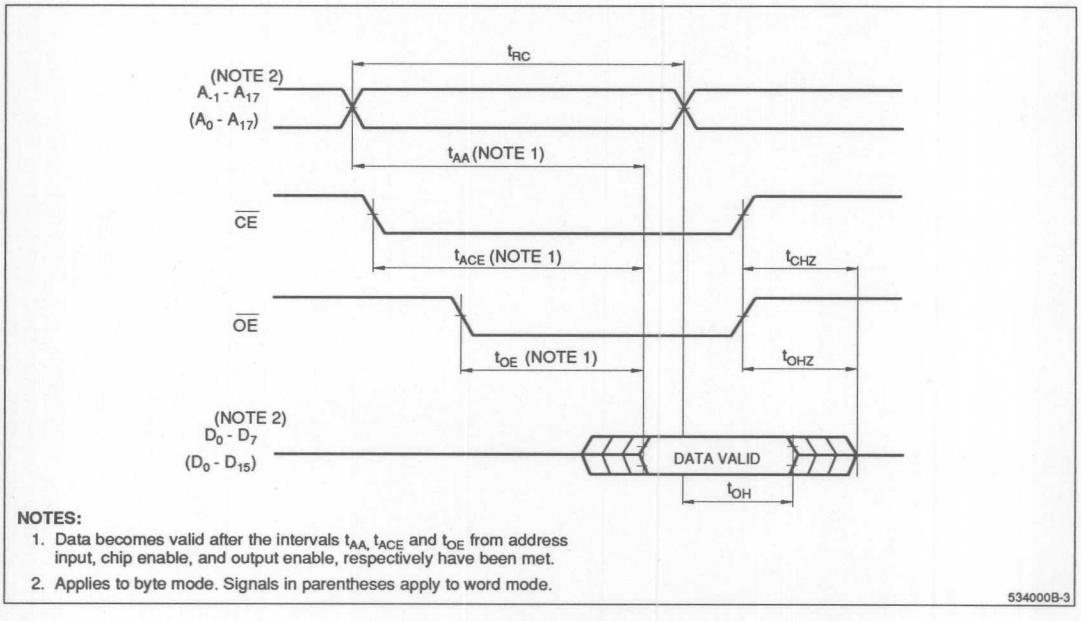
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

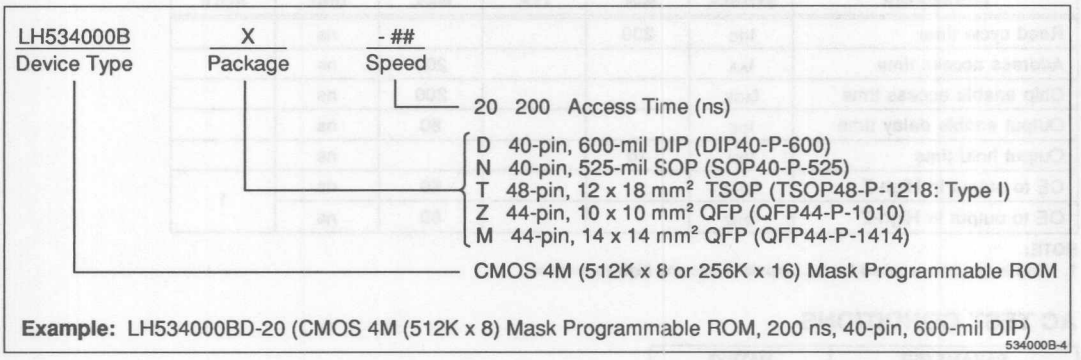


NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE} and t_{OE} from address input, chip enable, and output enable, respectively have been met.
2. Applies to byte mode. Signals in parentheses apply to word mode.

534000B-3

Figure 3. Timing Diagram

ORDERING INFORMATION



LH534100B CMOS 4M (512K × 8) Mask-Programmable ROM

FEATURES

- 524,288 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Mask-programmable OE/$\overline{OE}$ and $OE_1/\overline{OE}_1$/DC
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH534100B is a 4M-bit mask-programmable ROM organized as 524,288 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

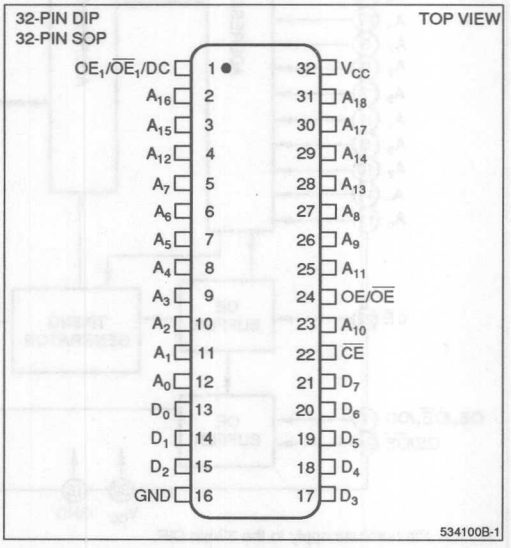


Figure 1. Pin Connections for DIP and SOP Packages

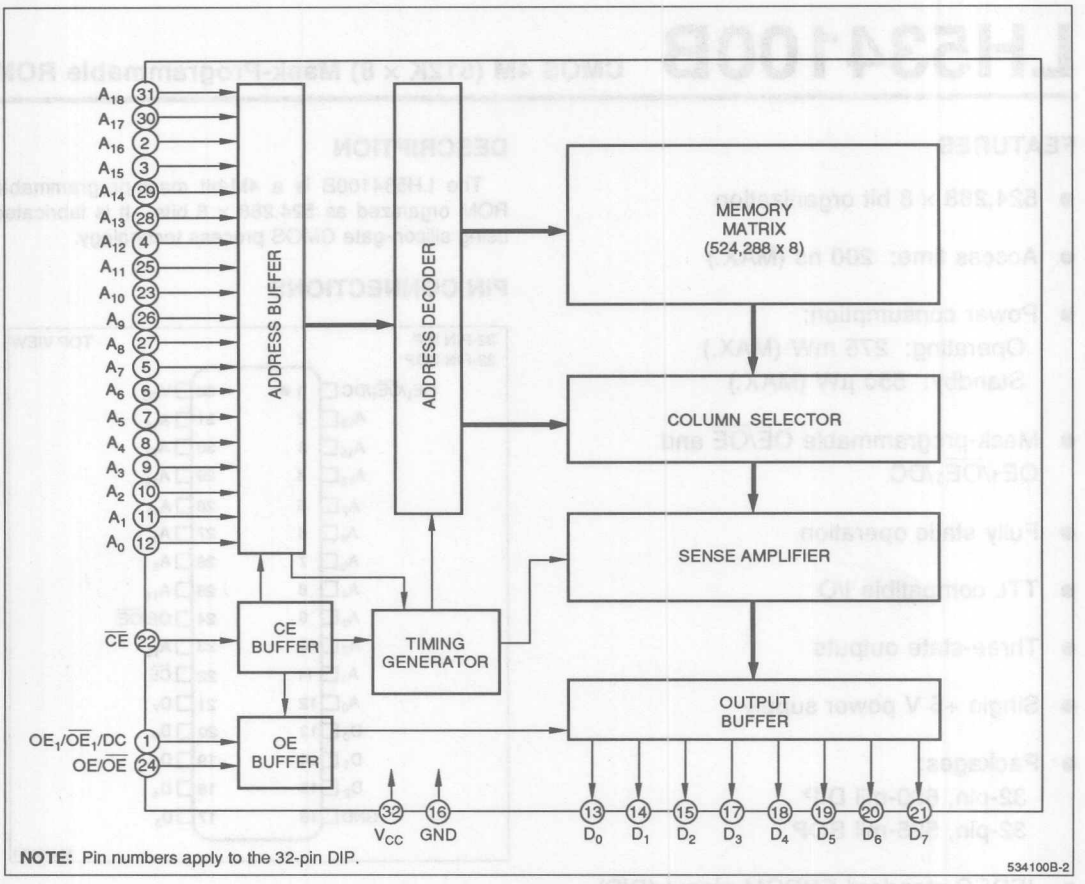


Figure 2. LH534100B Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{18}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip Enable input	
OE/$\overline{OE}$	Output Enable input	1

SIGNAL	PIN NAME	NOTE
$OE_1/\overline{OE_1}$/DC	Output Enable input/ Don't Care	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. Active levels of $OE_1/\overline{OE_1}$/DC and OE/$\overline{OE}$ are mask-programmable.
   Selecting DC allows the outputs to be active for both high and low levels applied to this pin.
   It is recommended to apply either a HIGH or a LOW to the DC pin.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$OE_1/\overline{OE_1}$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	X	Non selected	High-Z	Standby (I_{SB})
L	X	L/H	Non selected	High-Z	Operating (I_{CC})
L	L/H	X	Non selected	High-Z	Operating (I_{CC})
L	H/L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 200 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}/\overline{OE_1}$ = V_{IH} or OE/OE_1 = V_{IL}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Chip enable time	t_{ACE}		200	ns	
Output enable time	t_{OE}		80	ns	
Output hold time	t_{OH}	10		ns	
CE to output in High-Z	t_{CHZ}		80	ns	1
OE to output in High-Z	t_{OHZ}		80	ns	

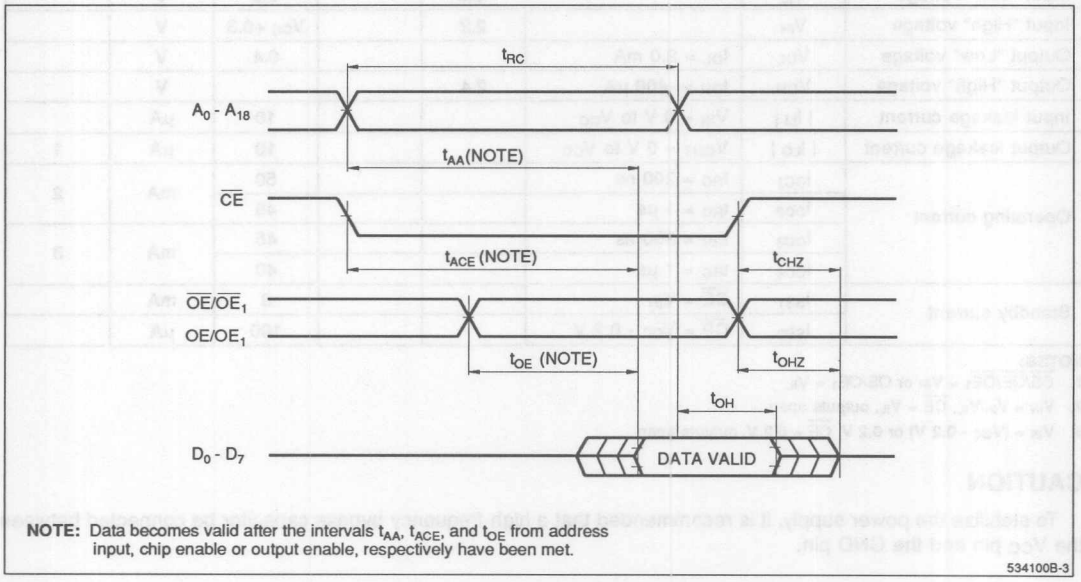
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

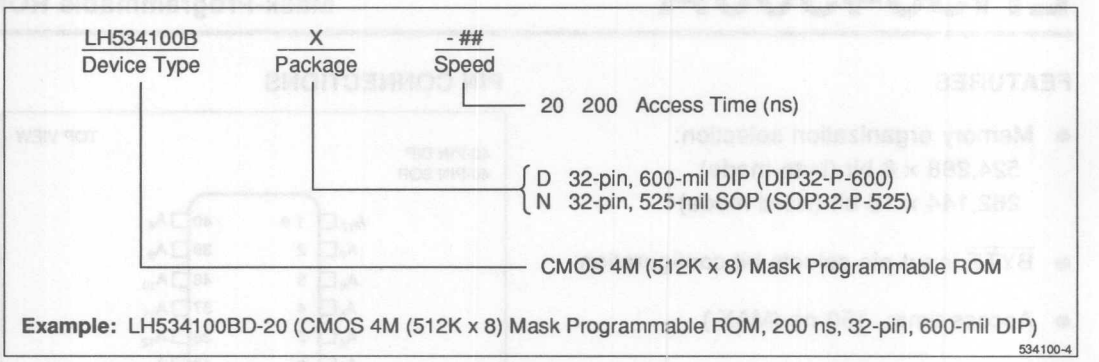


NOTE: Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively have been met.

534100B-3

Figure 3. Timing Diagram

ORDERING INFORMATION



LH534500A

CMOS 4M (512K × 8 / 256K × 16)
Mask-Programmable ROM

FEATURES

- Memory organization selection:
  524,288 × 8 bit (byte mode)
  262,144 × 16 bit (word mode)
- $\overline{BYTE}$ input pin selects bit configuration
- Access time: 150 ns (MAX.)
- Low power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Static operation (Internal sync. system)
- Automatic power down mode
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
  44-pin, 14 × 14 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH534500A is a 4M bit mask-programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

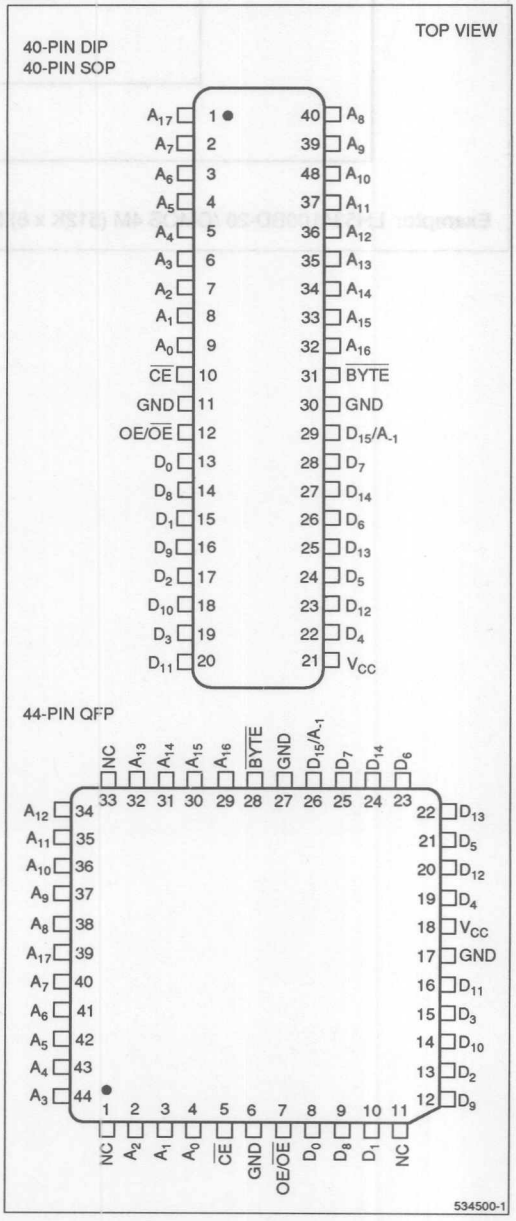


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

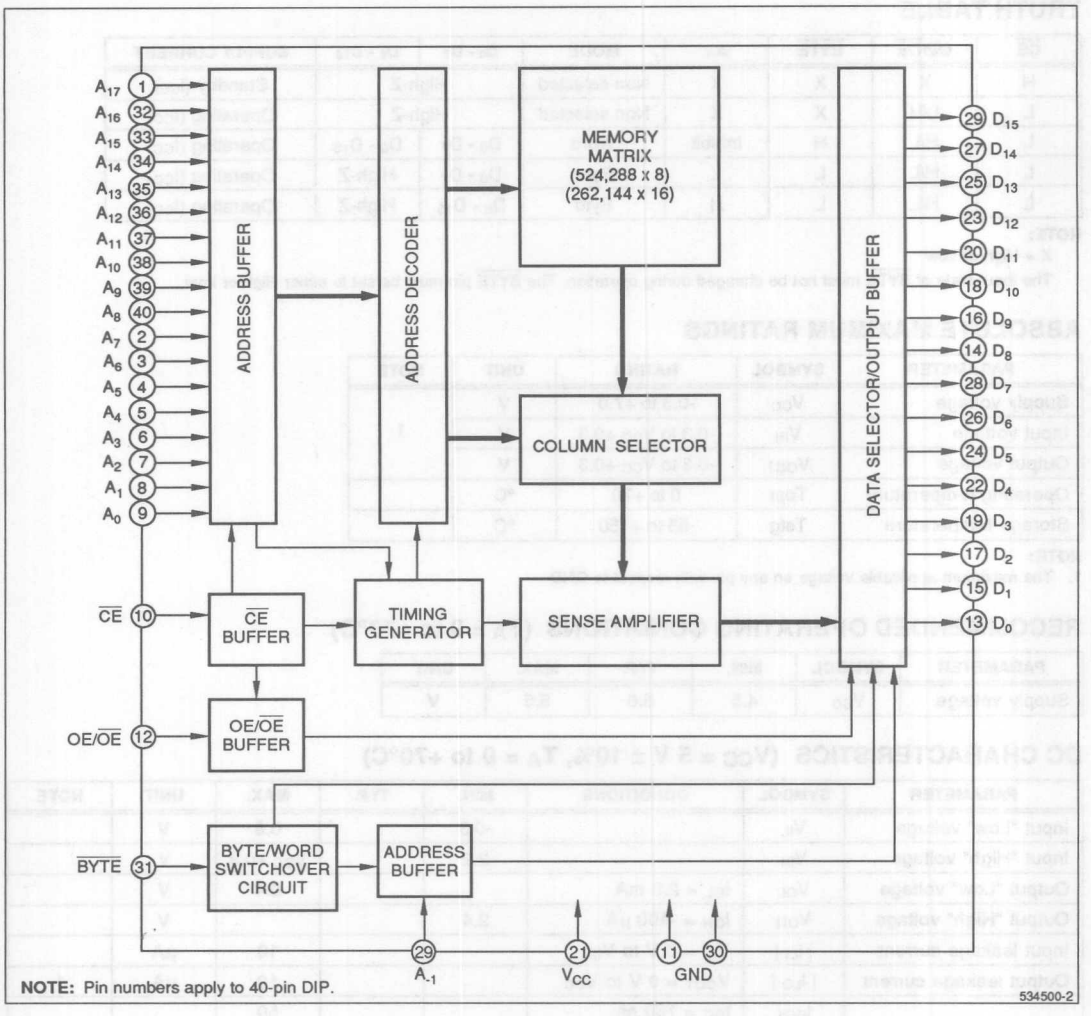


Figure 2. LH534500A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input	1
A_0 - A_{17}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Chip Enable input	2
$\overline{BYTE}$	Byte/word mode switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.
2. Active level of OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	L/H	X	X	Non selected	High-Z		Operating (I_{CC})
L	H/L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	H/L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	H/L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTE:
X = High or Low
The input state of $\overline{BYTE}$ must not be changed during operation. The $\overline{BYTE}$ pin must be set to either High or Low.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			45		
	I_{CC3}	t_{RC} = 150 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			5	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. OE = V_{IL}, $\overline{CE}$/$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150			ns	
Address access time	t_{AA}			150	ns	
Chip enable access time	t_{ACE}			150	ns	
Output enable delay time	t_{OE}			70	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

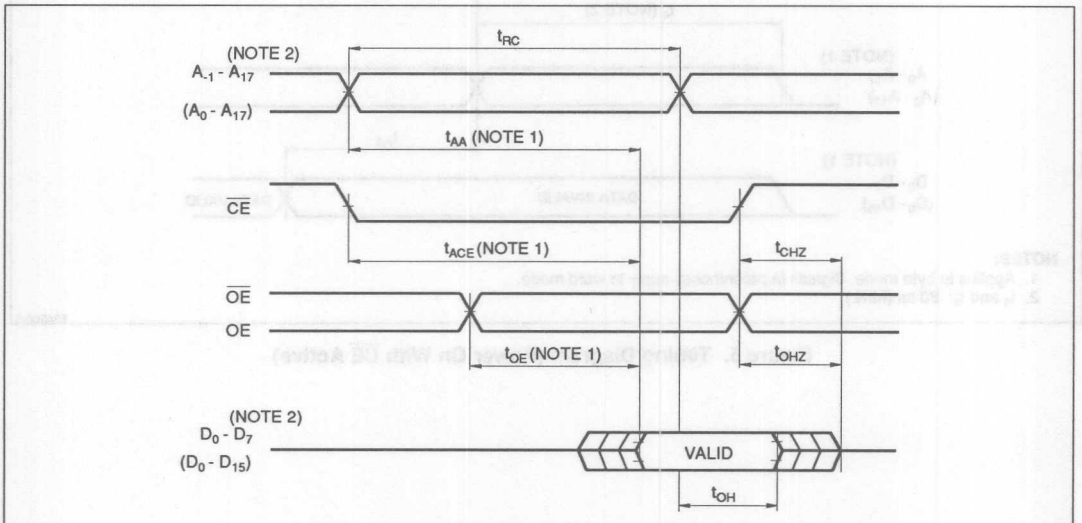
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE} and t_{OE} from address input, chip enable, and output enable, respectively have been met.
2. Applies to byte mode. Signals in parentheses apply to word mode.

534500-3

Figure 3. Timing Diagram

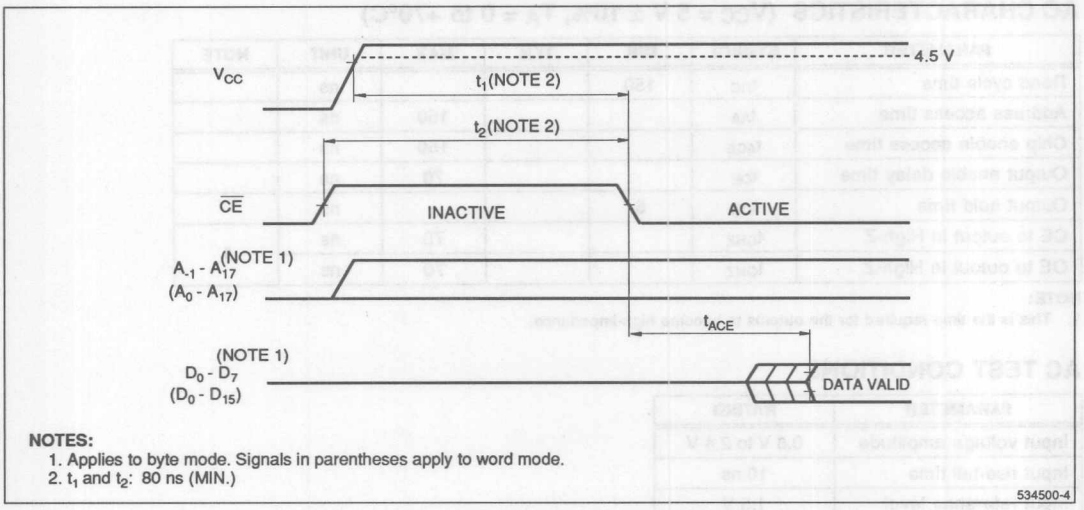


Figure 4. Timing Diagram (Power On With $\overline{CE}$ Inactive)

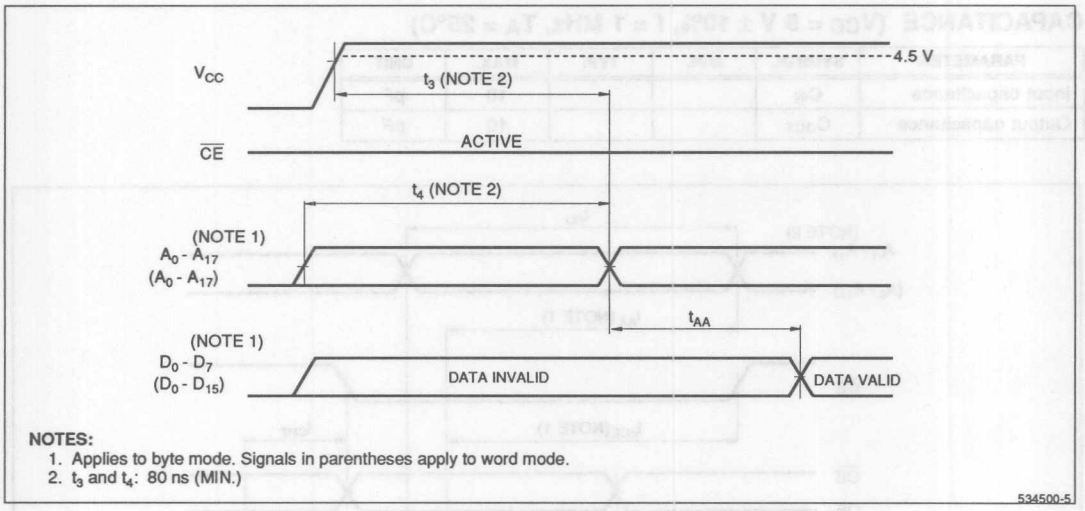
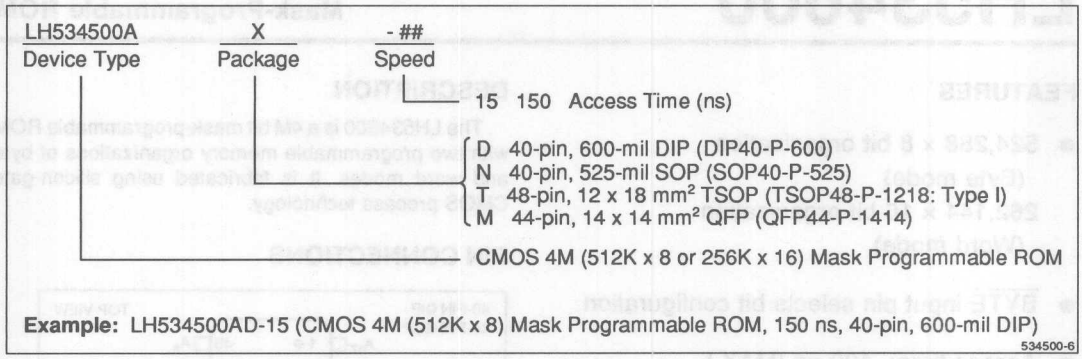


Figure 5. Timing Diagram (Power On With $\overline{CE}$ Active)

ORDERING INFORMATION



Example: LH534500AD-15 (CMOS 4M (512K x 8) Mask Programmable ROM, 150 ns, 40-pin, 600-mil DIP)

534500-6

LH534600

CMOS 4M (512K × 8 / 256K × 16) Mask-Programmable ROM

FEATURES

- 524,288 × 8 bit organization
  (Byte mode)
  262,144 × 16 bit organization
  (Word mode)
- $\overline{BYTE}$ input pin selects bit configuration
- Access time: 100 ns (MAX.)
- Low power consumption:
  Operating: 550 mW (MAX.)
  Standby: 1.65 mW (MAX.)
- Static operation (Internal sync. system)
- Automatic power down mode
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  40-pin, 600-mil DIP
  40-pin, 525-mil SOP
  44-pin, 14 × 14 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH534600 is a 4M bit mask-programmable ROM with two programmable memory organizations of byte and word modes. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

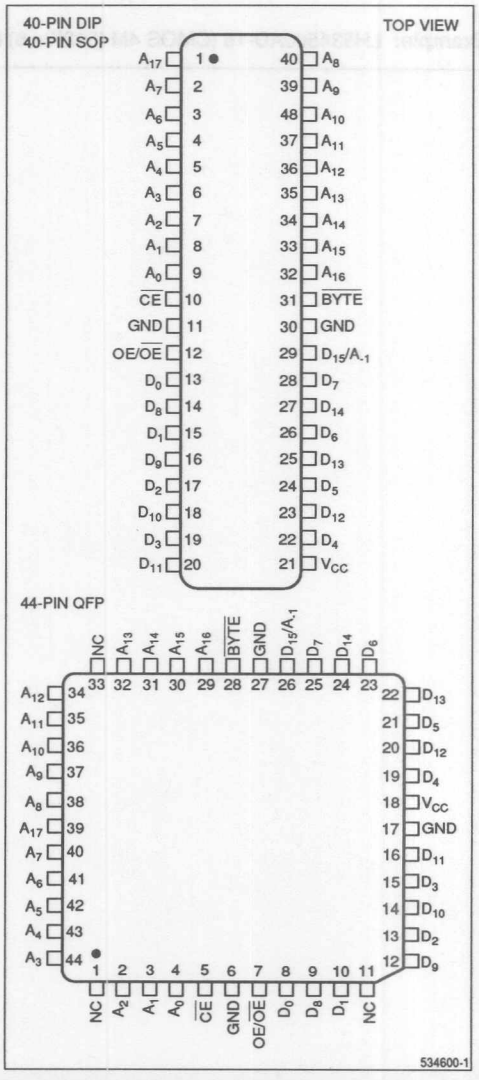


Figure 1. Pin Connections for DIP, SOP, and QFP Packages

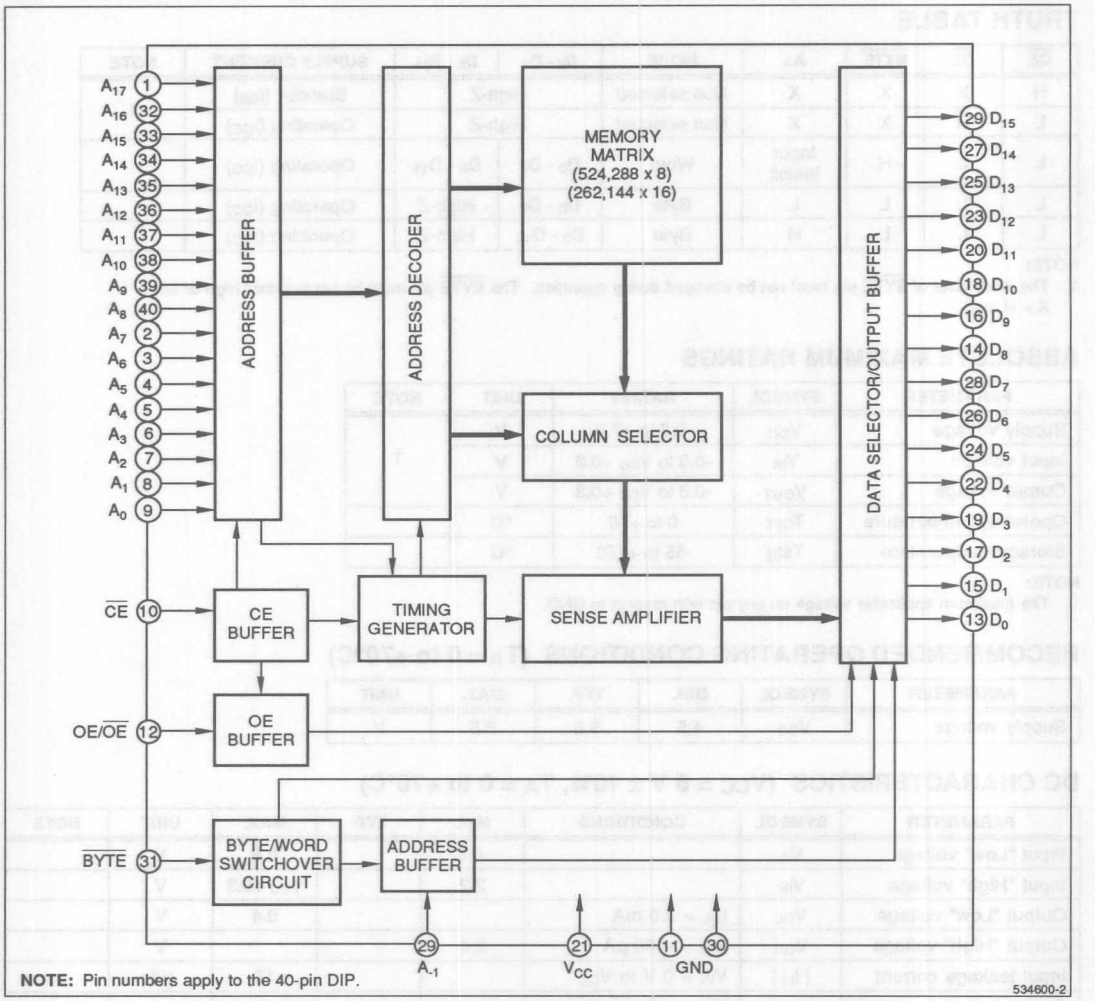


Figure 2. LH534600 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input ($\overline{BYTE}$ MODE)	1
A_0 - A_{17}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output Enable input	2
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTES:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.
2. Active level of OE/$\overline{OE}$ is mask-programmable.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT	NOTE
H	X	X	X	Non selected	High-Z		Standby (I_{SB})	1
L	H	X	X	Non selected	High-Z		Operating (I_{CC})	
L	L	H	Input inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})	
L	L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})	
L	L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})	

NOTE:
1. The input state of $\overline{BYTE}$ pin must not be changed during operation. The $\overline{BYTE}$ pin must be set to either High or Low. X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 100 ns			100	mA	2
	I_{CC2}	t_{RC} = 1 µs			70		
	I_{CC3}	t_{RC} = 100 ns			100	mA	3
	I_{CC4}	t_{RC} = 1 µs			70		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			300	µA	

NOTES:
1. OE = V_{IL}, $\overline{CE}$/$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	LH534600			UNIT	NOTE
		MIN.	TYP.	MAX.		
Read cycle time	t_{RC}	100			ns	
Address access time	t_{AA}			100	ns	
Chip enable access time	t_{ACE}			100	ns	
Output enable delay time	t_{OE}			40	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			40	ns	1
OE to ouput in High-Z	t_{OHZ}			40	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	1.5 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

CAUTION

To stabillize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

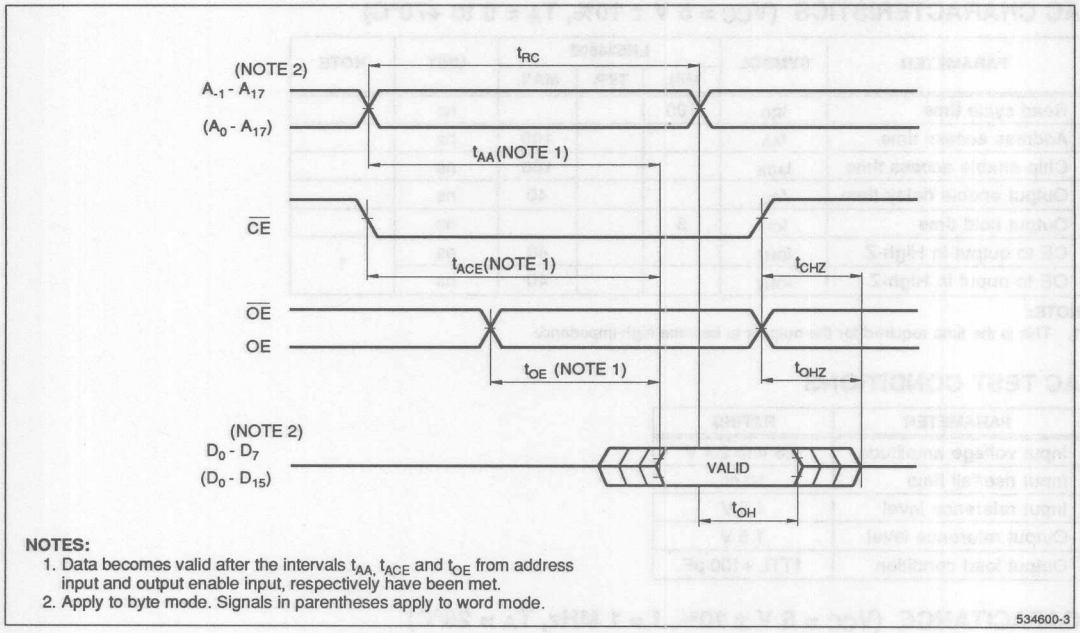
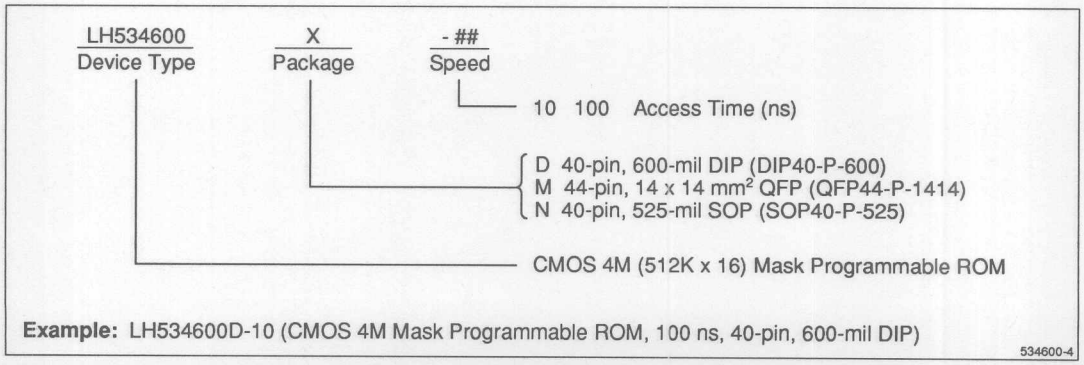


Figure 3. Timing Diagram

ORDERING INFORMATION



LH538000

CMOS 8M (1M × 8 / 512K × 16)
Mask-Programmable ROM

FEATURES

- 1,048,576 × 8 bit organization
  (Byte mode)
  524,288 × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  48-pin, 12 × 18 mm^2 TSOP (Type I)
  64-pin, 14 × 20 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH538000 is a mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{\text{BYTE}}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

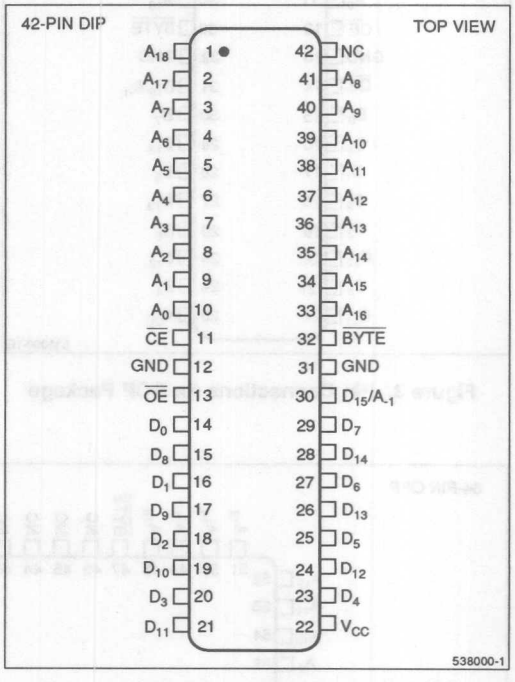


Figure 1. Pin Connections for DIP Package

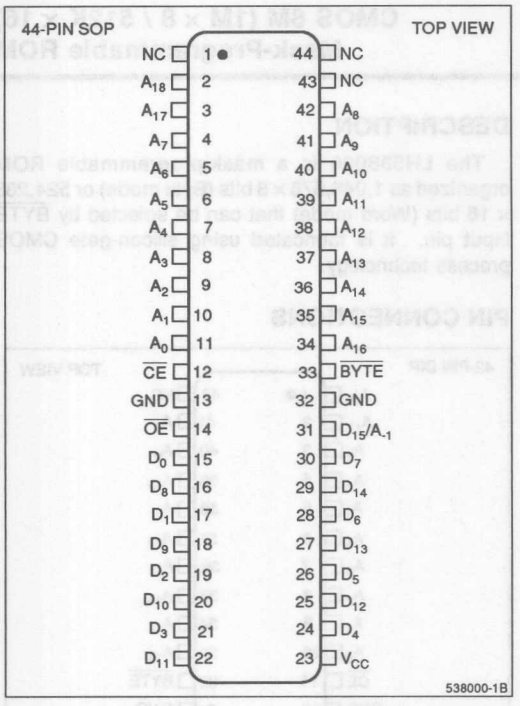


Figure 3. Pin Connections for SOP Package

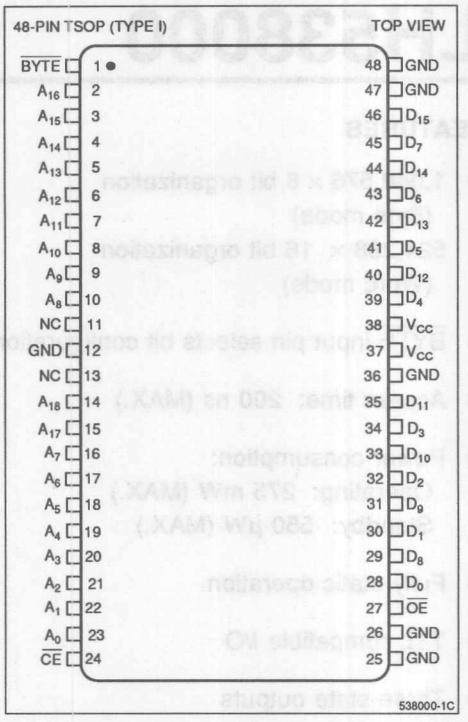


Figure 4. Pin Connections for TSOP Package

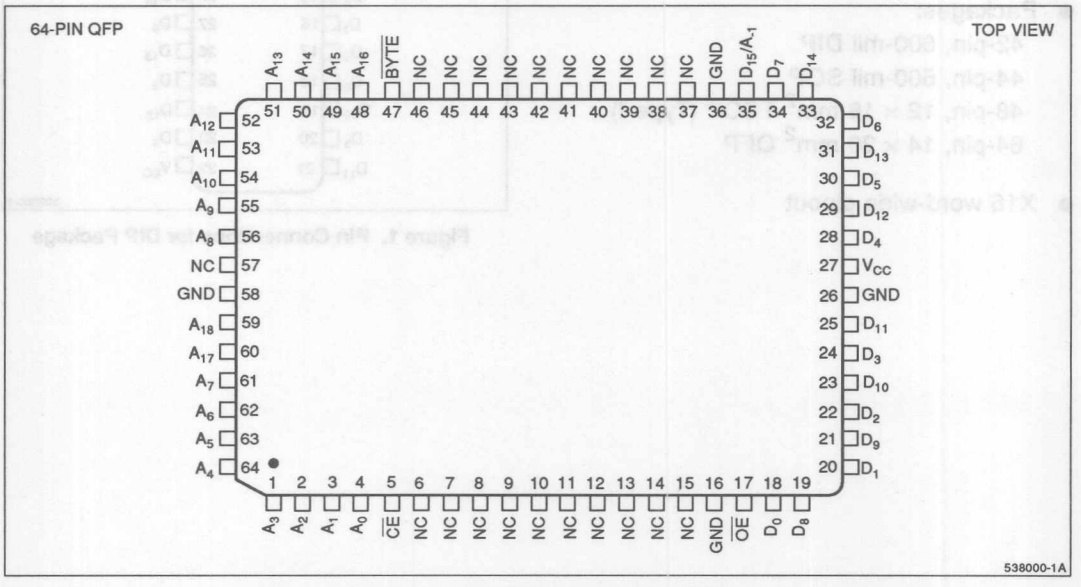


Figure 2. Pin Connections for QFP Package

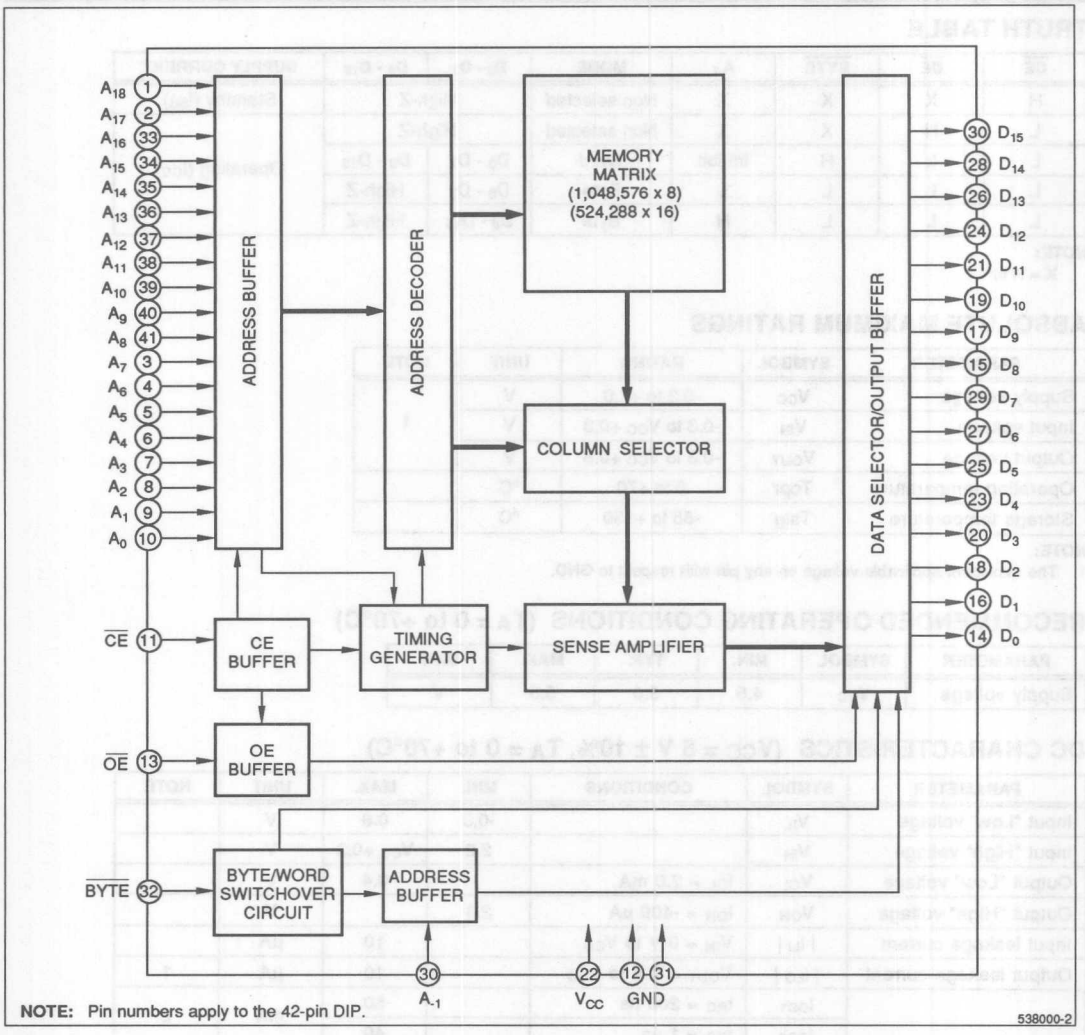


Figure 5. LH538000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (Byte Mode)	1
A_0 - A_{18}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output Enable input	
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. BYTE input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	H	X	X	Non selected	High-Z		Operating (I_{CC})
L	L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	
L	L	L	L	Byte	D_0 - D_7	High-Z	
L	L	L	H	Byte	D_8 - D_{15}	High-Z	

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Input "High" voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
	I_{CC3}	t_{RC} = 200 ns		45	mA	3
	I_{CC4}	t_{RC} = 1 µs		35		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	

NOTES:
1. $\overline{CE}$ /$\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Chip enable time	t_{ACE}		200	ns	
Output enable time	t_{OE}		80	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

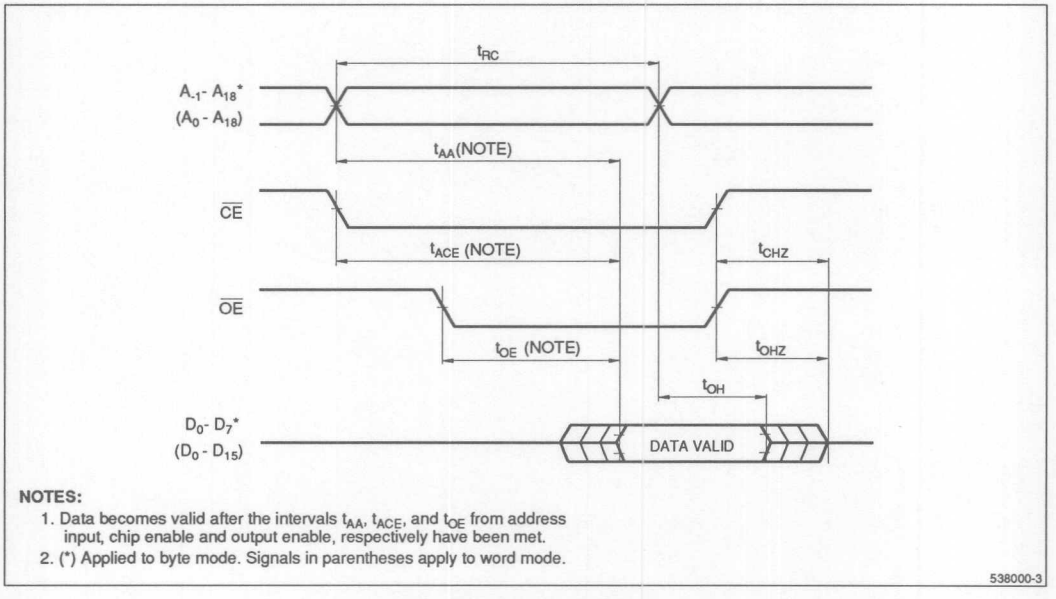
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable and output enable, respectively have been met.
2. (*) Applied to byte mode. Signals in parentheses apply to word mode.

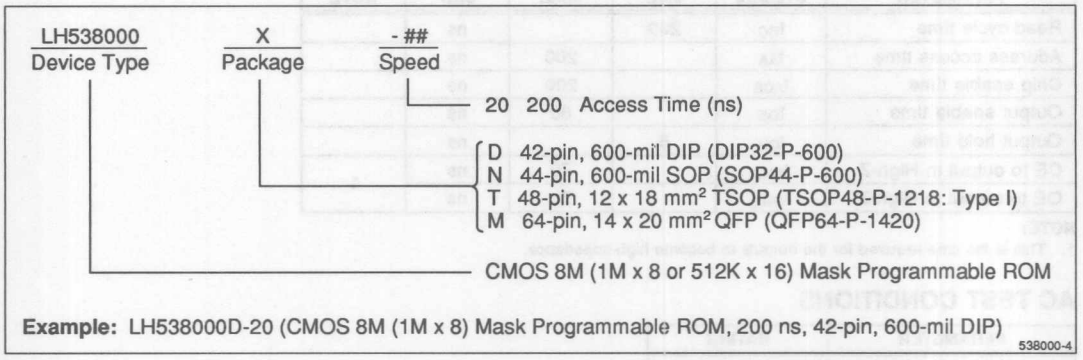
538000-3

Figure 6. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the Vcc pin and GND.

ORDERING INFORMATION



Example: LH538000D-20 (CMOS 8M (1M x 8) Mask Programmable ROM, 200 ns, 42-pin, 600-mil DIP)

538000-4

LH538100

CMOS 8M (1M × 8) Mask-Programmable ROM

FEATURES

- 1,048,576 × 8 bit organization
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 500 µW (MAX.)
- Programmable output enable
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  32-pin, 600-mil DIP
  32-pin, 525-mil SOP
- JEDEC standard EPROM pinout (DIP)

DESCRIPTION

The LH538100 is a mask-programmable ROM organized as 1,048,576 × 8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

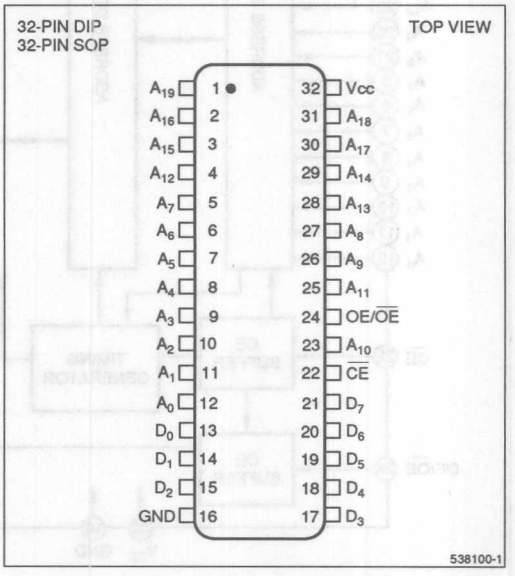


Figure 1. Pin Connections for DIP and SOP Packages

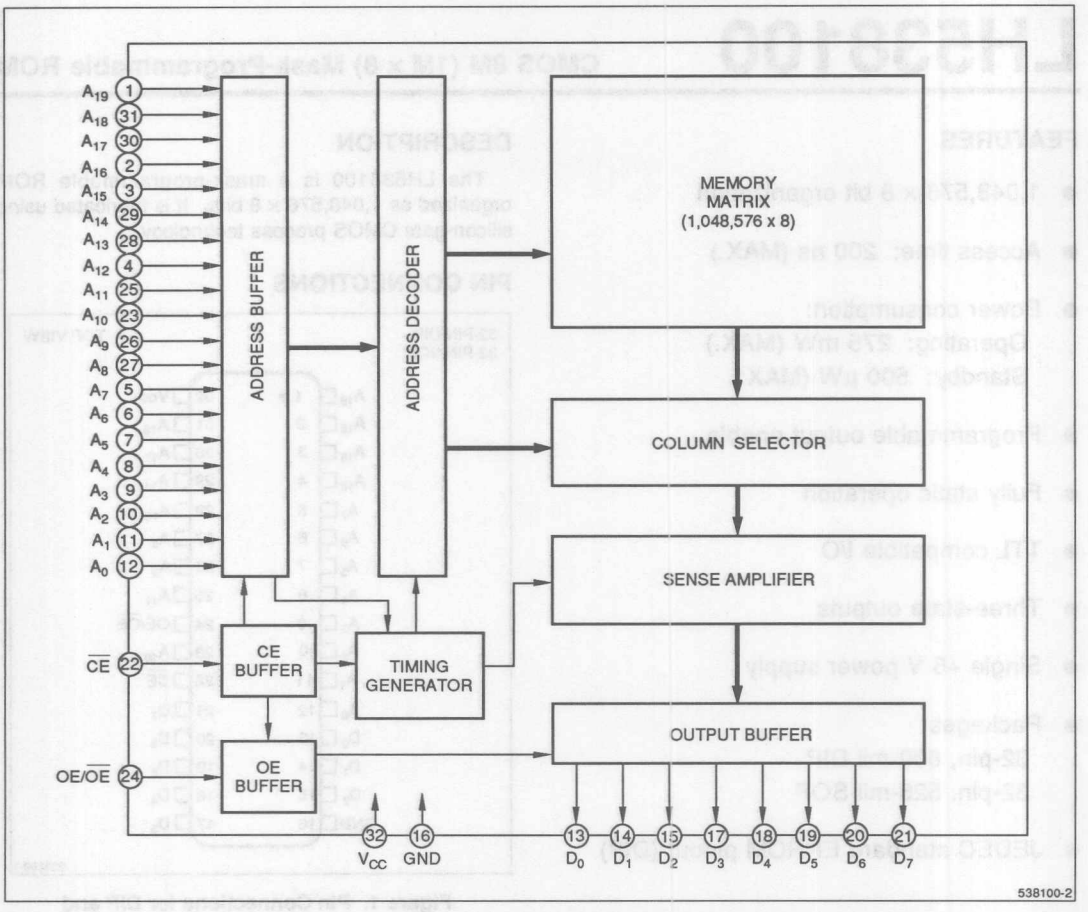


Figure 2. LH538100 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_0 - A_{19}	Address input	
D_0 - D_7	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
OE/$\overline{OE}$	Output Enable input	1
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:
1. The active level of OE/$\overline{OE}$ is mask programmable.

TRUTH TABLE

$\overline{CE}$	OE/$\overline{OE}$	MODE	D_0 - D_7	SUPPLY CURRENT
H	X	Non selected	High-Z	Standby (I_{SB})
L	L/H	Non selected	High-Z	Operating (I_{CC})
L	H/L	Selected	D_{OUT}	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3		0.8	V	
Input "High" voltage	V_{IH}		2.2		V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA			0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4			V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}			10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}			10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns			50	mA	2
	I_{CC2}	t_{RC} = 1 µs			40		
	I_{CC3}	t_{RC} = 200 ns			45	mA	3
	I_{CC4}	t_{RC} = 1 µs			35		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V			100	µA	

NOTES:
1. $\overline{CE}$ = V_{IH} or OE/$\overline{OE}$ = V_{IL}/V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200			ns	
Address access time	t_{AA}			200	ns	
Chip enable time	t_{ACE}			200	ns	
Output enable time	t_{OE}	10		80	ns	
Output hold time	t_{OH}	5			ns	
CE to output in High-Z	t_{CHZ}			70	ns	1
OE to output in High-Z	t_{OHZ}			70	ns	

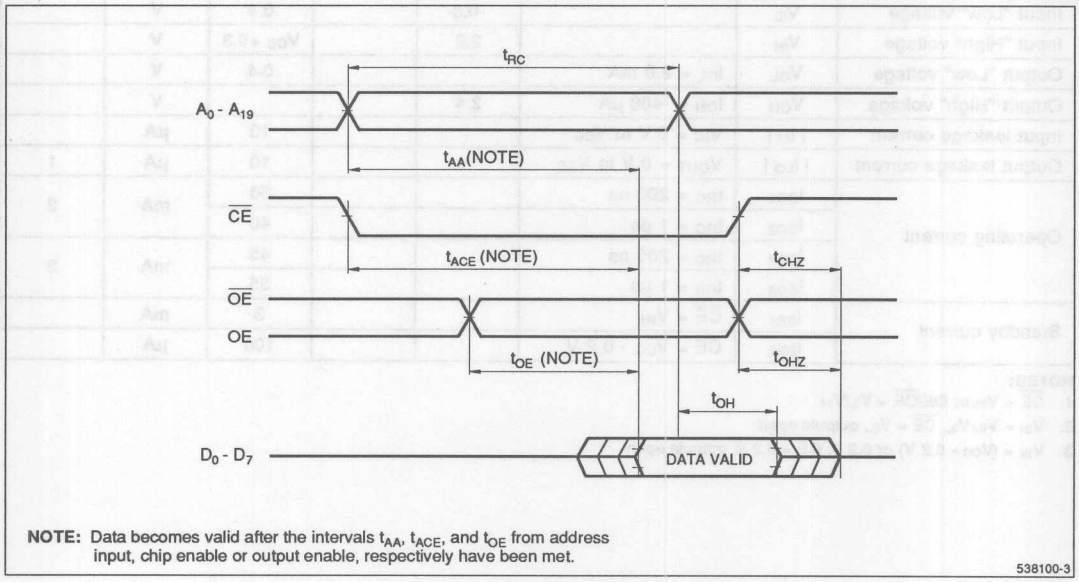
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTE: Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively have been met.

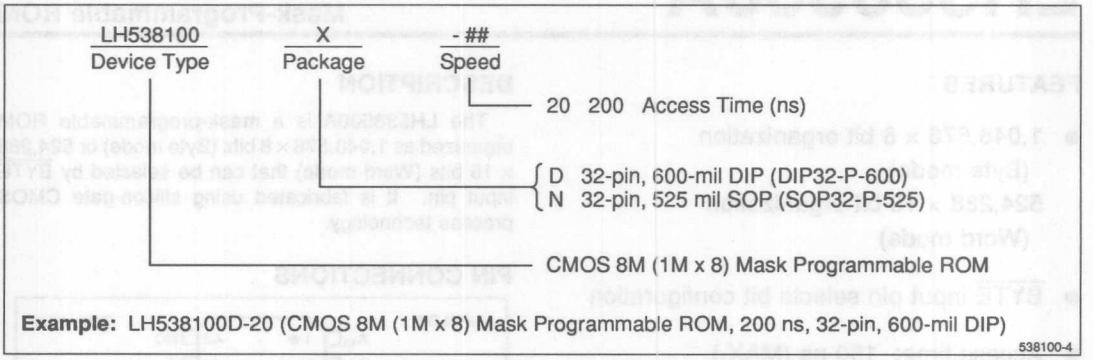
538100-3

Figure 3. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and the GND pin.

ORDERING INFORMATION



LH538500A

CMOS 8M (1M × 8 / 512K × 16) Mask-Programmable ROM

FEATURES

- 1,048,576 × 8 bit organization
  (Byte mode)
  524,288 × 16 bit organization
  (Word mode)
- $\overline{BYTE}$ input pin selects bit configuration
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP
  44-pin, 600-mil SOP
  44-pin, 14 × 14 mm^2 QFP
  64-pin, 14 × 20 mm^2 QFP
  48-pin, 12 × 18 mm^2 TSOP I
- X16 word-wide pinout

DESCRIPTION

The LH538500A is a mask-programmable ROM organized as 1,048,576 × 8 bits (Byte mode) or 524,288 × 16 bits (Word mode) that can be selected by $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

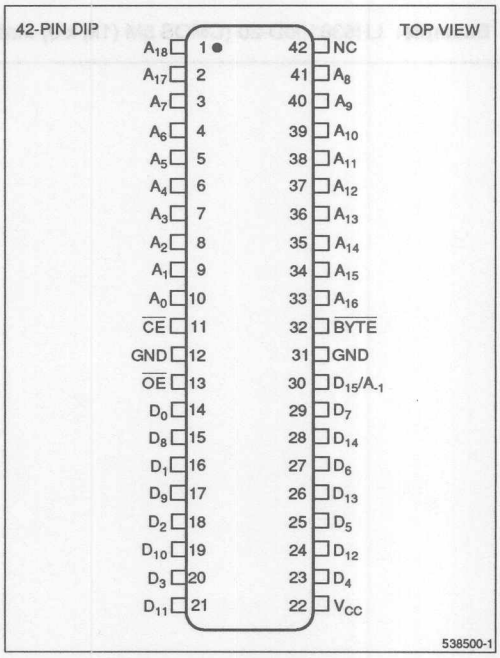


Figure 1. Pin Connections for DIP Package

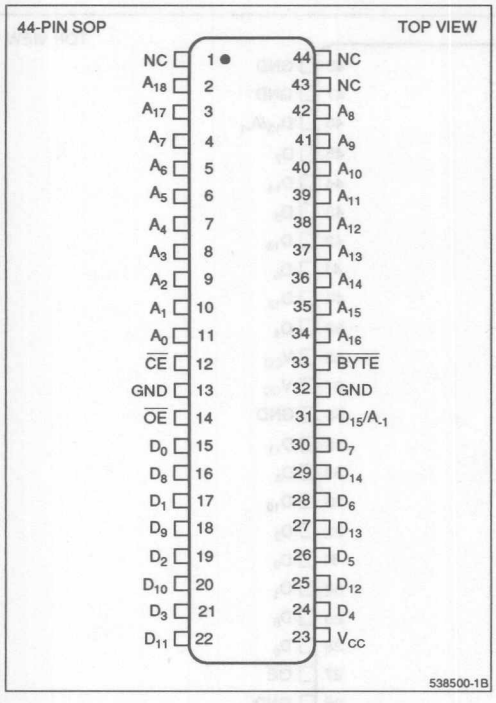


Figure 2. Pin Connections for SOP Package

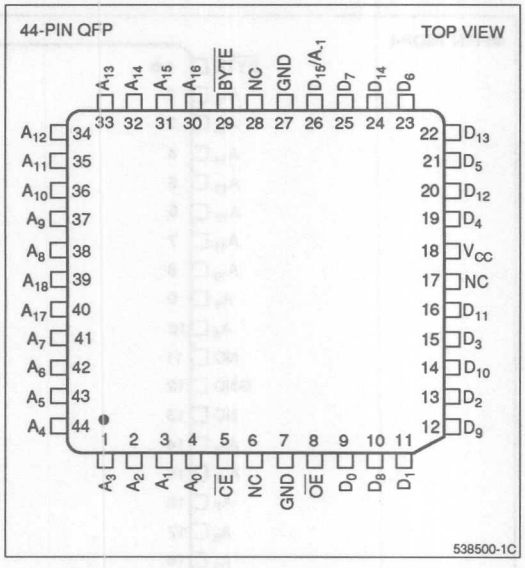


Figure 3. Pin Connections for 44-Pin QFP

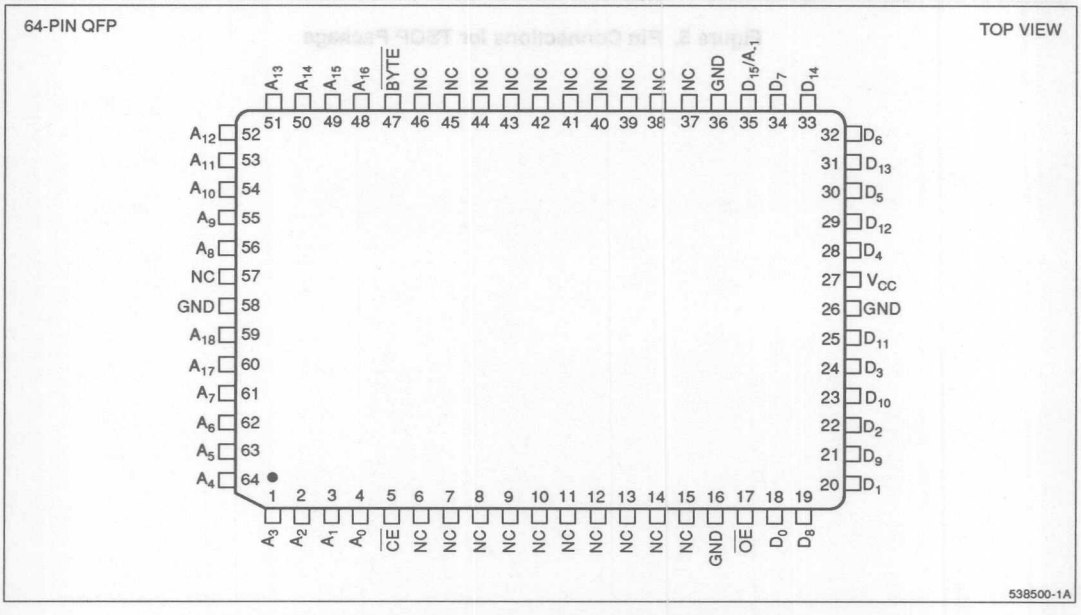


Figure 4. Pin Connections for 64-Pin QFP Package

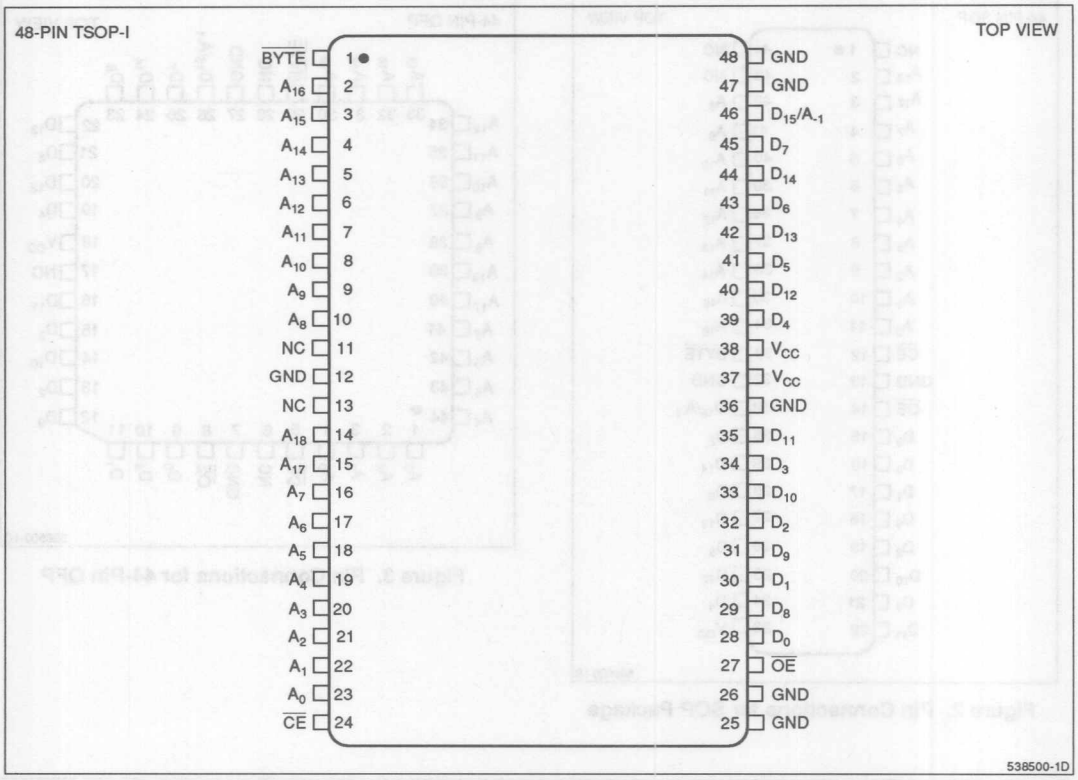


Figure 5. Pin Connections for TSOP Package

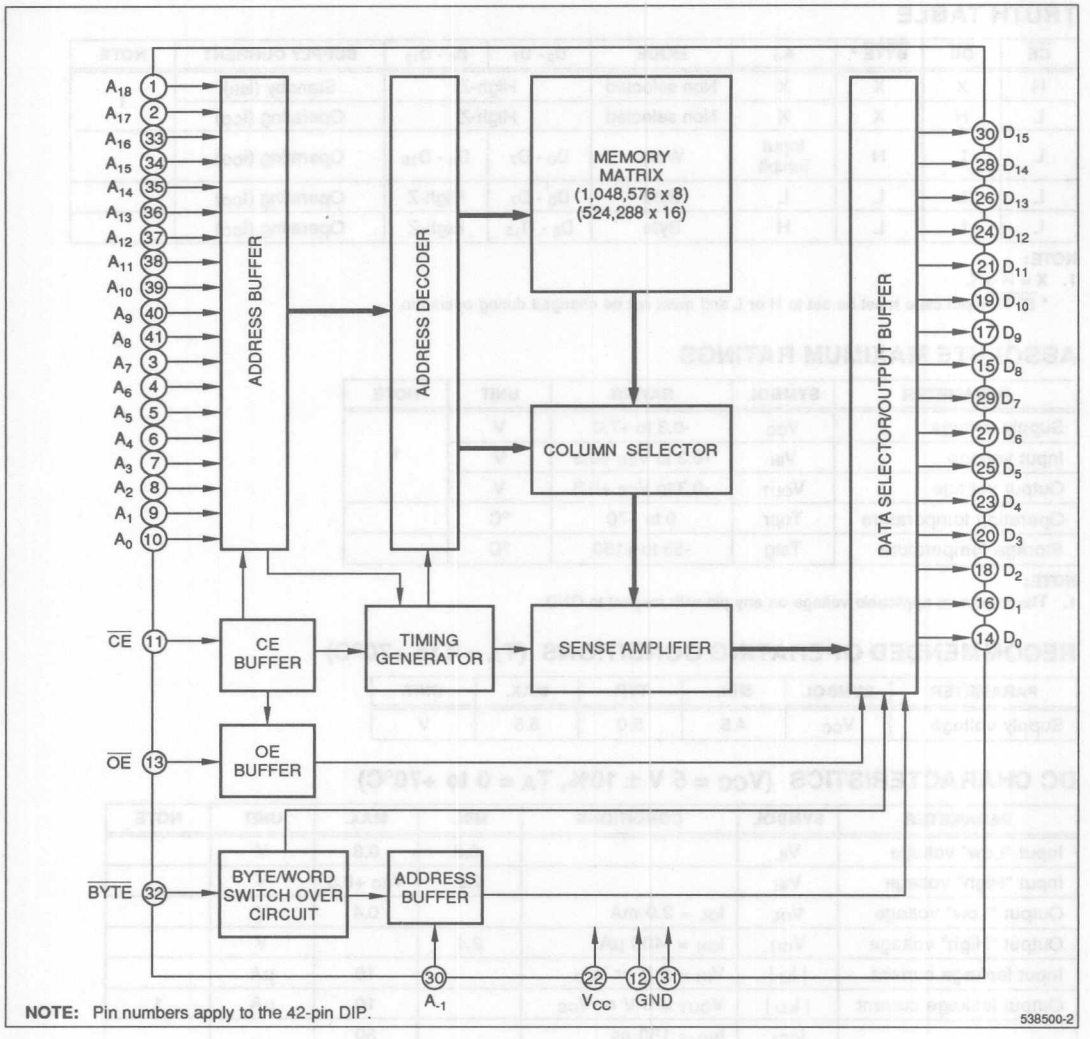


Figure 6. LH538500A Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (Byte mode)	1
A_0 - A_{18}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	
$\overline{OE}$	Output Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set to byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration..

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$ *	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT	NOTE
H	X	X	X	Non selected	High-Z		Standby (I_{SB})	1
L	H	X	X	Non selected	High-Z		Operating (I_{CC})	
L	L	H	Input inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})	
L	L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})	
L	L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})	

NOTE:
1. X = H or L
   * $\overline{BYTE}$ input state must be set to H or L and must not be changed during operation.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Input "High" voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V or V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V or V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable time	t_{ACE}		150	ns	
Output enable time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

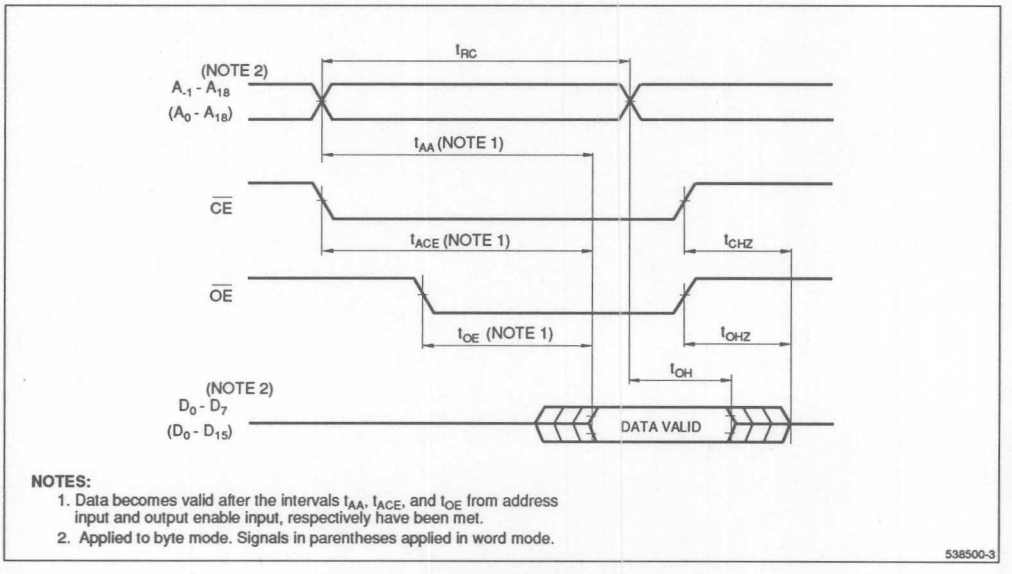
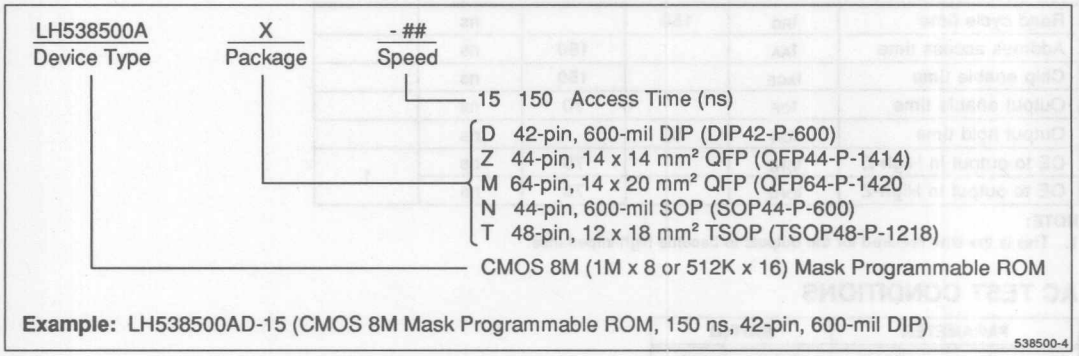


Figure 7. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

ORDERING INFORMATION



LH5316000

CMOS 16M (2M × 8 / 1M × 16)
Mask-Programmable ROM

FEATURES

- 2,097,152 × 8 bit organization
  (Byte mode)
  1,048,576 × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  64-pin, 750-mil SDIP
  64-pin, 14 × 20 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH5316000 is a mask-programmable ROM organized as 2,097,152 × 8 bits (Byte mode) or 1,048,576 × 16 bits (Word mode) that can be selected by an input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

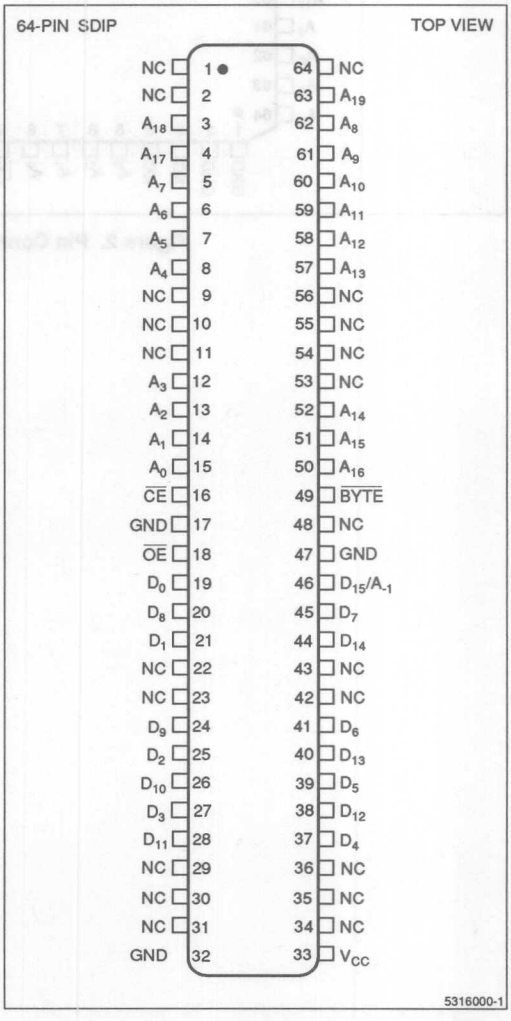


Figure 1. Pin Connections for SDIP Package

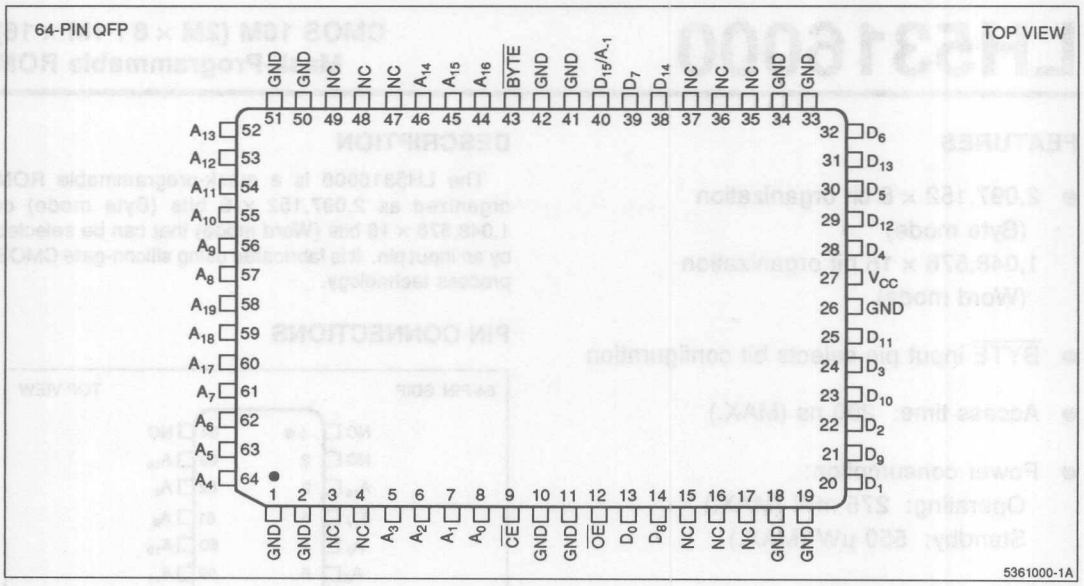


Figure 2. Pin Connections for QFP Package

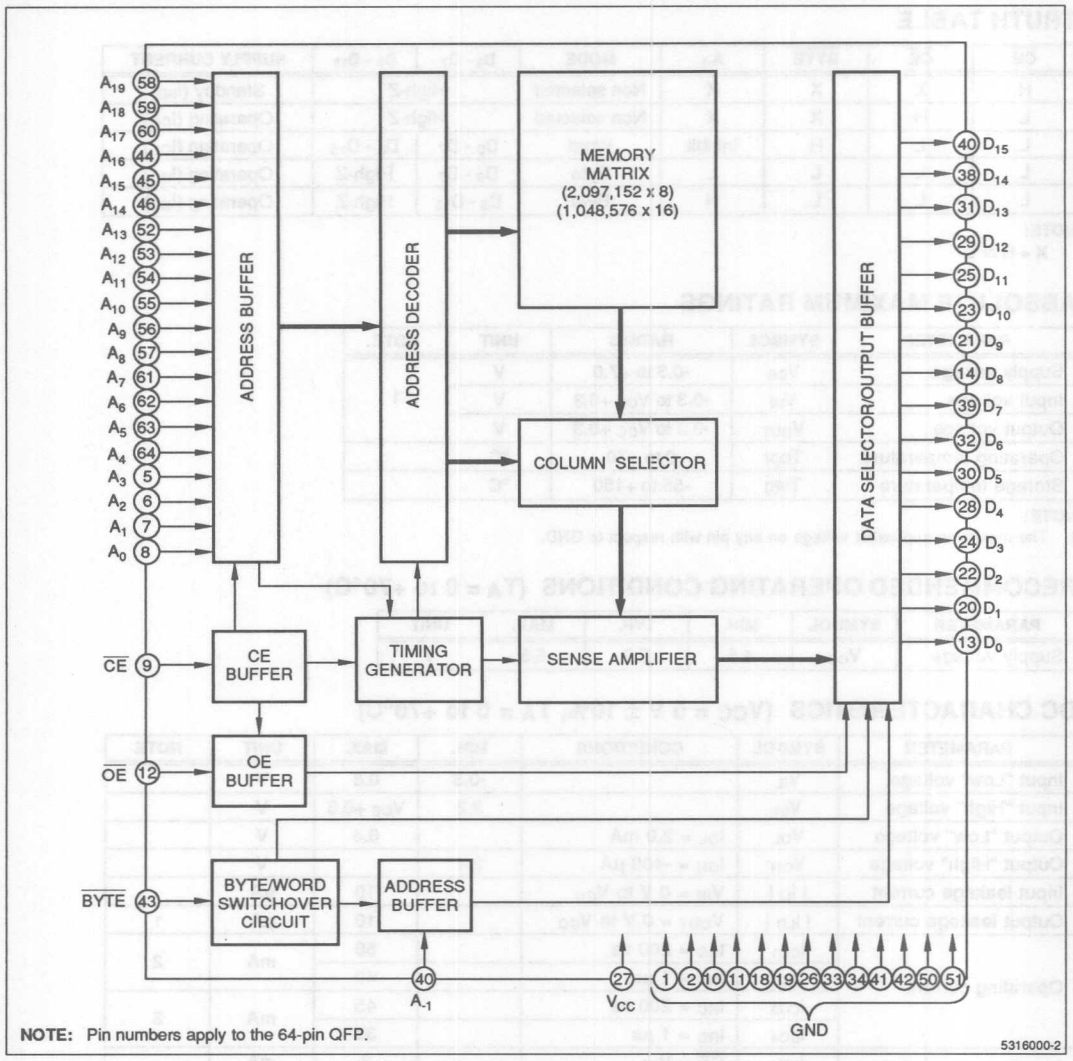


Figure 3. LH5316000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (Byte Mode)	1
A_0 - A_{19}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output Enable input	
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set in byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT
H	X	X	X	Non selected	High-Z		Standby (I_{SB})
L	H	X	X	Non selected	High-Z		Operating (I_{CC})
L	L	H	Inhibit	Word	D_0 - D_7	D_8 - D_{15}	Operating (I_{CC})
L	L	L	L	Byte	D_0 - D_7	High-Z	Operating (I_{CC})
L	L	L	H	Byte	D_8 - D_{15}	High-Z	Operating (I_{CC})

NOTE:
X = H or L

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Input "High" voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V to V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V to V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
	I_{CC3}	t_{RC} = 200 ns		45	mA	3
	I_{CC4}	t_{RC} = 1 µs		35		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		3	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	

NOTES:
1. $\overline{CE}$ /$\overline{OE}$ = V_{IH}.
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open.
3. V_{IN} = (V_{CC} - 0.2 V) or 0.2 V, $\overline{CE}$ = 0.2 V, outputs open.

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Chip enable time	t_{ACE}		200	ns	
Output enable time	t_{OE}		80	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF

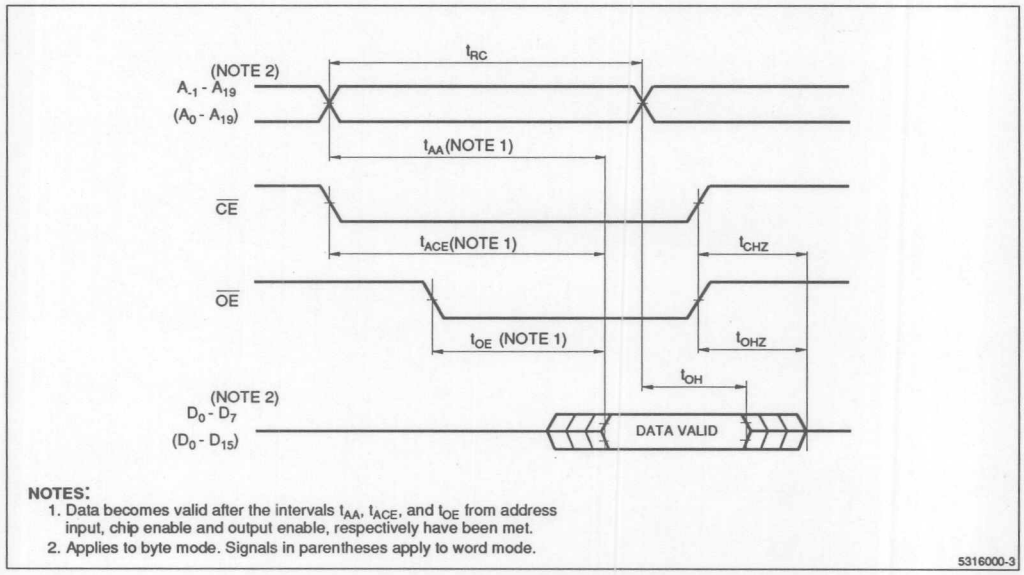
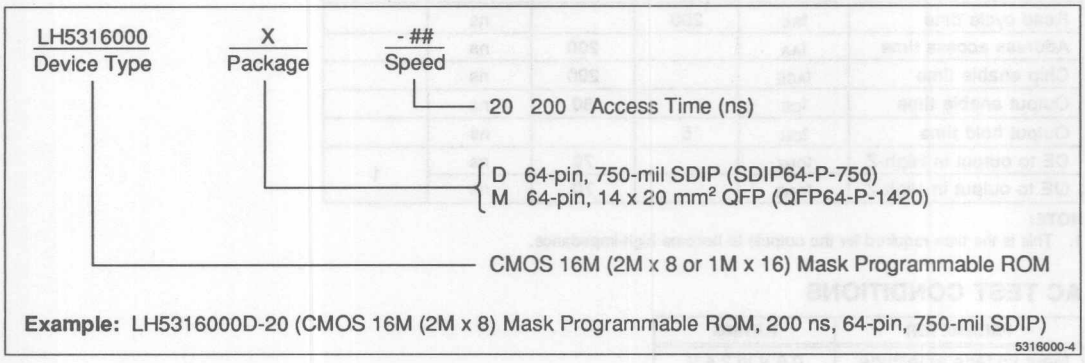


Figure 4. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

ORDERING INFORMATION



LH5316500

CMOS 16M (2M × 8 / 1M × 16)
Mask-Programmable ROM

FEATURES

- 2,097,152 × 8 bit organization
  (Byte mode: $\overline{BYTE}$ = V_{IL})
  1,048,576 × 16 bit organization
  (Word mode: $\overline{BYTE}$ = V_{IH})
- Access time: 150 ns (MAX.)
- Power consumption:
  Operating: 50 mA (MAX.)
  Standby: 100 µA (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  42-pin, 600-mil DIP *
  44-pin, 600-mil SOP
  48-pin, 12 × 18 TSOP I
  64-pin, 14 × 20 mm^2 QFP

PIN CONNECTIONS

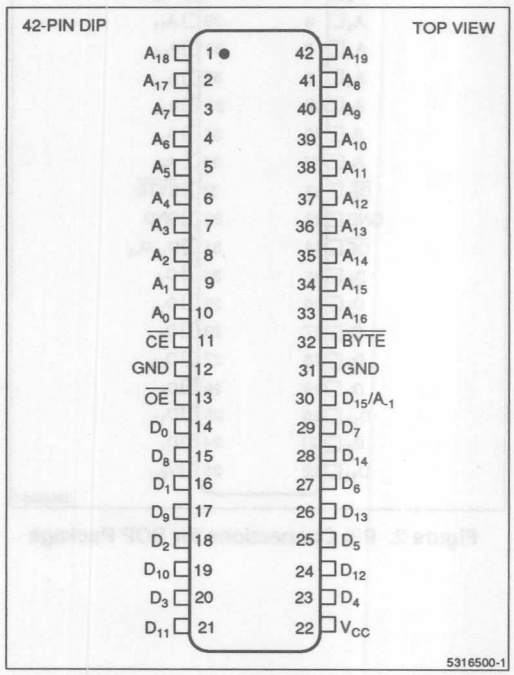


Figure 1. Pin Connections for DIP Package

DESCRIPTION

The LH5316500 is a 16M-bit mask-programmable ROM organized as 2,097,152 × 8 bits (Byte mode) or 1,048,576 × 16 bits (Word mode) that can be selected by a $\overline{BYTE}$ input pin. It is fabricated using silicon-gate CMOS process technology.

It provides high density and high speed access in a variety of packages including small and thin surface mount technology.

* NOTE: For the 42-pin DIP, pin 30 becomes LSB address input (A_{-1}) when in byte mode, and data output (D_{15}) when in word mode.

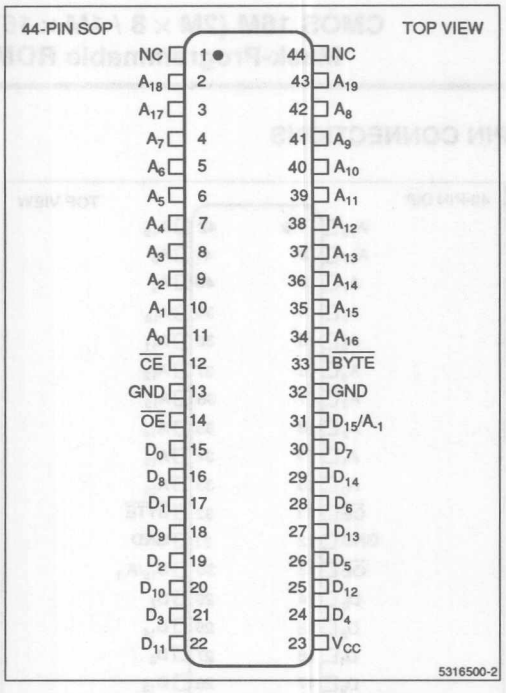


Figure 2. Pin Connections for SOP Package

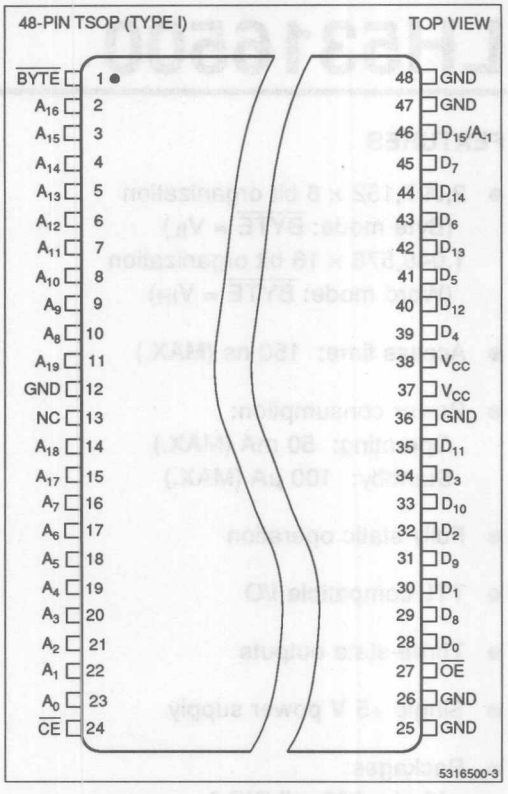


Figure 3. Pin Connections for TSOP Package (Type I)

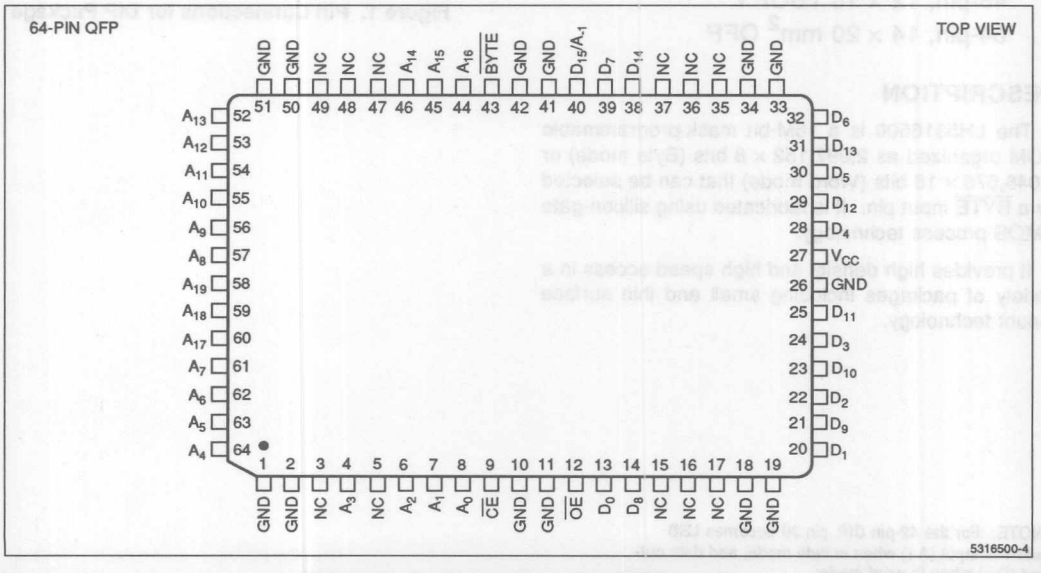


Figure 4. Pin Connections for QFP Package

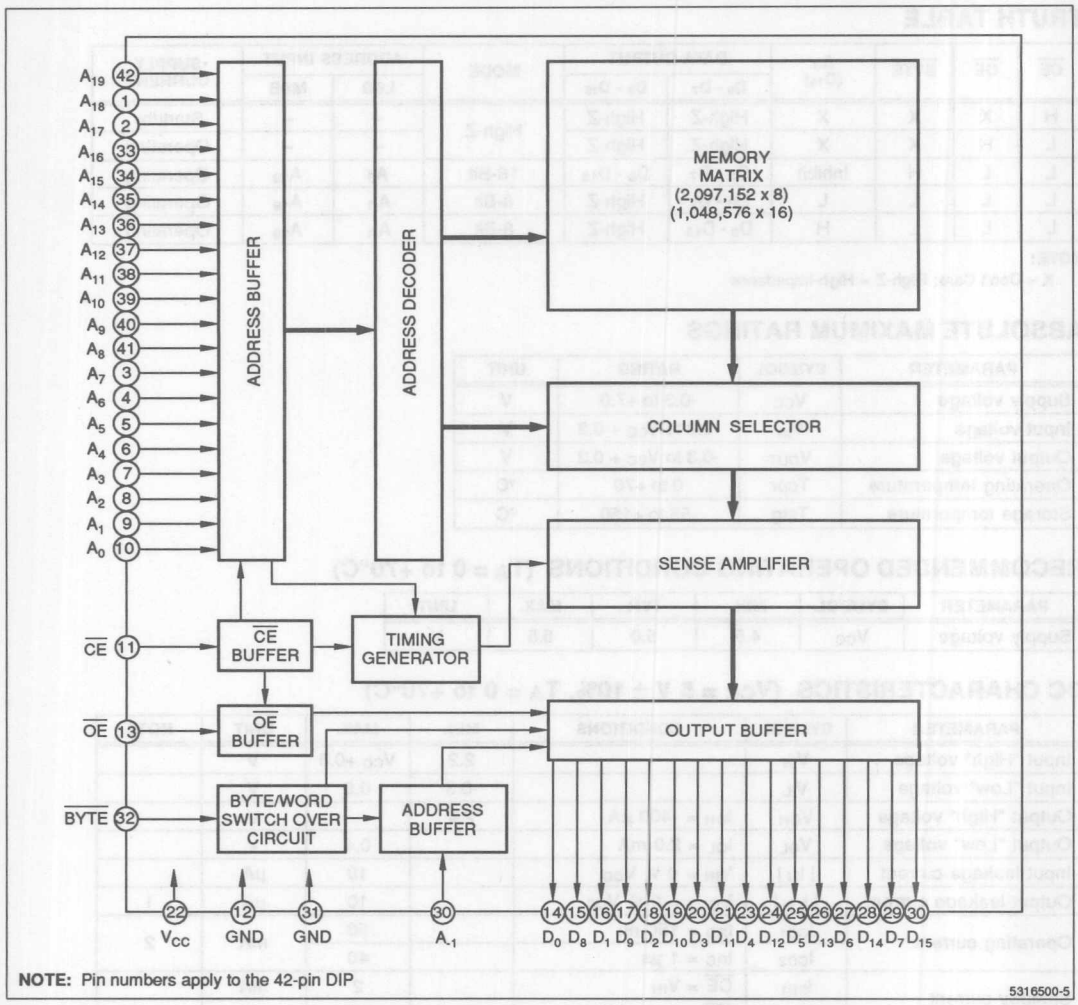


Figure 5. LH5316500 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_{-1} - A_{19}	Address input
D_0 - D_{15}	Data output
$\overline{BYTE}$	8/16-bit (Byte/Word) mode switch input
$\overline{CE}$	Chip Enable input

SIGNAL	PIN NAME
$\overline{OE}$	Output Enable input
V_{CC}	Power supply (+5 V)
GND	Ground
NC	No Connection

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$	A_{-1} (D_{15})	DATA OUTPUT		MODE	ADDRESS INPUT		SUPPLY CURRENT
				D_0 - D_7	D_8 - D_{15}		LSB	MSB	
H	X	X	X	High-Z	High-Z	High-Z	–	–	Standby
L	H	X	X	High-Z	High-Z		–	–	Operating
L	L	H	Inhibit	D_0 - D_7	D_8 - D_{15}	16-Bit	A_0	A_{19}	Operating
L	L	L	L	D_0 - D_7	High-Z	8-Bit	A_{-1}	A_{19}	Operating
L	L	L	H	D_8 - D_{15}	High-Z	8-Bit	A_{-1}	A_{19}	Operating

NOTE:
X = Don't Care; High-Z = High-Impedance

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
Supply voltage	V_{CC}	-0.3 to +7.0	V
Input voltage	V_{IN}	-0.3 to V_{CC} + 0.3	V
Output voltage	V_{OUT}	-0.3 to V_{CC} + 0.3	V
Operating temperature	Topr	0 to +70	°C
Storage temperature	Tstg	-55 to +150	°C

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "High" voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V, V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V, V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 150 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	
Input capacitance	C_{IN}	f = 1 MHz, t_A = 25°C		10	pF	
Output capacitance	C_{OUT}			10	pF	

NOTES:
1. $\overline{CE}$ = V_{IH}, $\overline{OE}$ = V_{IH} (Outputs open).
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL} (TTL level).

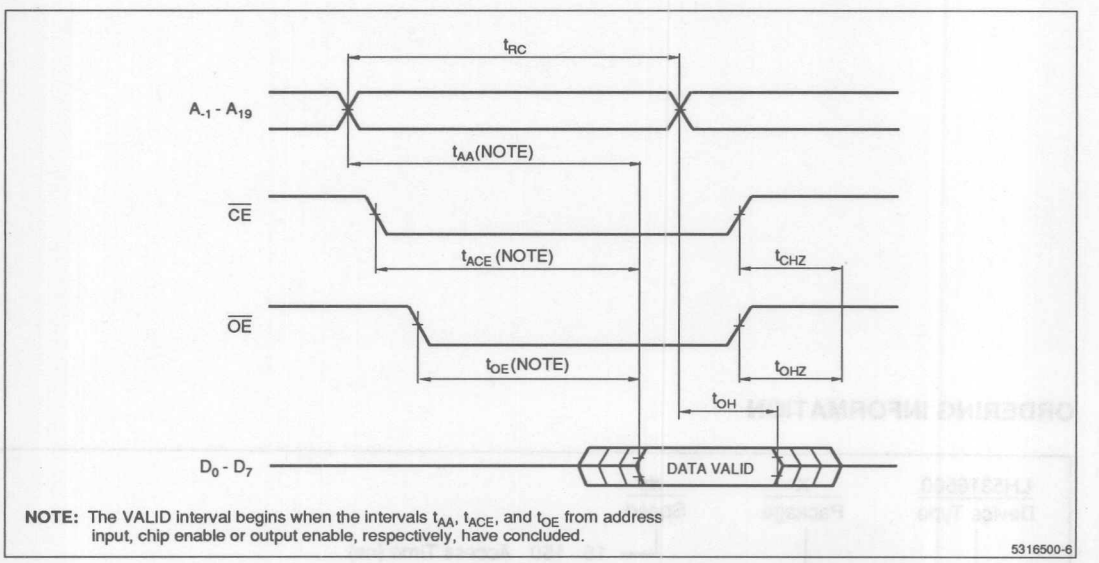
AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	150		ns	
Address access time	t_{AA}		150	ns	
Chip enable access time	t_{ACE}		150	ns	
Output enable time	t_{OE}		70	ns	
Output hold time	t_{OH}	5		ns	
Output floating time	t_{CHZ}		60	ns	1
	t_{OHZ}				

NOTE:
1. Determined by the time for the output to be opened, irrespective of output voltage.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V, 2.2 V
Output load condition	1TTL + 100 pF



NOTE: The VALID interval begins when the intervals t_{AA}, t_{ACE}, and t_{OE} from address input, chip enable or output enable, respectively, have concluded.

5316500-6

Figure 6. $\overline{BYTE}$ = V_{IL} in Byte Mode

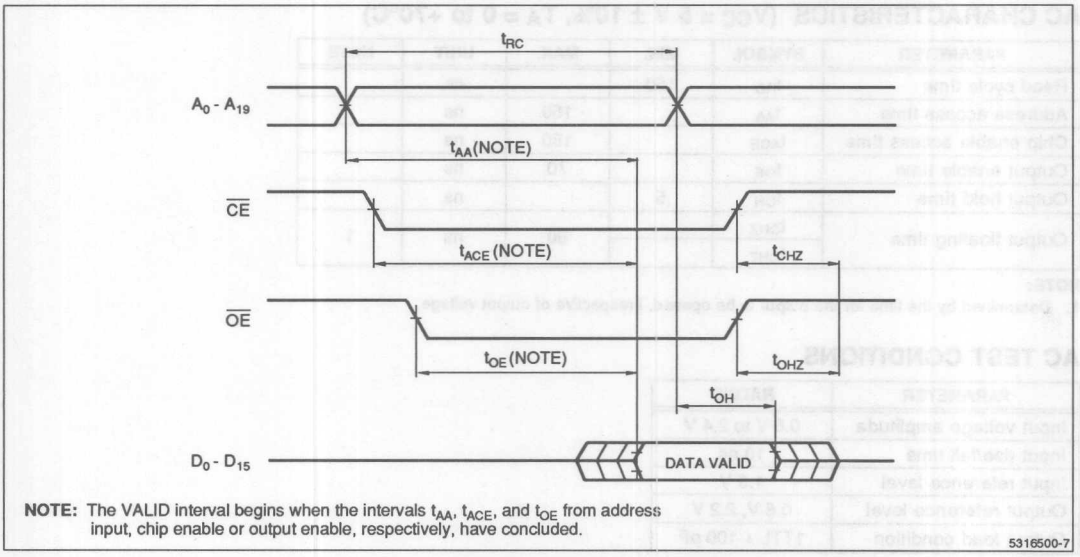
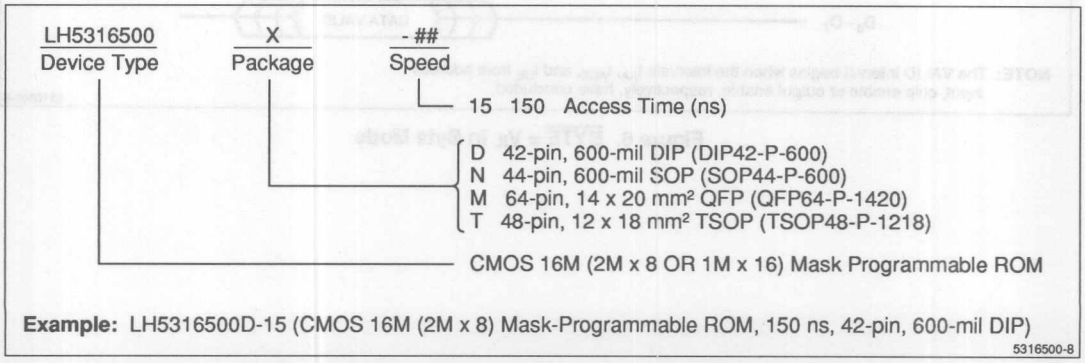


Figure 7. $\overline{BYTE}$ = V_{IH} in Word Mode

ORDERING INFORMATION



PRELIMINARY

LH5332000

CMOS 32M (4M × 8 / 2M × 16)
Mask-Programmable ROM

FEATURES

- 4,194,304 × 8 bit organization
  (Byte mode)
  2,097,152 × 16 bit organization
  (Word mode)
- $\overline{\text{BYTE}}$ input pin selects bit configuration
- Access time: 200 ns (MAX.)
- Power consumption:
  Operating: 275 mW (MAX.)
  Standby: 550 µW (MAX.)
- Fully static operation
- TTL compatible I/O
- Three-state outputs
- Single +5 V power supply
- Packages:
  44-pin, 600-mil SOP
  64-pin, 14 × 20 mm^2 QFP
- X16 word-wide pinout

DESCRIPTION

The LH5332000 is a mask-programmable ROM organized as 4,194,304 × 8 bits (Byte mode) or 2,097,152 × 16 bits (Word mode) that can be selected by input pin. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

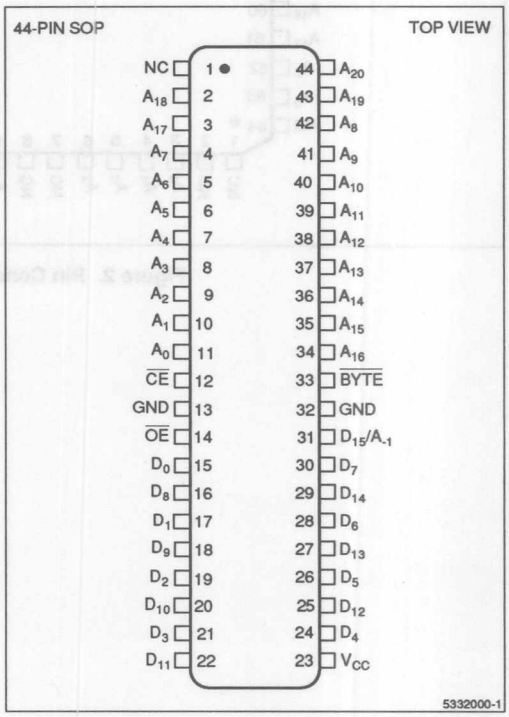


Figure 1. Pin Connections for SOP Package

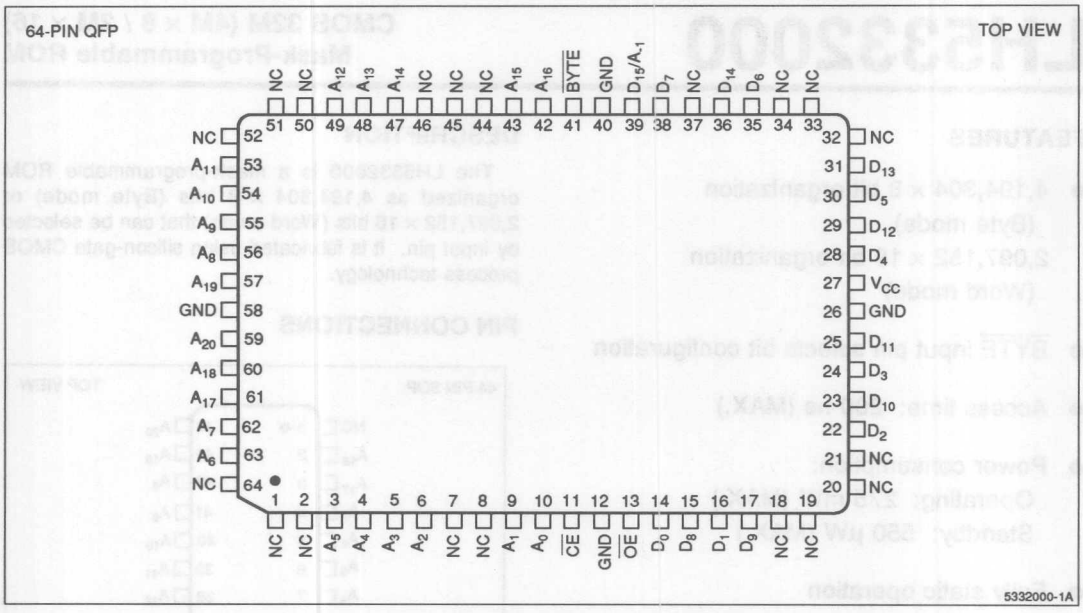


Figure 2. Pin Connections for QFP Package

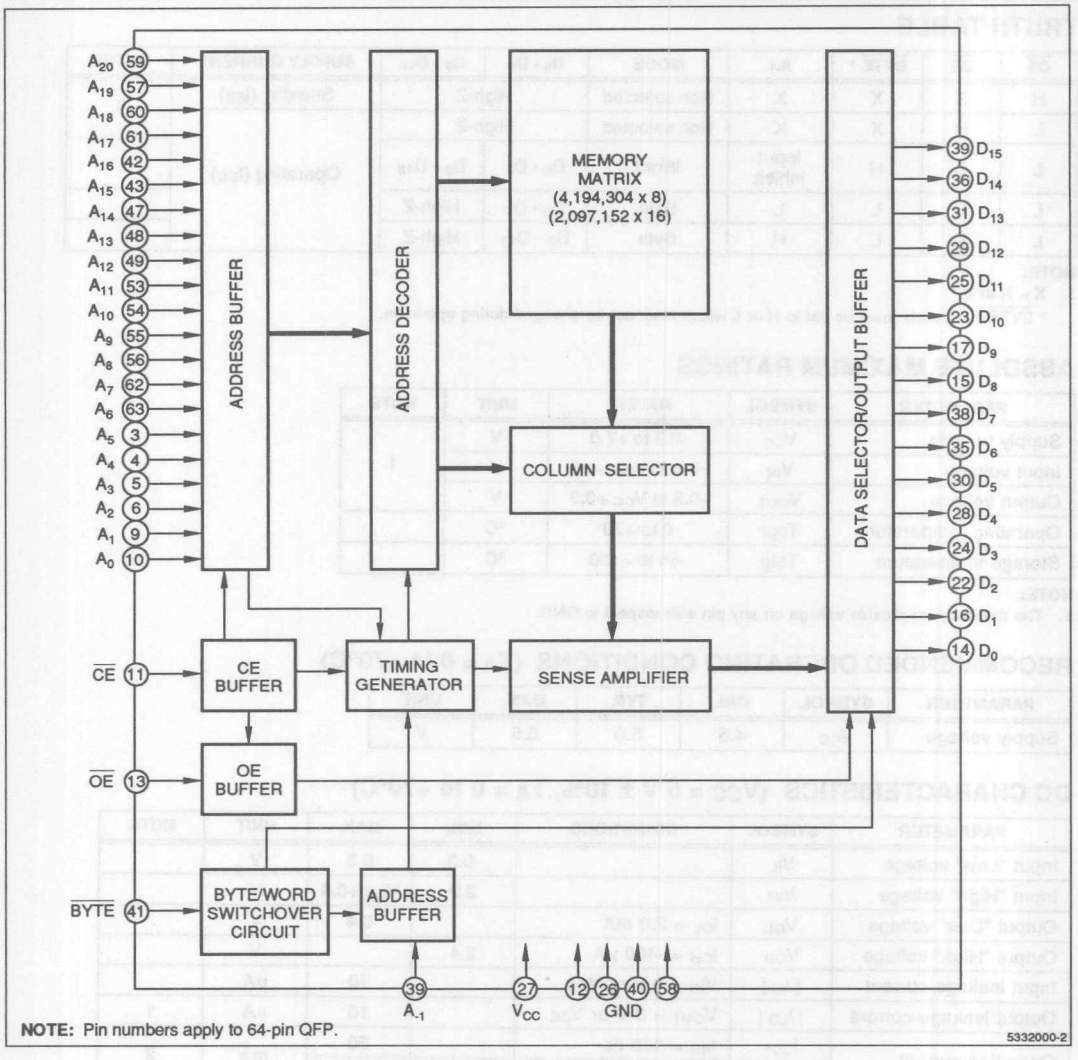


Figure 3. LH5332000 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME	NOTE
A_{-1}	Address input (Byte mode)	1
A_0 - A_{20}	Address input	
D_0 - D_{15}	Data output	
$\overline{CE}$	Chip Enable input	

SIGNAL	PIN NAME	NOTE
$\overline{OE}$	Output Enable input	
$\overline{BYTE}$	Byte/word switch	
V_{CC}	Power supply (+5 V)	
GND	Ground	

NOTE:

1. D_{15}/A_{-1} pin becomes LSB address input (A_{-1}) when the bit configuration is set to byte mode, and data output (D_{15}) when in word mode. $\overline{BYTE}$ input pin selects bit configuration.

TRUTH TABLE

$\overline{CE}$	$\overline{OE}$	$\overline{BYTE}$ *	A_{-1}	MODE	D_0 - D_7	D_8 - D_{15}	SUPPLY CURRENT	NOTE
H	X	X	X	Non selected	High-Z		Standby (I_{SB})	1
L	H	X	X	Non selected	High-Z		Operating (I_{CC})	
L	L	H	Input inhibit	Word	D_0 - D_7	D_8 - D_{15}		
L	L	L	L	Byte	D_0 - D_7	High-Z		
L	L	L	H	Byte	D_8 - D_{15}	High-Z		

NOTE:
1. X = H or L
   * $\overline{BYTE}$ input state must be set to H or L which must not be changed during operation.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to V_{CC} +0.3	V	
Output voltage	V_{OUT}	-0.3 to V_{CC} +0.3	V	
Operating temperature	Topr	0 to +70	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTE:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		-0.3	0.8	V	
Input "High" voltage	V_{IH}		2.2	V_{CC} +0.3	V	
Output "Low" voltage	V_{OL}	I_{OL} = 2.0 mA		0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -400 µA	2.4		V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN} = 0 V or V_{CC}		10	µA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT} = 0 V or V_{CC}		10	µA	1
Operating current	I_{CC1}	t_{RC} = 200 ns		50	mA	2
	I_{CC2}	t_{RC} = 1 µs		40		
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}		2	mA	
	I_{SB2}	$\overline{CE}$ = V_{CC} - 0.2 V		100	µA	

NOTES:
1. $\overline{CE}/\overline{OE}$ = V_{IH}
2. V_{IN} = V_{IH}/V_{IL}, $\overline{CE}$ = V_{IL}, outputs open

AC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = 0 to +70°C)

PARAMETER	SYMBOL	MIN.	MAX.	UNIT	NOTE
Read cycle time	t_{RC}	200		ns	
Address access time	t_{AA}		200	ns	
Chip enable time	t_{ACE}		200	ns	
Output enable time	t_{OE}		80	ns	
Output hold time	t_{OH}	5		ns	
CE to output in High-Z	t_{CHZ}		70	ns	1
OE to output in High-Z	t_{OHZ}		70	ns	

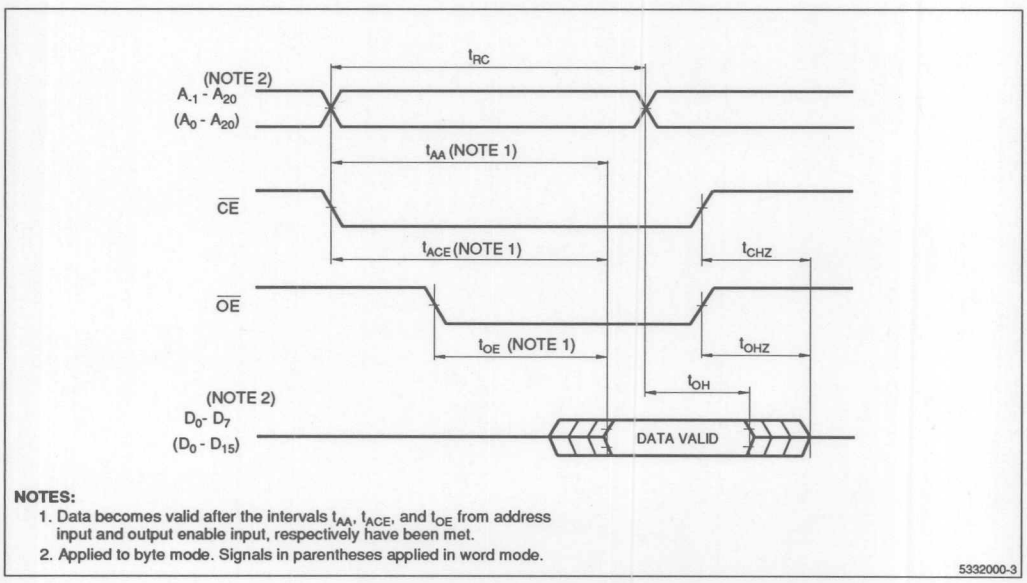
NOTE:
1. This is the time required for the outputs to become high-impedance.

AC TEST CONDITIONS

PARAMETER	RATING
Input voltage amplitude	0.6 V to 2.4 V
Input rise/fall time	10 ns
Input reference level	1.5 V
Output reference level	0.8 V and 2.2 V
Output load condition	1TTL +100 pF

CAPACITANCE (V_{CC} = 5 V ± 10%, f = 1 MHz, T_A = 25°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}			10	pF
Output capacitance	C_{OUT}			10	pF



NOTES:
1. Data becomes valid after the intervals t_{AA}, t_{ACE}, and t_{OE} from address input and output enable input, respectively have been met.
2. Applied to byte mode. Signals in parentheses applied in word mode.

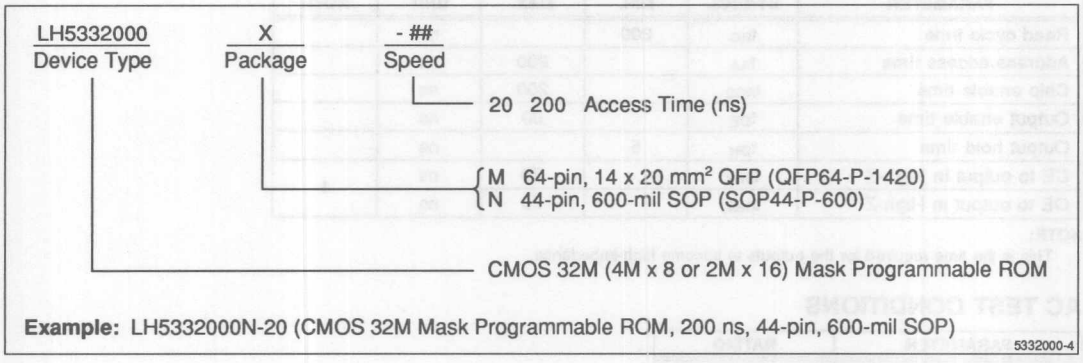
5332000-3

Figure 4. Timing Diagram

CAUTION

To stabilize the power supply, it is recommended that a high-frequency bypass capacitor be connected between the V_{CC} pin and GND.

ORDERING INFORMATION



GENERAL INFORMATION – 1

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FIFO MEMORIES – 5

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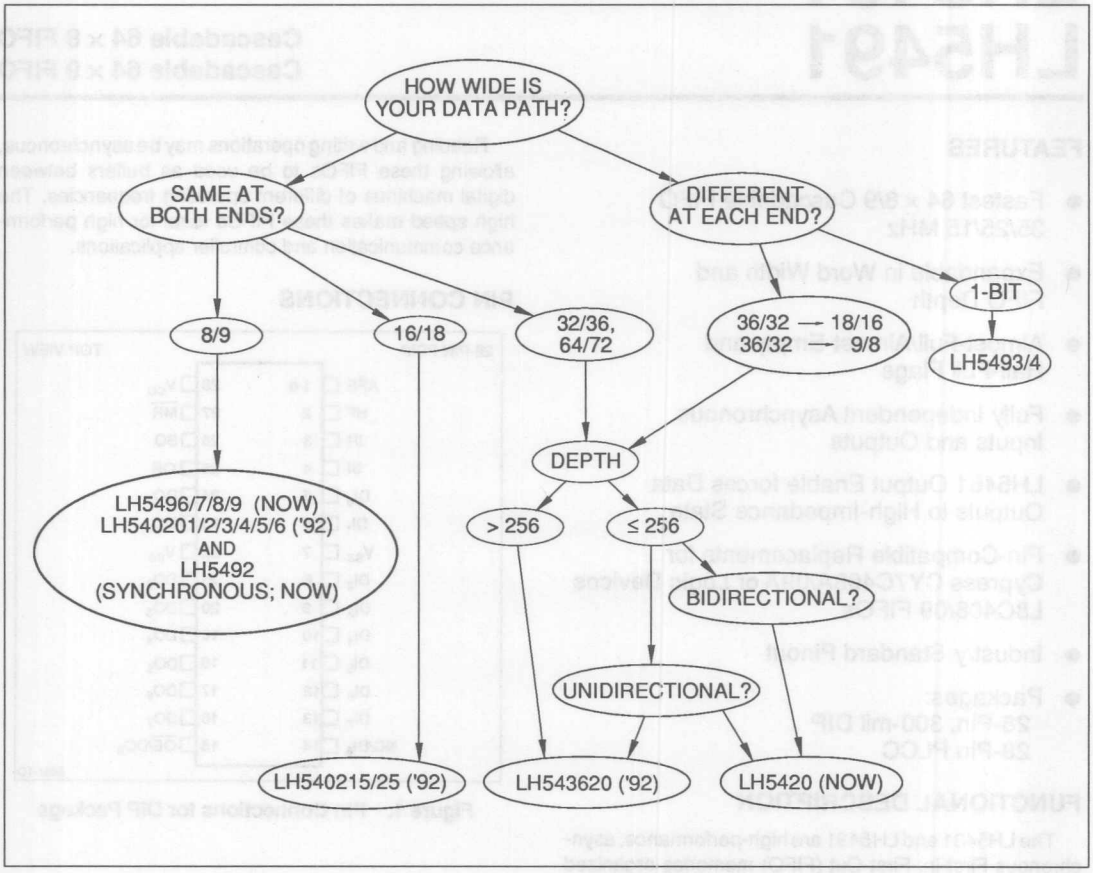
FIFO MEMORIES

	Organization	Page
LH5481/91	64 × 8/64 × 9	5-2
LH5496	512 × 9	5-16
LH5497	1K × 9	5-31
LH5498	2K × 9	5-46
LH5499	4K × 9	5-61
LH5492	4K × 9	5-76
LH5493	4K × 9	5-94
LH5494	4K × 9	5-110
LH5420	256 × 36 × 2	5-125
LH540201/02	512 × 9/1K × 9	5-160
LH540203	2K × 9	5-176
LH540204	4K × 9	5-192
LH540205	8K × 9	5-208
LH540206	16K × 9	5-224
LH540215/25	512 × 18/1K × 18	5-226
LH543620	1K × 36	5-255

THE SHARP WAY TO CHOOSE A FIFO



LH5481
LH5491

Cascadable 64 × 8 FIFO
Cascadable 64 × 9 FIFO

FEATURES

- Fastest 64 × 8/9 Cascadable FIFO 35/25/15 MHz
- Expandable in Word Width and FIFO Depth
- Almost-Full/Almost-Empty and Half-Full Flags
- Fully Independent Asynchronous Inputs and Outputs
- LH5481 Output Enable forces Data Outputs to High-Impedance State
- Pin-Compatible Replacements for Cypress CY7C408A/09A or Logic Devices L8C408/09 FIFOs
- Industry Standard Pinout
- Packages:
  28-Pin, 300-mil DIP
  28-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH5481 and LH5491 are high-performance, asynchronous First-In, First-Out (FIFO) memories organized 64 words deep by eight or nine bits wide. The eight-bit LH5481 has an Output Enable ($\overline{OE}$) function, which can be used to force the eight data outputs (DO) to a high-impedance state. The LH5491 has nine data outputs.

These FIFOs accept eight or nine-bit data at the Data Inputs (DI). A Shift In (SI) signal writes the DI data into the FIFO. A Shift Out (SO) signal shifts stored data to the Data Outputs (DO). The Output Ready (OR) signal indicates when valid data is present on the DO outputs.

If the FIFO is full and unable to accept more DI data, Input Ready (IR) will not return HIGH, and SI pulses will be ignored. If the FIFO is empty and unable to shift data to the DO outputs, OR will not return HIGH, and SO pulses will be ignored. The Almost-Full/Almost-Empty (AFE) flag is asserted (HIGH) when the FIFO is almost-full (56 words or more) or almost- empty (eight words or less). The Half-Full (HF) flag is asserted (HIGH) when the FIFO contains 32 words or more.

Reading and writing operations may be asynchronous, allowing these FIFOs to be used as buffers between digital machines of different operating frequencies. The high speed makes these FIFOs ideal for high performance communication and controller applications.

PIN CONNECTIONS

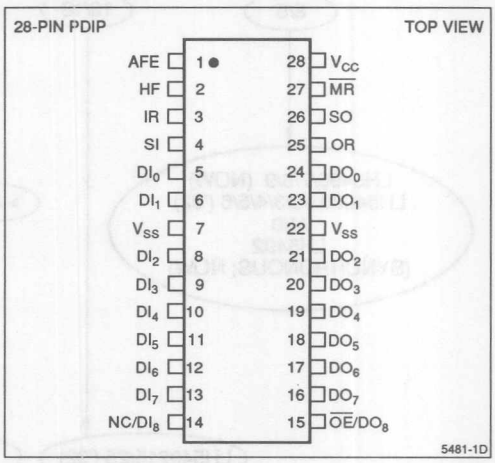


Figure 1. Pin Connections for DIP Package

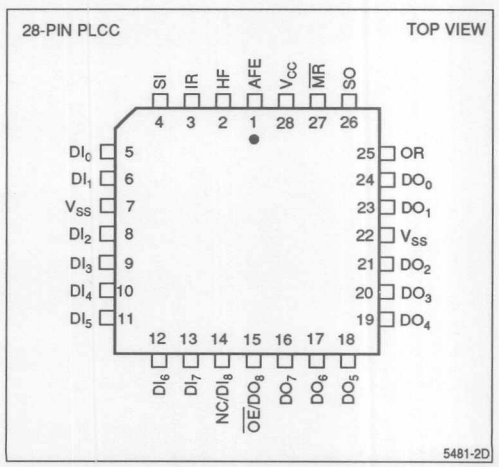


Figure 2. Pin Connections for PLCC Package

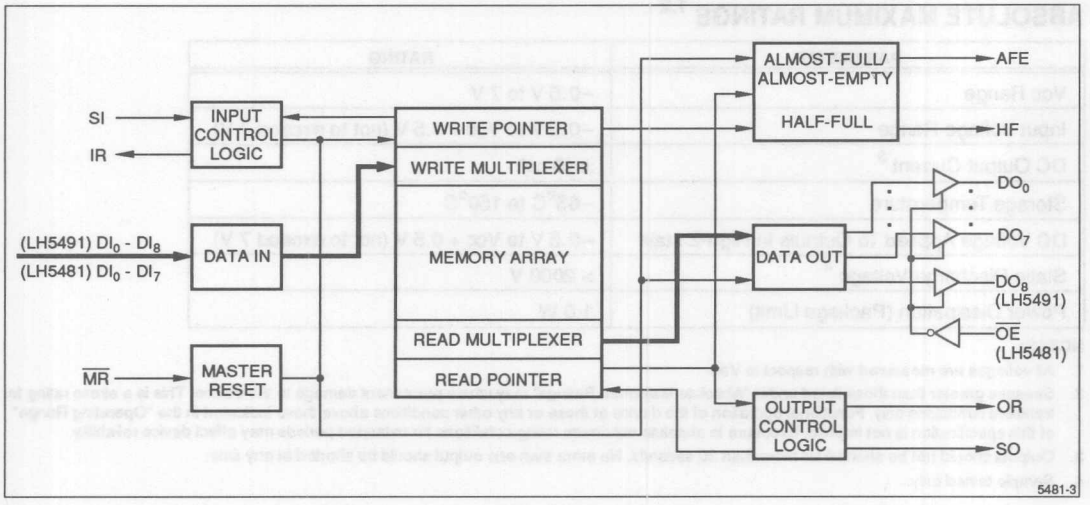


Figure 3. LH5481/91 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$DI_0 - DI_7$	I	Data Inputs, LH5481
$DO_0 - DO_7$	O/Z	Data Outputs, LH5481
$DI_0 - DI_8$	I	Data Inputs, LH5491
$DO_0 - DO_8$	O	Data Outputs, LH5491
SI	I	Shift In
SO	I	Shift Out
IR	O	Input Ready
OR	O	Output Ready

PIN	PIN TYPE *	DESCRIPTION
HF	O	Half-Full Flag
AFE	O	Almost-Full / Almost-Empty
$\overline{MR}$	I	Master Reset
$\overline{OE}$	I	Output Enable (LH5481 only)
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I=Input, O=Output, Z=High-Impedance, V=Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1,2]

PARAMETER	RATING
Vcc Range	−0.5 V to 7 V
Input Voltage Range	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 40 mA
Storage Temperature	−65°C to 150°C
DC Voltage Applied To Outputs In High-Z state	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)
Static Discharge Voltage [4]	> 2000 V
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. All voltages are measured with respect to Vss.
2. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
4. Sample tested only.

OPERATING RANGE [1]

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
T_A	Temperature, Ambient	0.0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
Vss	Ground	0.0	0.0	V
V_{IL}	Input Low Voltage (Logic "0") [2]	−0.5	0.8	V
V_{IH}	Input High Voltage (Logic "1")	2.0	Vcc + 0.5	V

NOTES:

1. All voltages are measured with respect to Vss.
2. FIFO inputs are able to withstand a −1.5 V undershoot for less than 10 ns per cycle.

DC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range Unless Otherwise Noted)

PARAMETER	DESCRIPTION	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current (High-Z)	V_{CC} = 5.5 V, V_{OUT} = 0 V to V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	V_{CC} = 4.5 V, I_{OH} = −4 mA	2.4		V
V_{OL}	Output Low Voltage	V_{CC} = 4.5 V, I_{OL} = 8.0 mA		0.4	V
I_{CCQ}	Power Supply Quiescent Current	V_{CC} = 5.5 V, I_{OUT} = 0 mA $V_{IN} \le V_{IL}$, $V_{IN} \ge V_{IH}$		25	mA
I_{CC}	Power Supply Current [2]	fsi = 35MHz, fso = 35MHz		45	mA

NOTES:

1. All voltages are measured with respect to Vss.
2. Icc is dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS [1]

PARAMETER	RATING
Input Pulse Levels	0 to 3 V
Input Rise and Fall Times (10% / 90%)	Figure 4a
Input Timing Reference Levels	1.5 V
Output Timing Reference Levels	1.5 V
Output Load for AC Timing Tests	Figure 4b

NOTE:
1. All voltages are measured with respect to Vss.

CAPACITANCE [1,2]

PARAMETER	DESCRIPTION	TEST CONDITIONS	RATING
C_{IN}	Input Capacitance	T_A = 25°C, f = 1MHz, V_{CC} = 4.5 V	5 pF
C_{OUT}	Output Capacitance	T_A = 25°C, f = 1MHz, Vcc = 4.5 V	7 pF

NOTES:
1. All voltages are measured with respect to Vss.
2. Sample tested only.

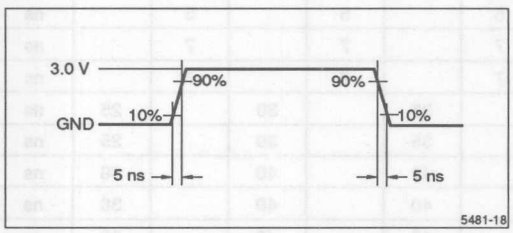


Figure 4a. Input Rise and Fall Times

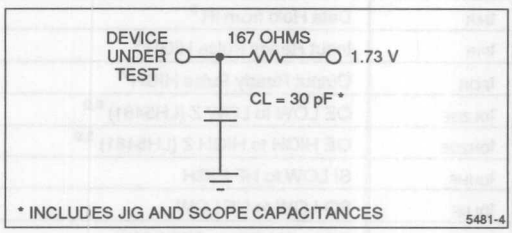


Figure 4b. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	15MHz		25MHz		35MHz		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
f_O	Operating Frequency [2]		15		25		35	MHz
t_{PHSI}	SI HIGH Time [3,8]	15		11		9		ns
t_{PLSI}	SI LOW Time [3,8]	20		18		17		ns
t_{SSI}	Data Setup to SI [4]	–1		–1		–1		ns
t_{HSI}	Data Hold from SI [4]	14		12		10		ns
t_{DLIR}	Delay, SI HIGH to IR LOW		20		18		16	ns
t_{DHIR}	Delay, SI LOW to IR HIGH		24		20		18	ns
t_{PHSO}	SO HIGH Time [3]	15		11		9		ns
t_{PLSO}	SO LOW Time [3]	20		18		17		ns
t_{DLOR}	Delay, SO HIGH to OR LOW		20		18		16	ns
t_{DHOR}	Delay, SO LOW to OR HIGH		24		20		18	ns
t_{SOR}	Data Setup to OR HIGH	–1		–1		–1		ns
t_{HSO}	Data Hold from SO LOW	0		0		0		ns
t_{FT}	Fallthrough Time		36		34		30	ns
t_{BT}	Bubblethrough Time		28		26		25	ns
t_{SIR}	Data Setup to IR [5]	5		5		5		ns
t_{HIR}	Data Hold from IR [5]	5		5		5		ns
t_{PIR}	Input Ready Pulse HIGH [8]	7		7		7		ns
t_{POR}	Output Ready Pulse HIGH [8]	7		7		7		ns
t_{DLZOE}	OE LOW to LOW Z (LH5481) [6,9]		35		30		25	ns
t_{DHZOE}	OE HIGH to HIGH Z (LH5481) [6,9]		35		30		25	ns
t_{DHHF}	SI LOW to HF HIGH		40		40		36	ns
t_{DLHF}	SO LOW to HF LOW		40		40		36	ns
t_{DLAFE}	SO or SI LOW to AFE LOW		40		40		36	ns
t_{DHAFE}	SO or SI LOW to AFE HIGH		40		40		36	ns
t_{PMR}	$\overline{MR}$ Pulse Width	35		35		35		ns
t_{DSI}	$\overline{MR}$ HIGH to SI HIGH		25		25		22	ns
t_{DOR}	$\overline{MR}$ LOW to OR LOW [7]		25		25		20	ns
t_{DIR}	$\overline{MR}$ LOW to IR HIGH [7]		25		25		20	ns
t_{LXMR}	$\overline{MR}$ LOW to Output LOW [7]		25		25		20	ns
t_{AFE}	$\overline{MR}$ LOW to AFE HIGH		30		30		30	ns
t_{HF}	$\overline{MR}$ LOW to HF LOW		30		30		30	ns
t_{OD}	SO LOW to Next Data Out Valid		26		22		20	ns

NOTES:

1. All time measurements performed at " AC Test Conditions".
2. $f_O = f_{SI} = f_{SO}$.
3. $t_{PHSI} + t_{PLSI} = t_{PHSO} + t_{PLSO} = 1/f_O$.
4. t_{SSI} and t_{HSI} apply when memory is not full.
5. t_{SIR} and t_{HIR} apply when memory is full and SI is HIGH.
6. High-Z transitions are referenced to the steady-state V_{OH} – 500 mV and V_{OL} + 500 mV levels on the output.
7. After reset goes LOW, all Data outputs will be at LOW level, IR goes HIGH and OR goes LOW.
8. Common dash number devices are guaranteed by design to function properly in a cascaded configuration.
9. Sample tested only.

OPERATIONAL DESCRIPTION

Unlike earlier versions of FIFOs, the LH5481 and LH5491 use dual-port Random-Access-Memory, write and read pointers, and special control logic. The write pointer is incremented by the falling edge of the Shift In (SI) signal, while the read pointer is incremented by the falling edge of the Shift Out (SO) signal. The Input Ready (IR) signal enables data writing to the FIFO. The Output Ready (OR) signal indicates valid read information is available on the Data Output (DO) pins.

Resetting The FIFO

The FIFO must be reset, upon power-up, using the Master Reset ($\overline{MR}$) signal. This causes the FIFO to enter an empty state, indicated by the Output Ready (OR) being LOW and Input Ready (IR) being HIGH. All Data Output (DO) pins will be LOW in this state. The AFE flag will be HIGH, and the HF flag will be LOW.

If Shift In (SI) is HIGH, when the Master Reset ($\overline{MR}$) signal is ended, then the data on the Data Input (DI) pins will be written into the FIFO, and Input Ready (IR) will return LOW until Shift In (SI) is brought LOW.

If Shift In (SI) is LOW when the Master Reset ($\overline{MR}$) is deasserted, then Input Ready (IR) goes HIGH, but the data on the Data Input (DI) pins does not enter the FIFO until Shift In (SI) goes HIGH.

Shifting Data In

Data Input (DI) is shifted into the FIFO on the rising edge of Shift In (SI). This loads input data into the FIFO, and causes Input Ready (IR) to go LOW. When a falling edge of Shift In (SI) occurs,the write pointer increments to the next word position, and Input Ready (IR) goes HIGH, indicating that the FIFO is ready to accept new data. When the FIFO is full, Input Ready (IR) remains LOW after the negative edge of Shift In (SI) signal; Shift Out (SO) action is required to unload a word of data and bring Input Ready (IR) HIGH. (See 'Bubblethrough Condition' description.)

Shifting Data Out

Data is shifted out of the FIFO on the falling edge of Shift Out (SO). The read pointer increments to the next word location; FIFO data, if present, appears on the Data Output (DO) pins; and the Output Ready (OR) signal goes HIGH. If FIFO data is not present, Output Ready (OR) stays LOW, indicating that the FIFO is empty; in this case, the last valid data read from the FIFO remains on the Data Output (DO) pins. When the FIFO is not empty, Output Ready (OR) goes LOW after the rising edge of Shift Out (SO). The previous data remains on the Data Output (DO) pins until a falling edge of Shift Out (SO).

Fallthrough Condition

When the FIFO is empty, a data word entering through the Shift In (SI) action follows one of two sequences.

If Shift Out (SO) is LOW, the data propagates to the Data Output (DO) pins; and Output Ready (OR) goes HIGH and stays HIGH until the next rising edge of Shift Out (SO).

If Shift Out (SO) is held HIGH while data is shifted into an empty FIFO as occurs in depth cascading of FIFOs, data propagates to the Data Output (DO) pins, and Output Ready (OR) pulses HIGH for a minimum time duration specified by t_{POR} and then goes back LOW again. The stored word remains on the Data Output (DO) pins. If more words are written into the FIFO, they line up behind the first word, and do not appear on the Data Output (DO) pins until Shift Out (SO) has returned LOW.

Bubblethrough Condition

When the FIFO is full, Shift Out (SO) action initiates one of the following two sequences:

If Shift In (SI) is LOW, Input Ready (IR) goes HIGH and stays HIGH until the next rising edge of Shift In (SI).

If Shift In (SI) is held HIGH while data is shifted out of a full FIFO, as occurs in depth cascading of FIFOs, Input Ready (IR) pulses HIGH for a minimum time duration specified by t_{PIR}, and then goes back LOW again. Special Data Input (DI) setup and hold times (t_{SIR} and t_{HIR}, respectively) are defined for this condition.

TIMING DIAGRAMS

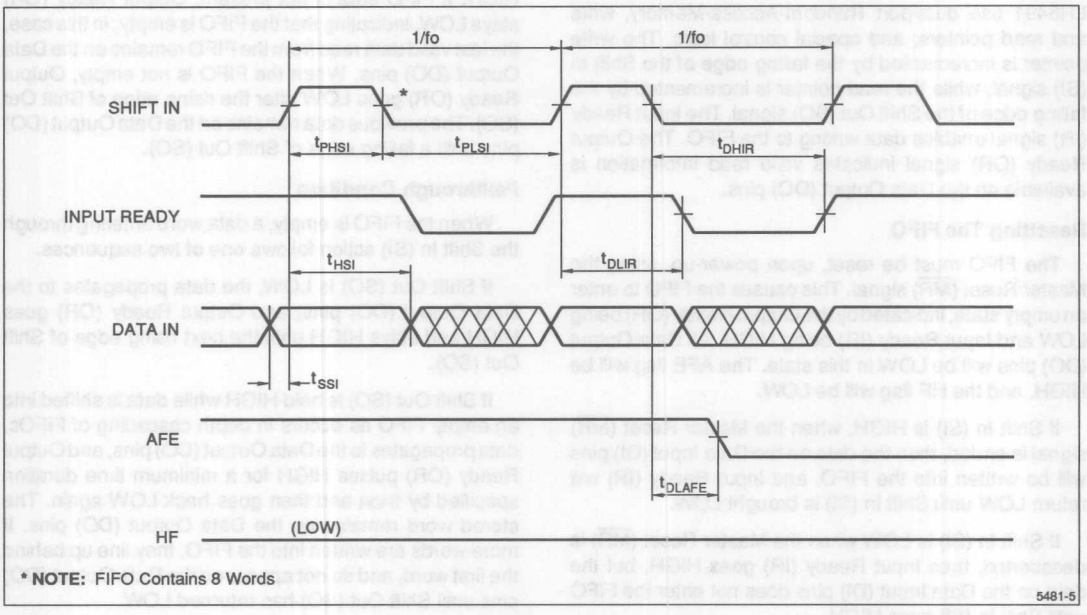


Figure 5. Data In Timing

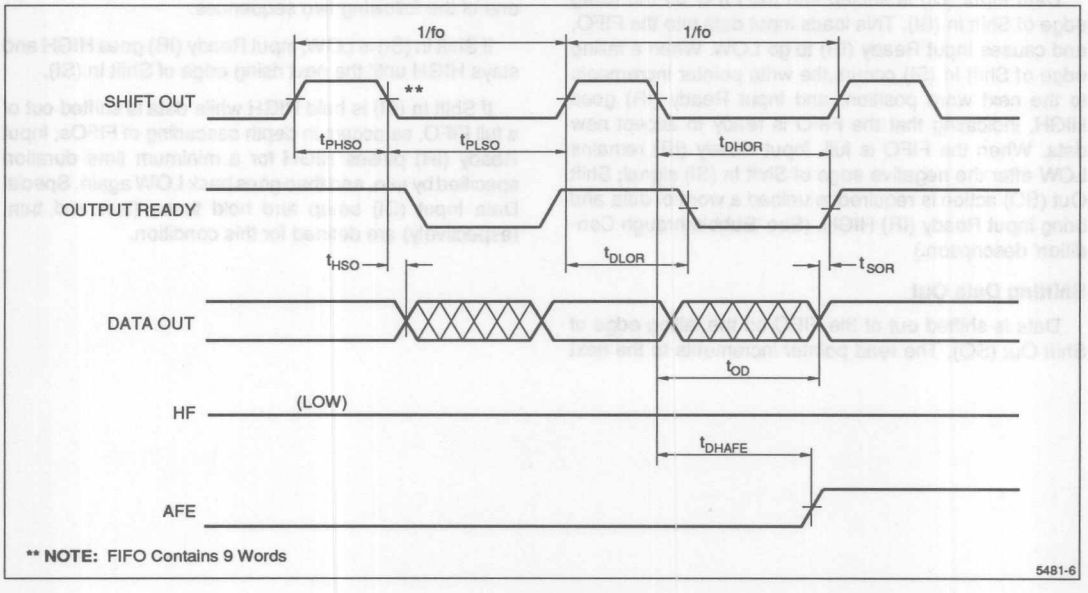


Figure 6. Data Out Timing

TIMING DIAGRAMS (cont'd)

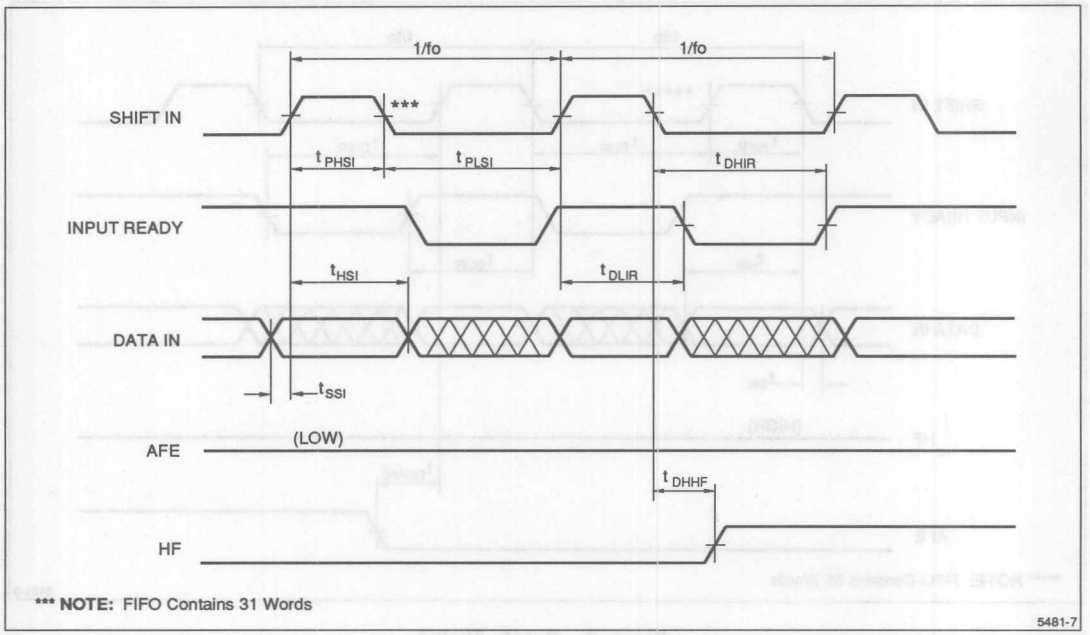


Figure 7. Data In Timing

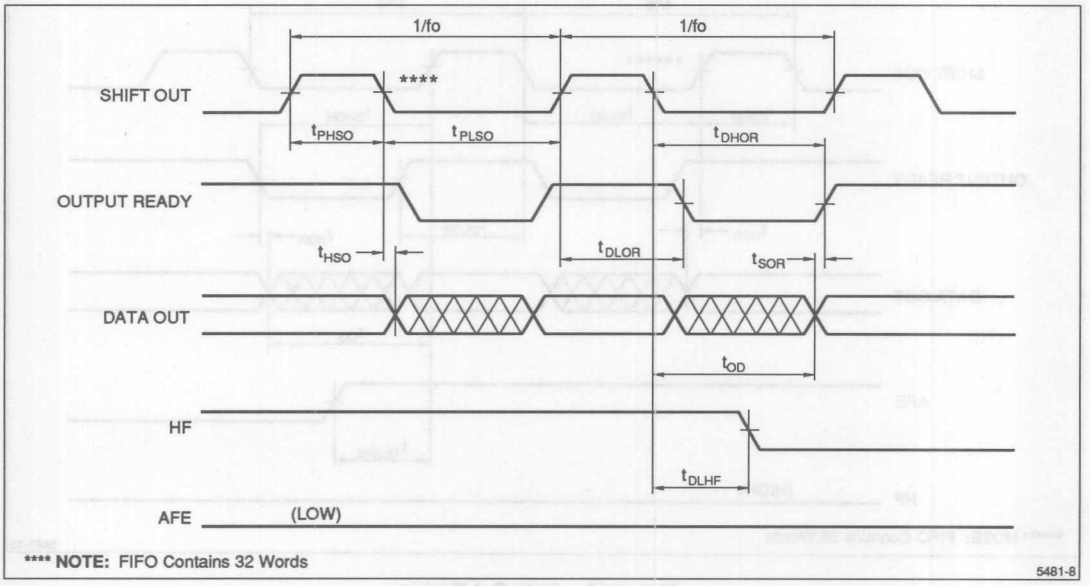


Figure 8. Data Out Timing

TIMING DIAGRAMS (cont'd)

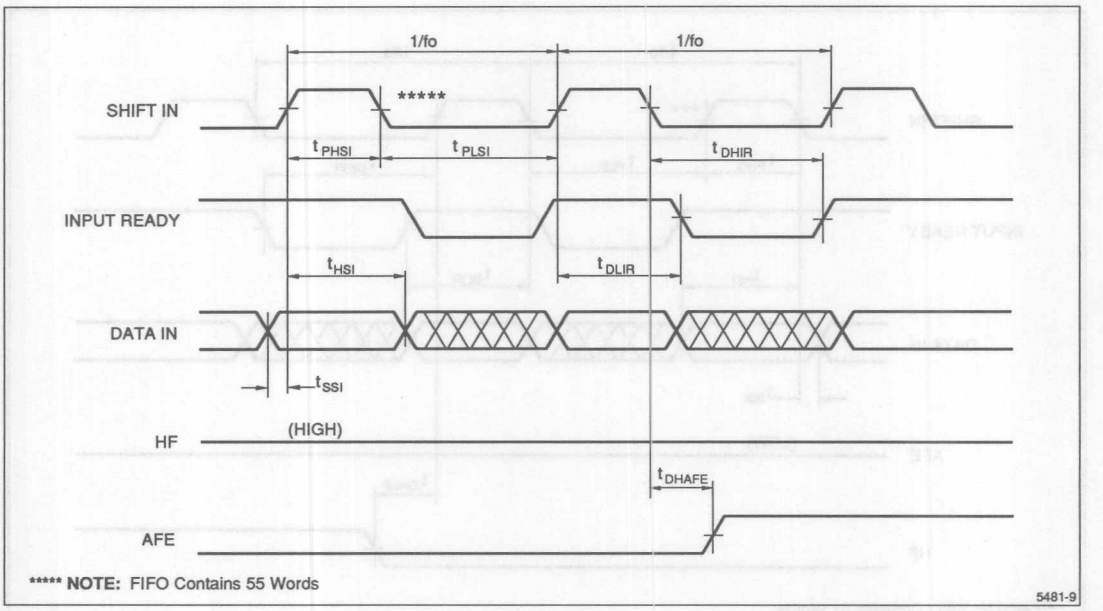


Figure 9. Data In Timing

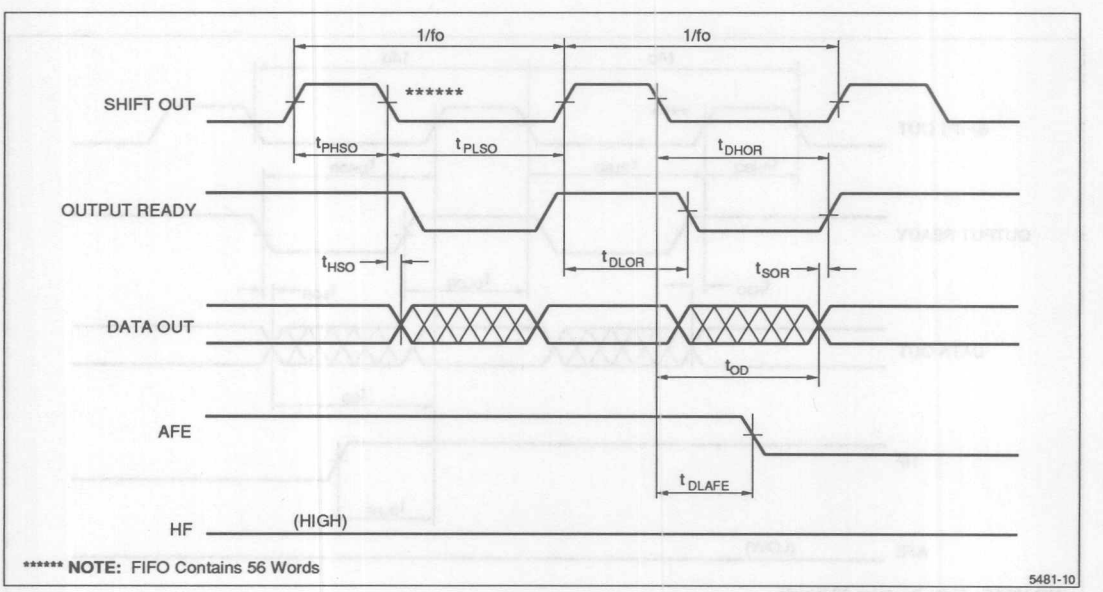


Figure 10. Data Out Timing

TIMING DIAGRAMS (cont'd)

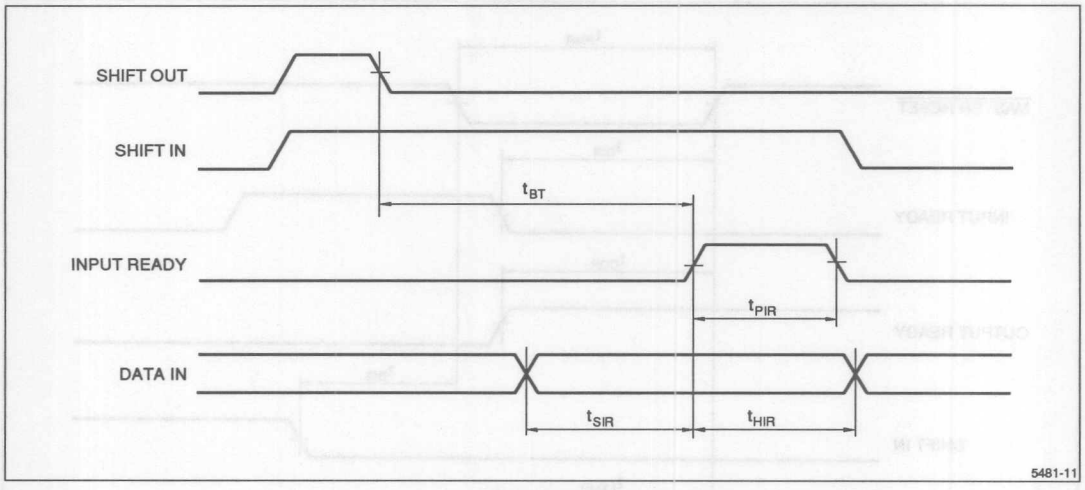


Figure 11. Bubblethrough Timing (Reading a Full FIFO)

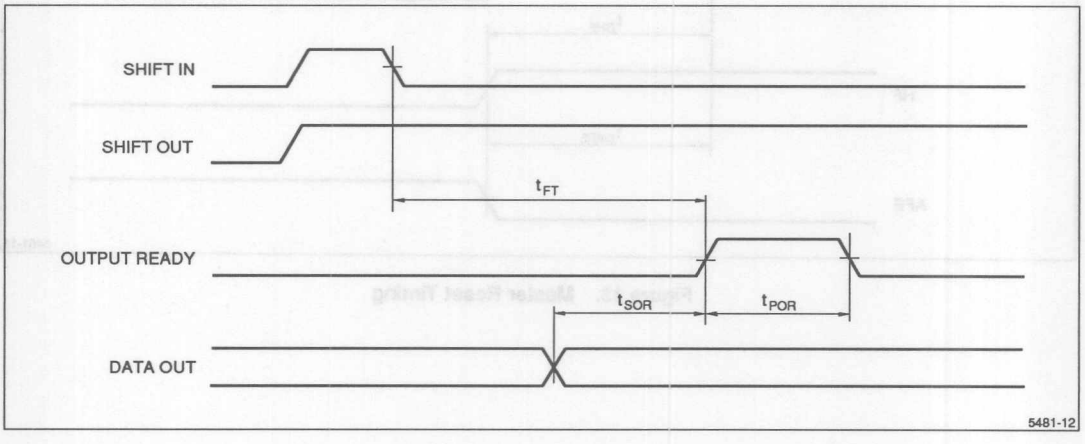


Figure 12. Fallthrough Timing (Writing an Empty FIFO)

TIMING DIAGRAMS (cont'd)

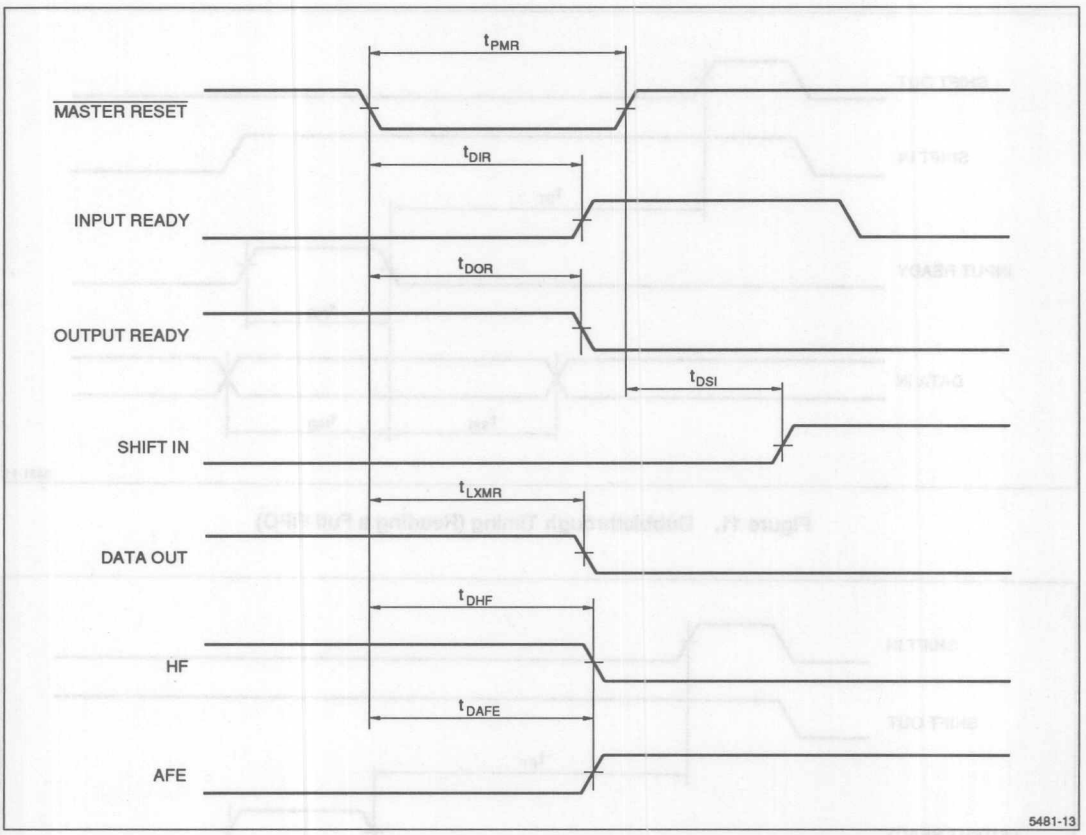


Figure 13. Master Reset Timing

TIMING DIAGRAMS (cont'd)

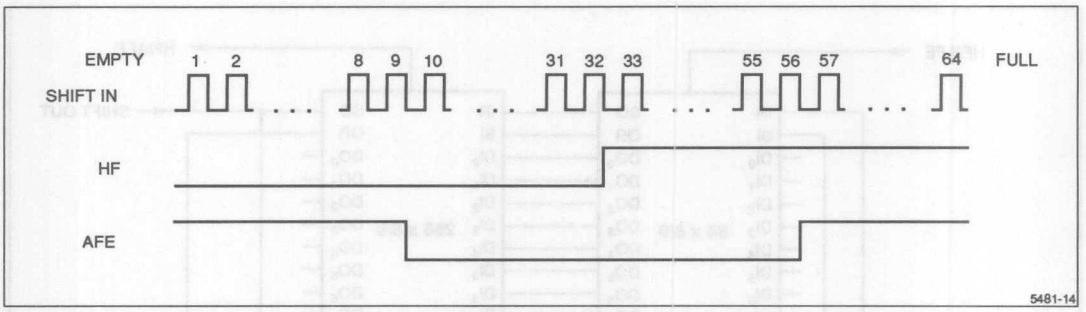


Figure 14. Shifting Words In

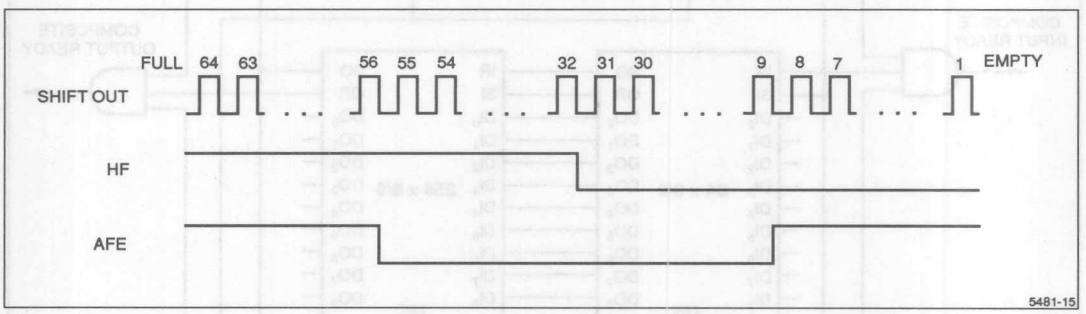


Figure 15. Shifting Words Out

FIFO EXPANSION

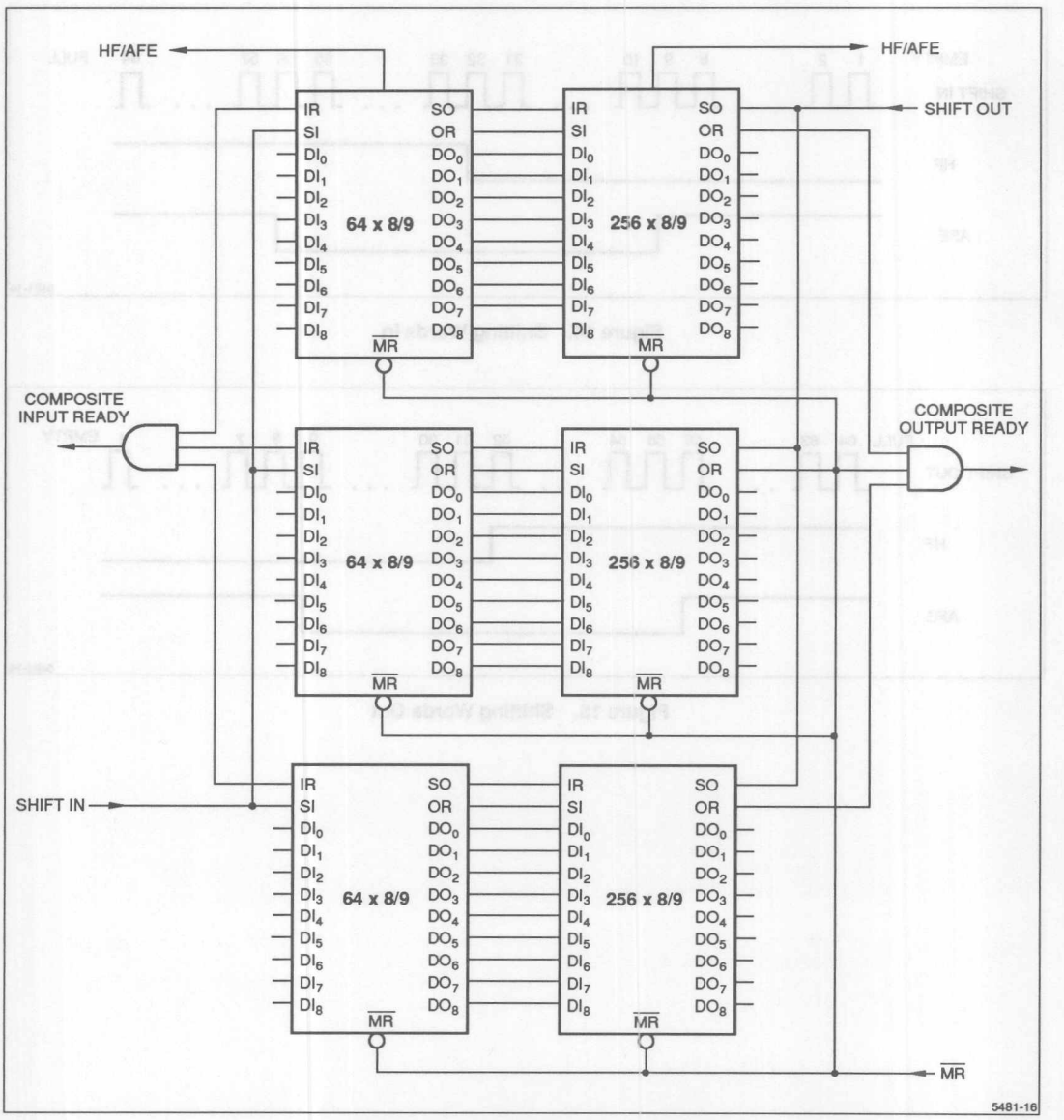


Figure 16. 320 × 24/27 Configuration Using 64 × 8/9 (LH5481/91) & 256 × 8/9 (LH5485/95) FIFOs

FIFO EXPANSION (cont'd)

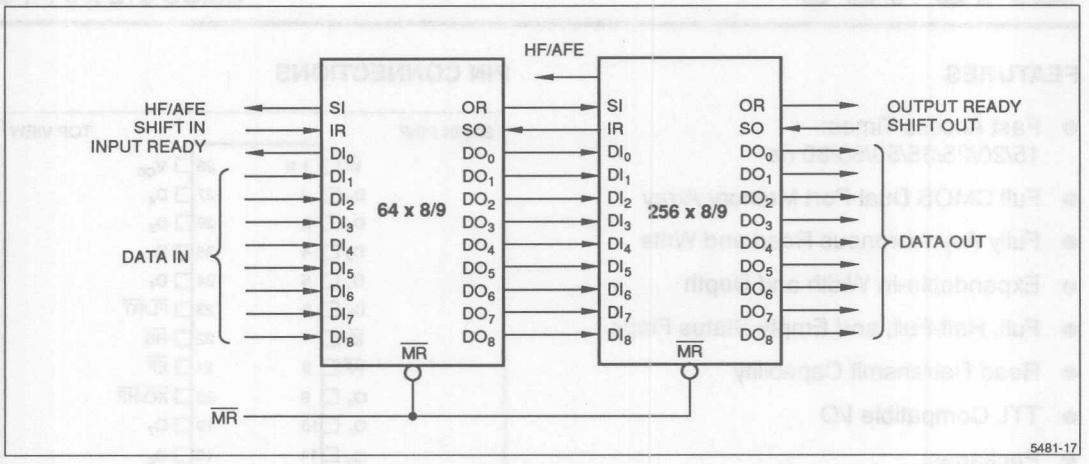


Figure 17. 128 × 8/9 Configuration

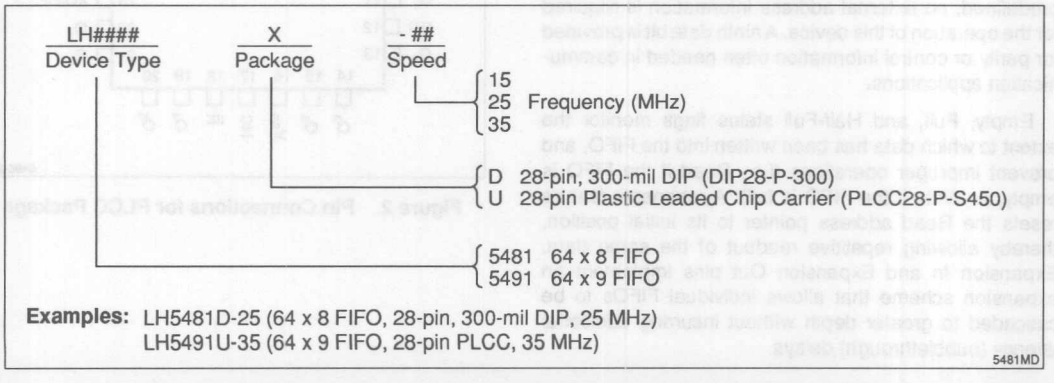
FIFOs are expandable in depth and width. However, in forming wider words, external logic is required to generate composite Input Ready and Output Ready flags. This is due to the variation of delays of the FIFOs. For example, the circuit of Figure 16 uses simple AND gates as the external IR and OR generators. More complex logic may be required if fallthrough and bubblethrough pulses are needed by the external system.

FIFOs can be easily cascaded to any desired depth, as illustrated in Figure 17. The handshaking and associated timing between the FIFOs are handled by the inherent timing of the devices.

NOTES:

1. When the memory is empty, the last word read remains on the outputs until Master Reset is strobed, or a new data word bubbles through to the output. However, OR remains LOW, indicating that the data word at the output is not valid.
2. When the output data word changes as a result of a pulse on SO, the OR signal always goes LOW before the output data word changes and stays LOW until a new data word has appeared at the outputs. Anytime OR is HIGH, there is valid stable data on the outputs.
3. All SHARP FIFOs can be cascaded with other SHARP FIFOs of the same architecture (i.e., 64 × 8/9 with 64 × 8/9). However, they may not cascade with FIFOs from other manufacturers.

ORDERING INFORMATION



LH5496

CMOS 512 × 9 FIFO

FEATURES

- Fast Access Times:
  15/20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable-in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 600-mil DIP
  32-Pin PLCC
- Pin and Functionally Compatible with IDT7201

FUNCTIONAL DESCRIPTION

The LH5496 is a dual port memory with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, it provides fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. In addition, internal logic provides for unlimited expansion in both word size and depth.

Read and write operations automatically access sequential locations in memory in that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e., Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion In and Expansion Out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

PIN CONNECTIONS

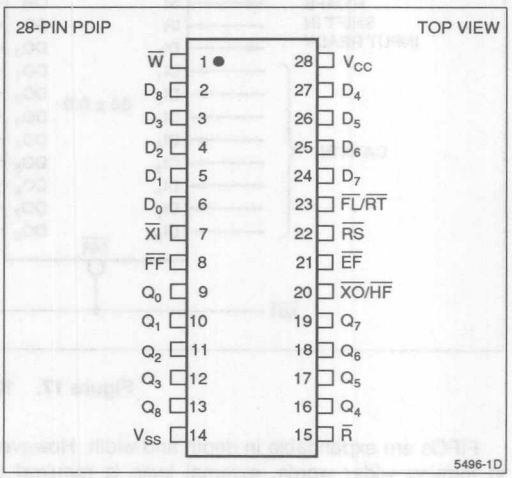


Figure 1. Pin Connections for PDIP Package

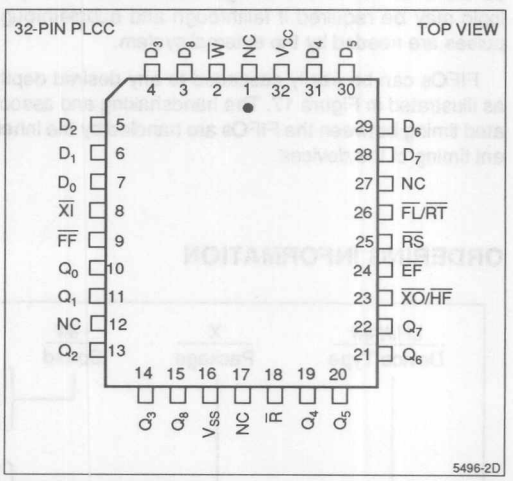


Figure 2. Pin Connections for PLCC Package

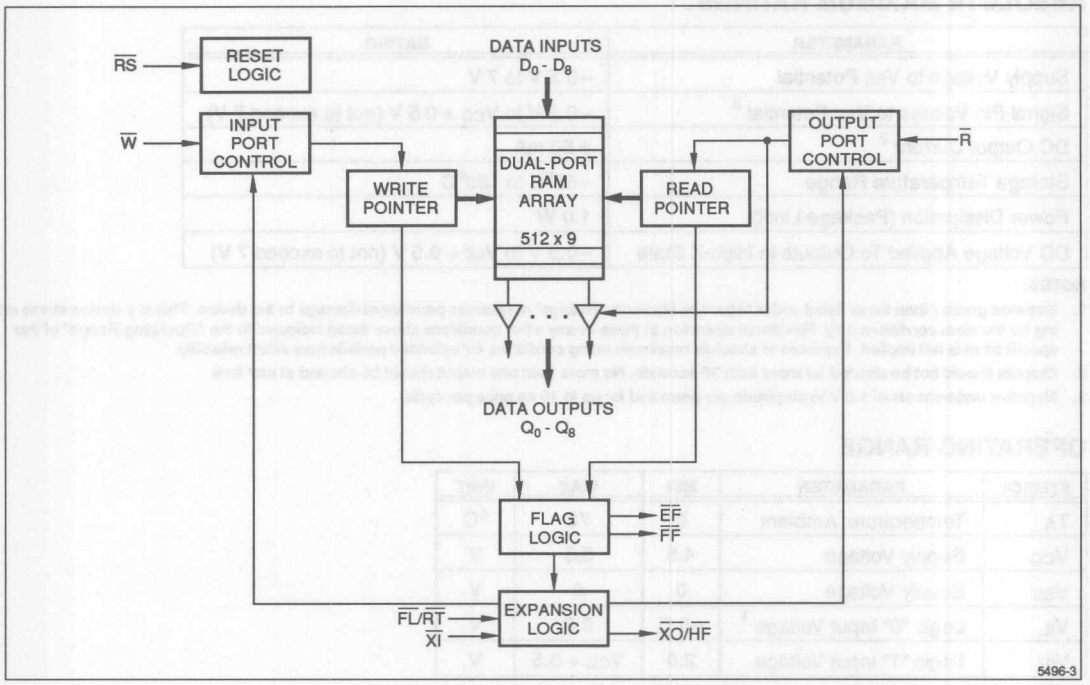


Figure 3. LH5496 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
Vcc	V	Positive Power Supply
Vss	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied To Outputs In High-Z State	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a device stress rating for transient conditions only. Functional operation at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic "1" Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2 V		5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

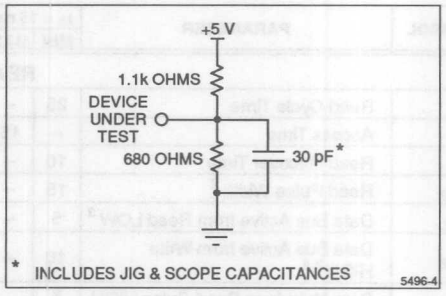


Figure 4. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
C_O MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
RETRANSMIT TIMING																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING																
t_{EFL}	Reset LOW to Empty Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out LOW	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at "AC Test Condition" levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the Reset pin ($\overline{RS}$) is taken to a LOW state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in Single mode or Depth Expansion mode. A reset pulse is required when the device is first powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a HIGH state t_{RPW} and t_{WPW} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the Write ($\overline{W}$) pin. Data setup and hold times must be observed on the data in (D_0 – D_8) pins. A write operation is only possible if the FIFO is not full, (i.e. the Full flag pin is HIGH). Writes may occur independently of any ongoing read opertations.

At the falling edge of the first write after the memory is half filled, the Half-Full flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The Half-Full flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The Full flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The Full flag will inhibit further writes until cleared by a valid read. The Full flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the Read ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The Empty flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the Read ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of t_{WEF} + t_A. Additional writes may occur while the $\overline{R}$ pin remains LOW, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the Write ($\overline{W}$) pin is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the Full flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur t_{RFF} + t_{WPW} after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be reaccessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 512 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

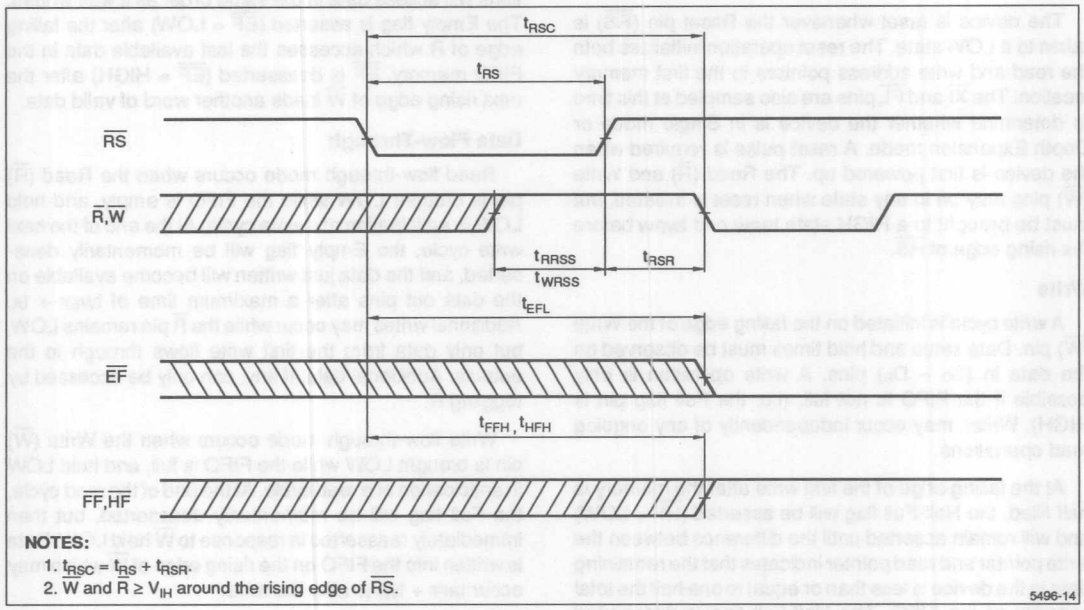


Figure 5. Reset Timing

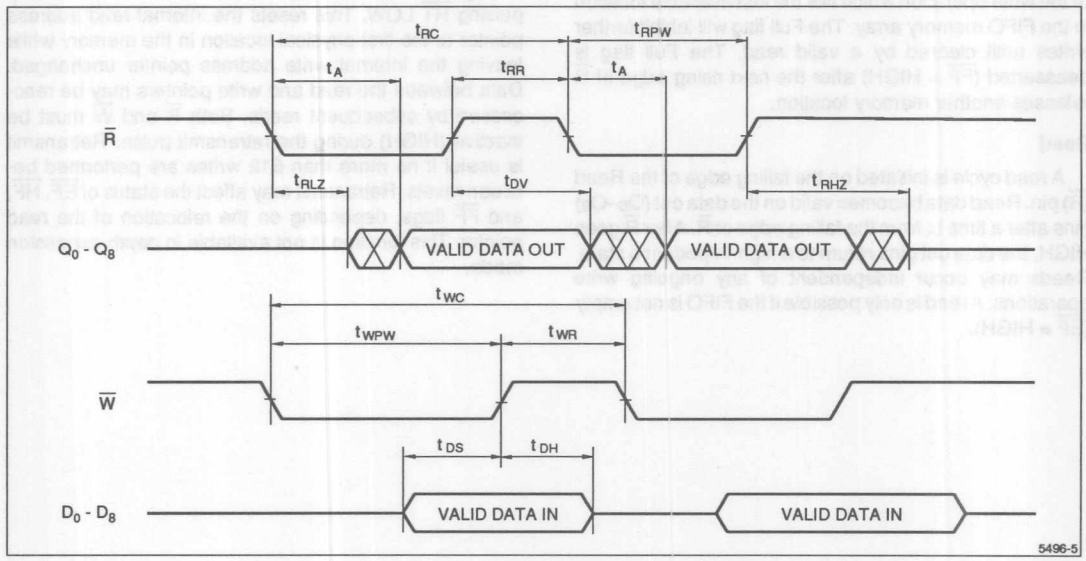


Figure 6. Asynchronous Write and Read Operation

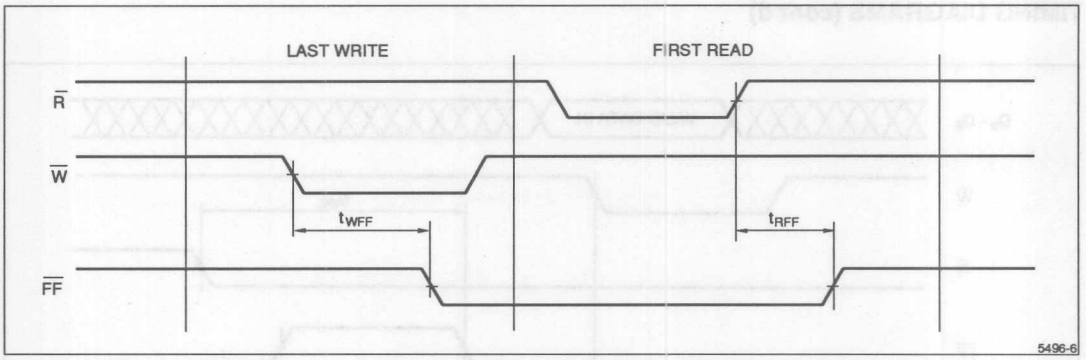


Figure 7. Full Flag from Last Write to First Read

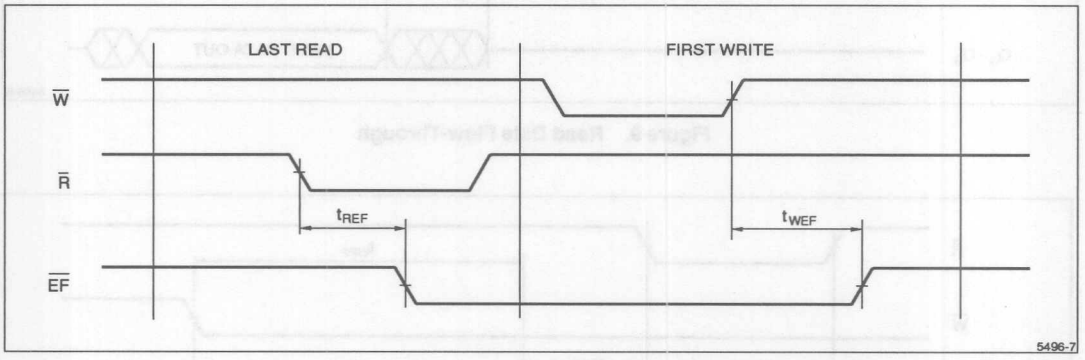


Figure 8. Empty Flag from Last Read to First Write

TIMING DIAGRAMS (cont'd)

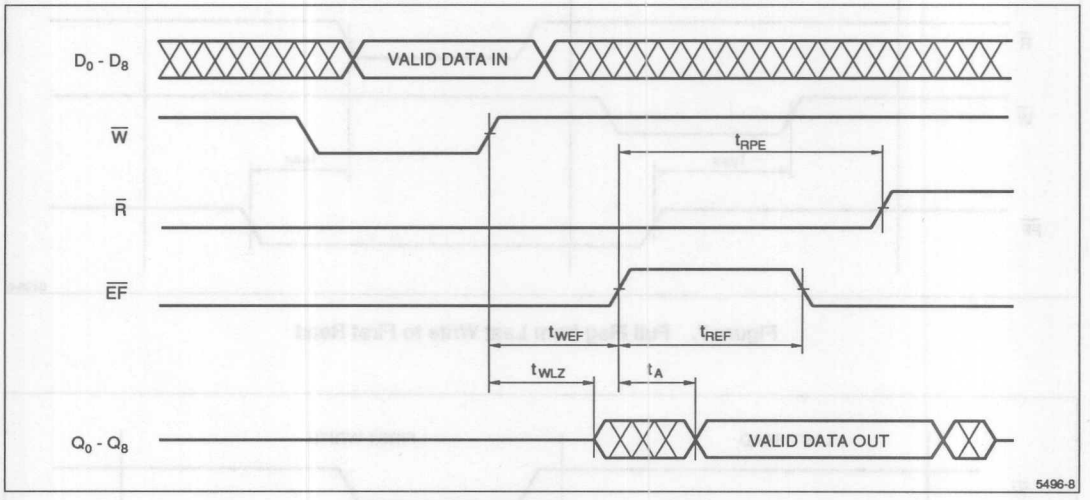


Figure 9. Read Data Flow-Through

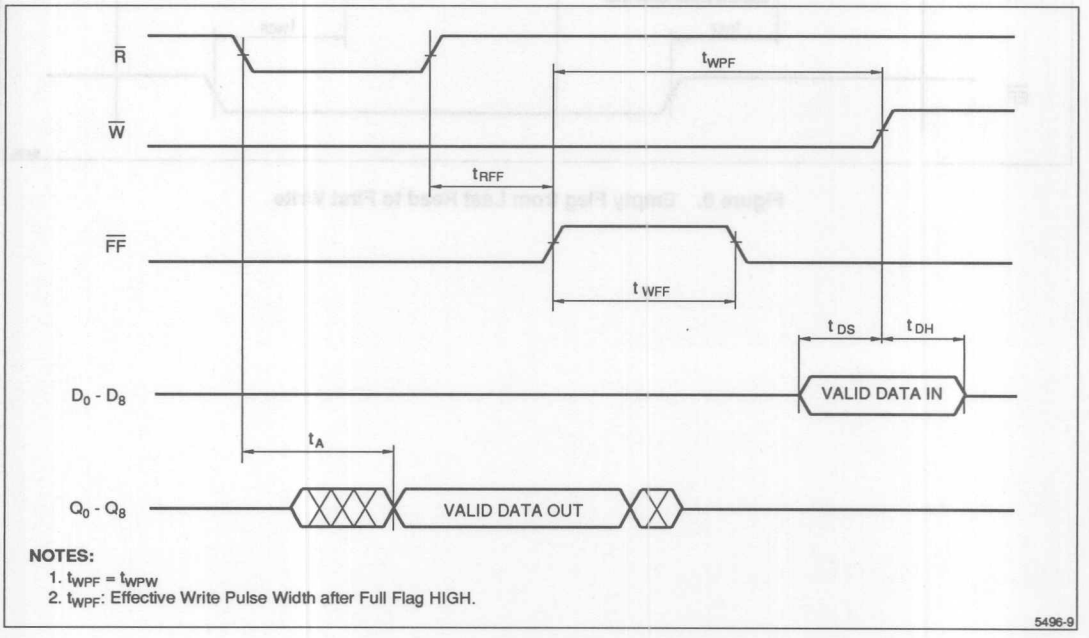


Figure 10. Write Data Flow-Through

TIMING DIAGRAMS (cont'd)

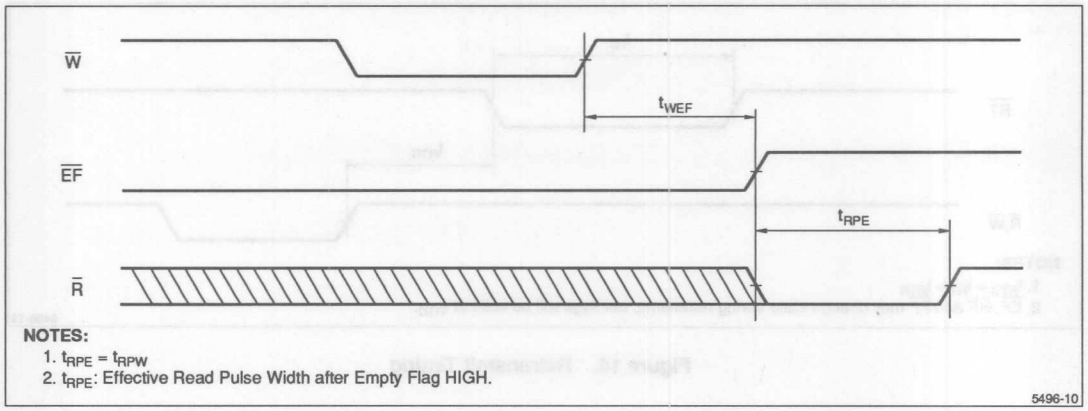


Figure 11. Empty Flag Timing

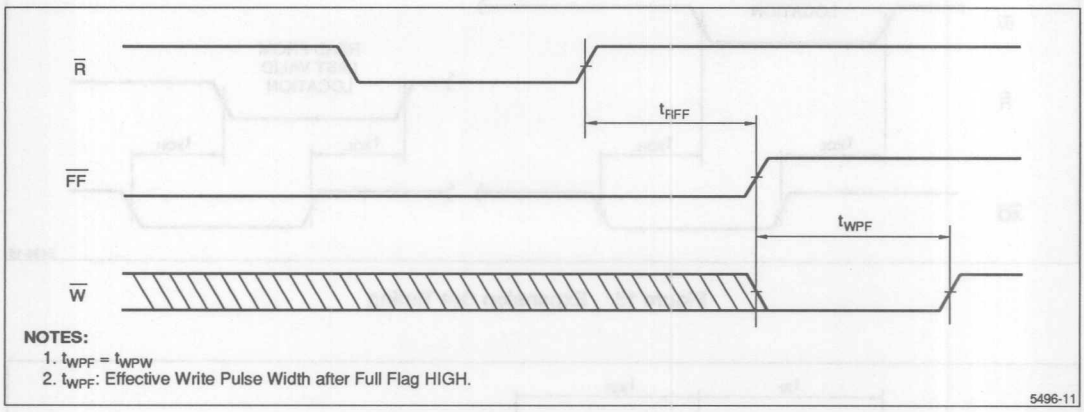


Figure 12. Full Flag Timing

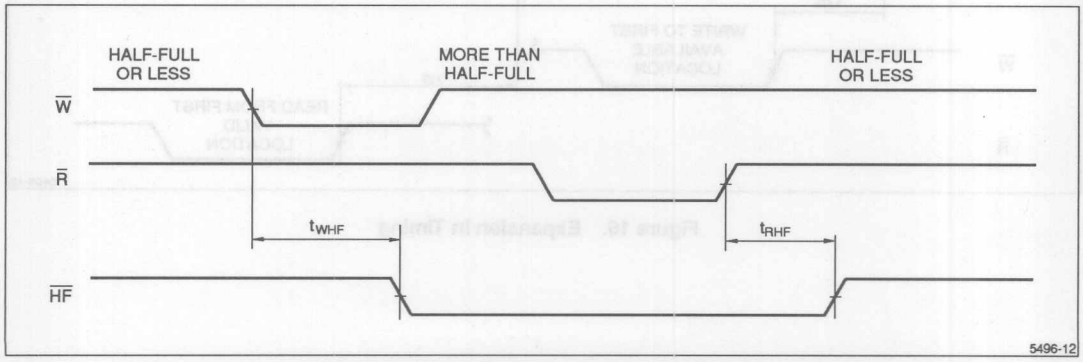


Figure 13. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)

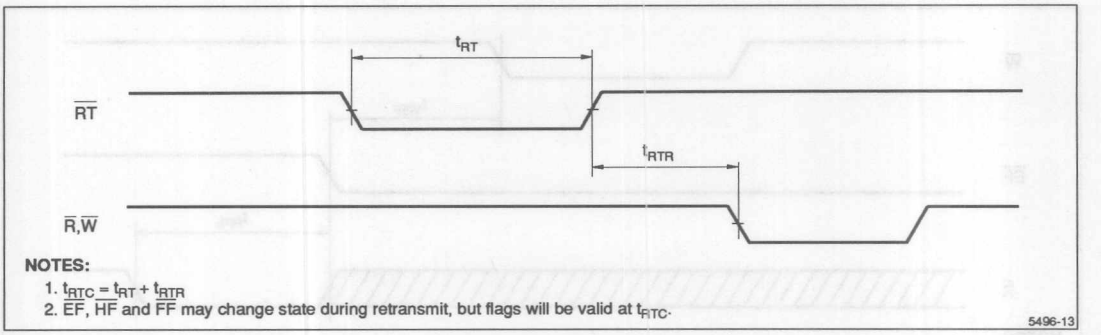


Figure 14. Retransmit Timing

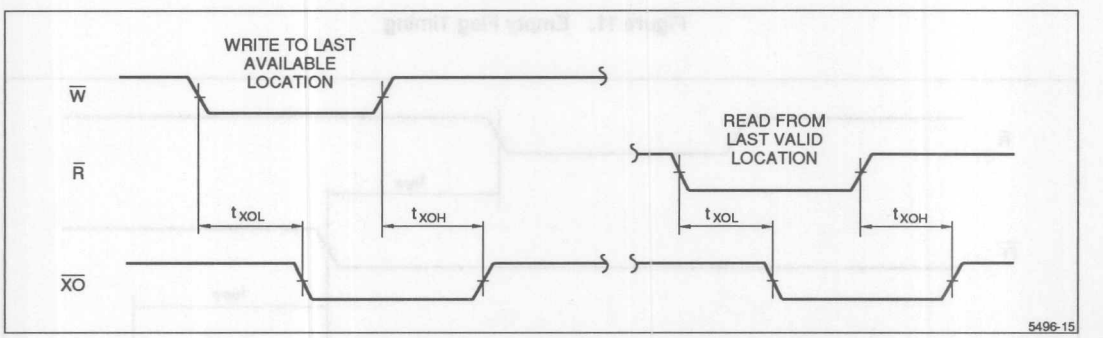


Figure 15. Expansion Out Timing

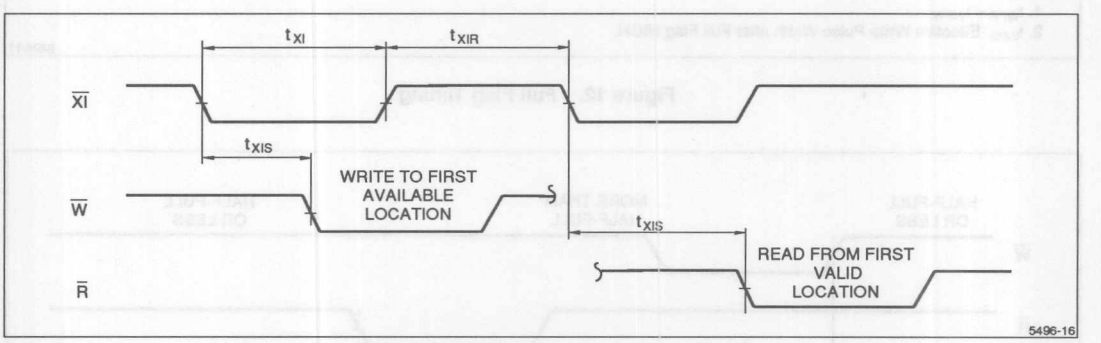


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in Single mode by tying the Expansion In pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word-width expansion is implemented by placing multiple LH5496 devices in parallel. Each LH5496 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 17 and 18.)

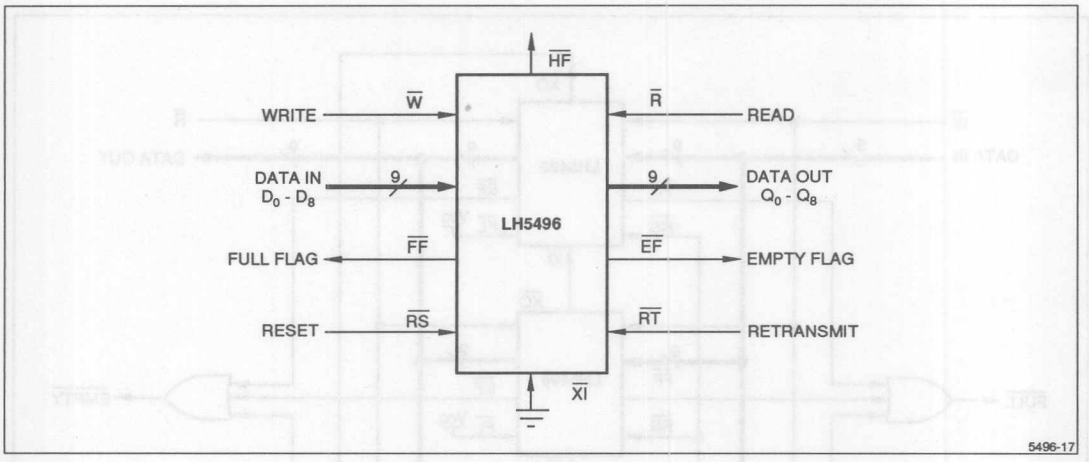


Figure 17. Single FIFO (512 × 9)

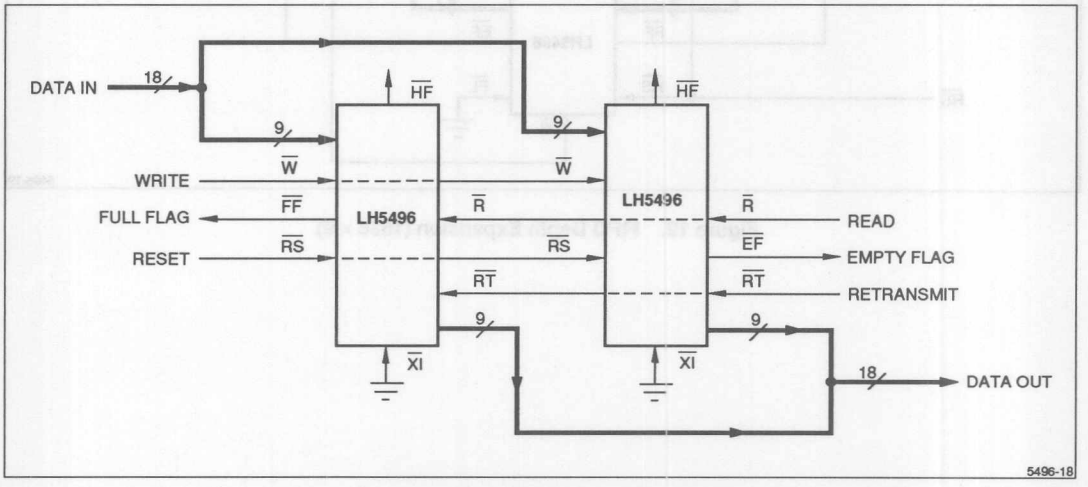


Figure 18. FIFO Width Expansion (512 × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in Expansion mode. In this arrangement, the FIFOs are connected in a circular fashion with the Expansion Out pin ($\overline{XO}$) of each device tied to the Expansion In pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the First Load pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In Expansion mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The Half-Full flag and Retransmit functions are not available in Depth Expansion mode.

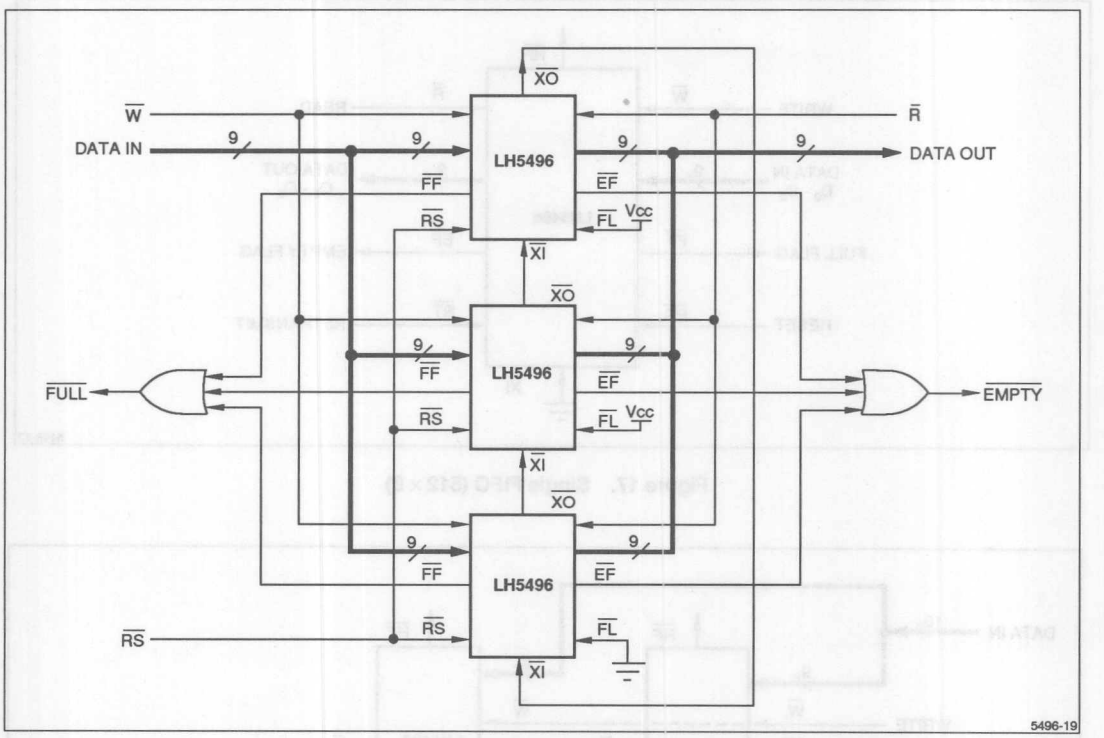


Figure 19. FIFO Depth Expansion (1536 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5496 devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

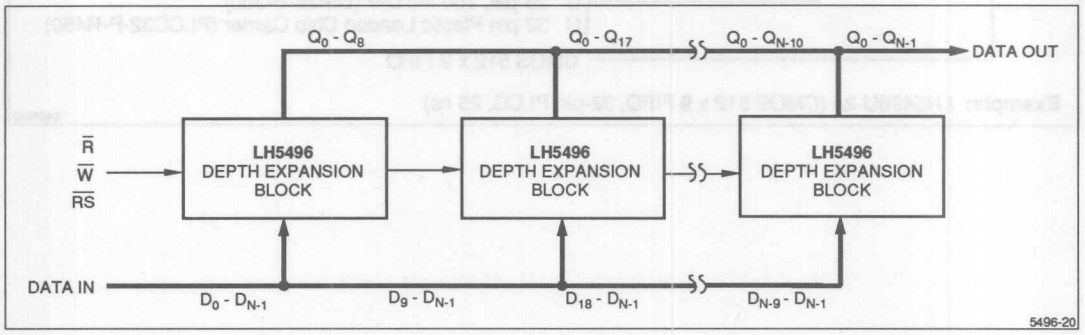


Figure 20. Compound FIFO Expansion

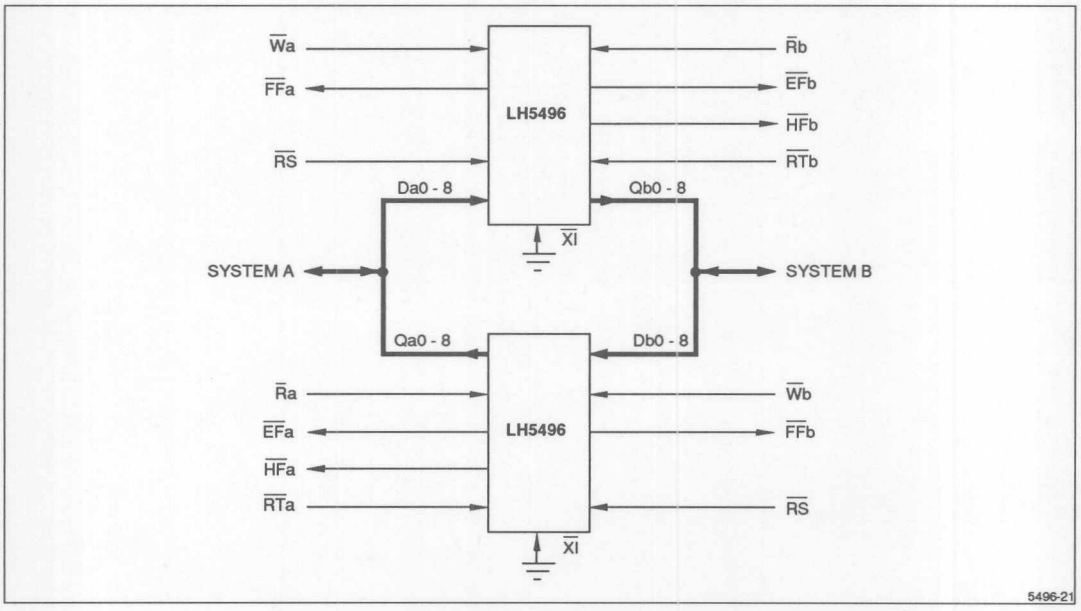
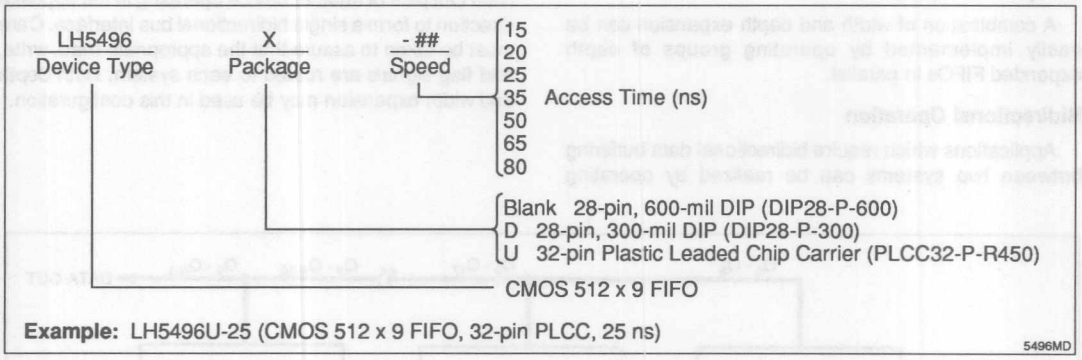


Figure 21. Bidirectional FIFO Buffer

ORDERING INFORMATION



Example: LH5496U-25 (CMOS 512 x 9 FIFO, 32-pin PLCC, 25 ns)

LH5497

CMOS 1K × 9 FIFO

FEATURES

- Fast Access Times:
  15/20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 600-mil DIP
  32-Pin PLCC
- Pin and Functionally Compatible with IDT7202

FUNCTIONAL DESCRIPTION

The LH5497 is a dual port memory with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, it provides fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. In addition, internal logic is provided for unlimited expansion in both word size and depth.

Read and Write operations automatically access sequential locations in memory in such a way that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e. Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion In and Expansion Out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

PIN CONNECTIONS

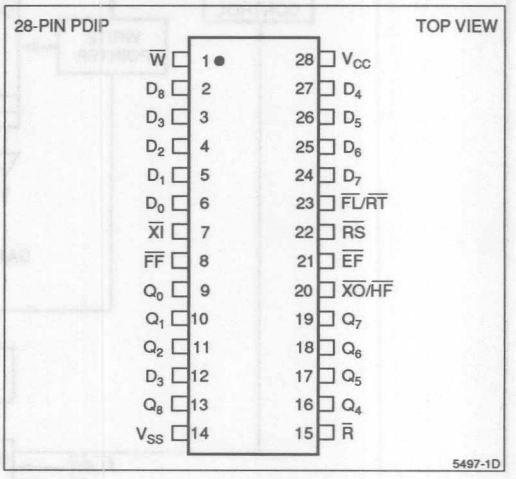


Figure 1. Pin Connections for DIP Package

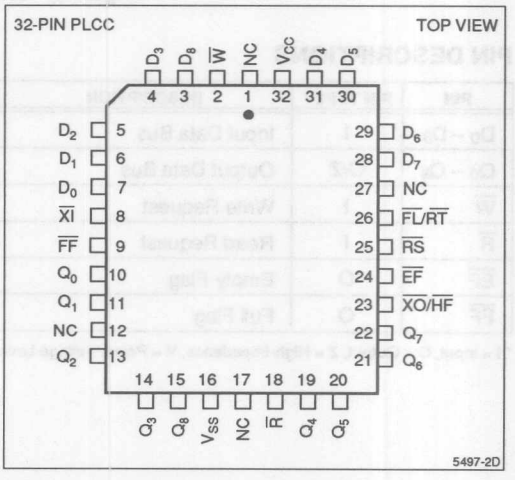


Figure 2. Pin Connections for PLCC Package

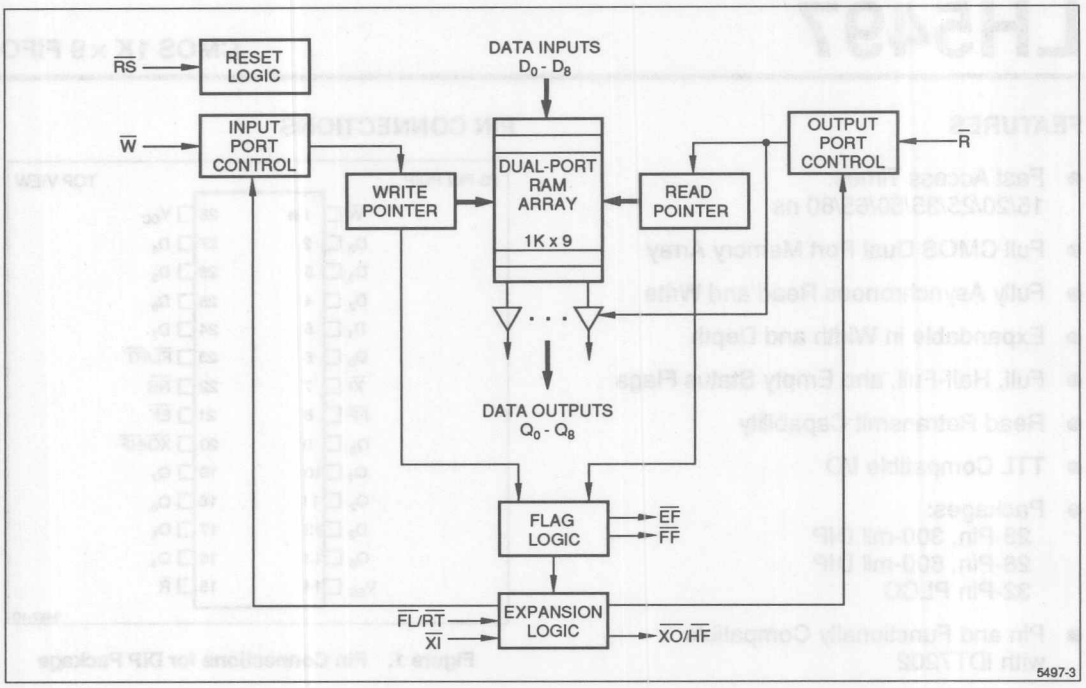


Figure 3. LH5497 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs in High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic "0" Input Voltage[1]	−0.5	0.8	V
V_{IH}	Logic "1" Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4	—	V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA	—	0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40MHz	—	100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}	—	15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V	—	5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

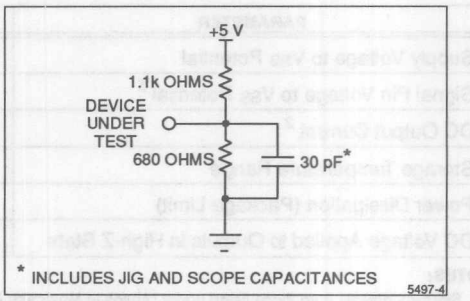


Figure 4. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
RETRANSMIT TIMING																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING																
t_{EFL}	Reset LOW to Empty Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out LOW	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at "AC Test Condition" levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the Reset pin ($\overline{RS}$) is taken to a LOW state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in Single mode or Depth Expansion mode. A reset pulse is required when the device is first powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a HIGH state t_{RPW} and t_{WPW} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the Write ($\overline{W}$) pin. Data setup and hold times must be observed on the data in ($D_0 - D_8$) pins. A write operation is only possible if the FIFO is not full, (i.e. the Full flag pin is HIGH). Writes may occur independently of any ongoing read operations.

At the falling edge of the first write after the memory is half filled, the Half-Full flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The Half-Full flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The Full flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The Full flag will inhibit further writes until cleared by a valid read. The Full flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the Read ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The Empty flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the Read ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains LOW, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the Write ($\overline{W}$) pin is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the Full flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be reaccessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 1024 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

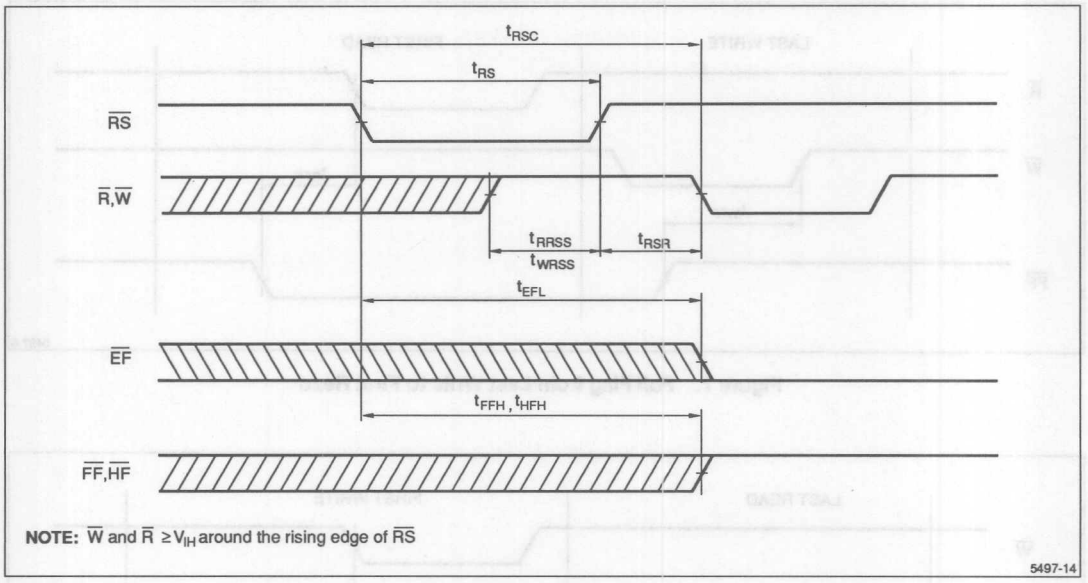


Figure 5. Reset Timing

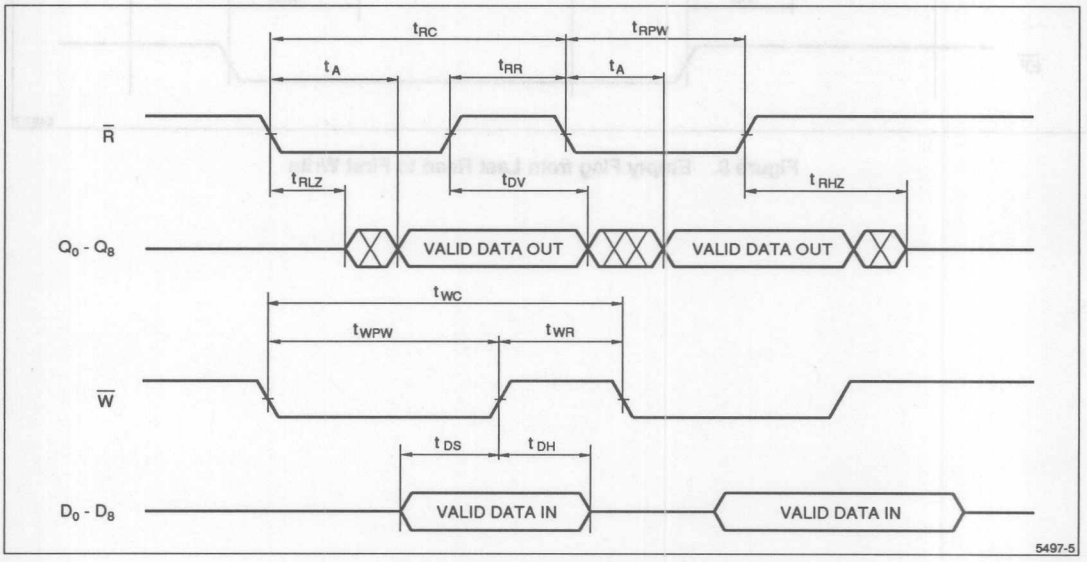


Figure 6. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

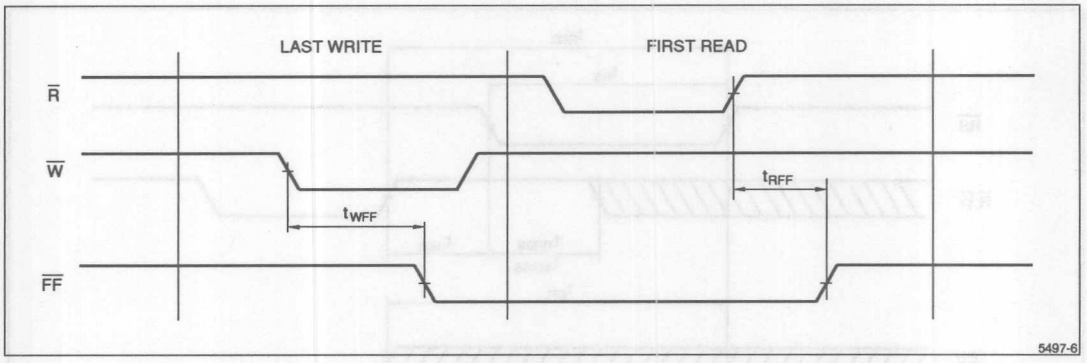


Figure 7. Full Flag from Last Write to First Read

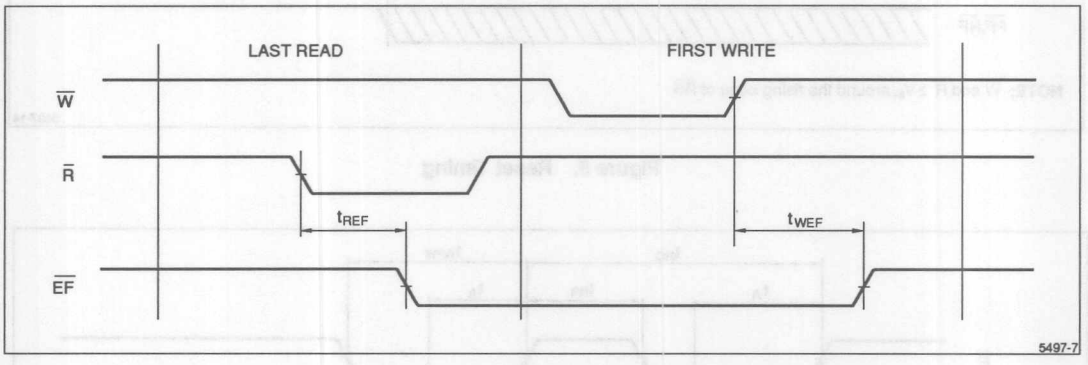


Figure 8. Empty Flag from Last Read to First Write

TIMING DIAGRAMS (cont'd)

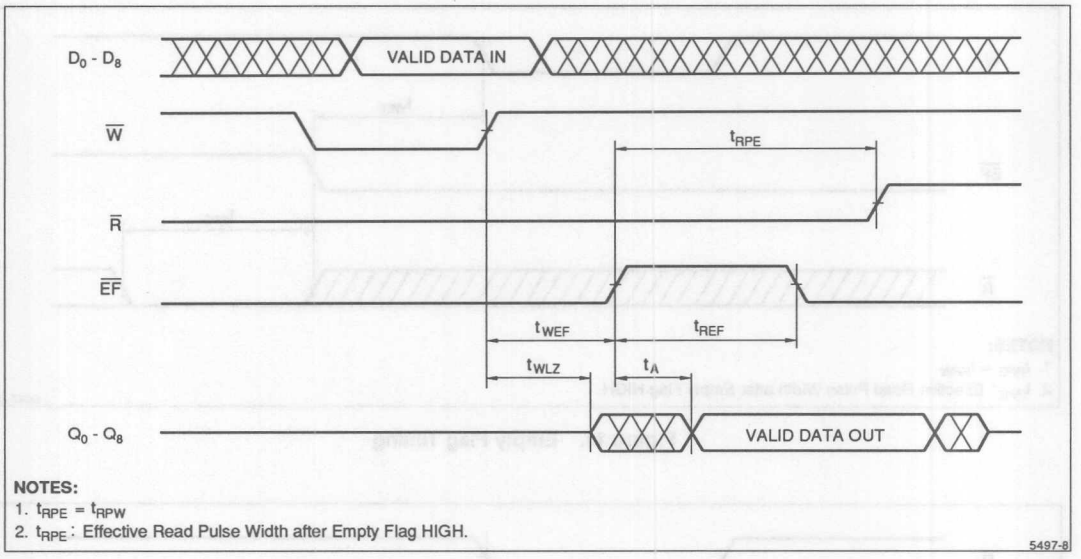


Figure 9. Read Data Flow-Through

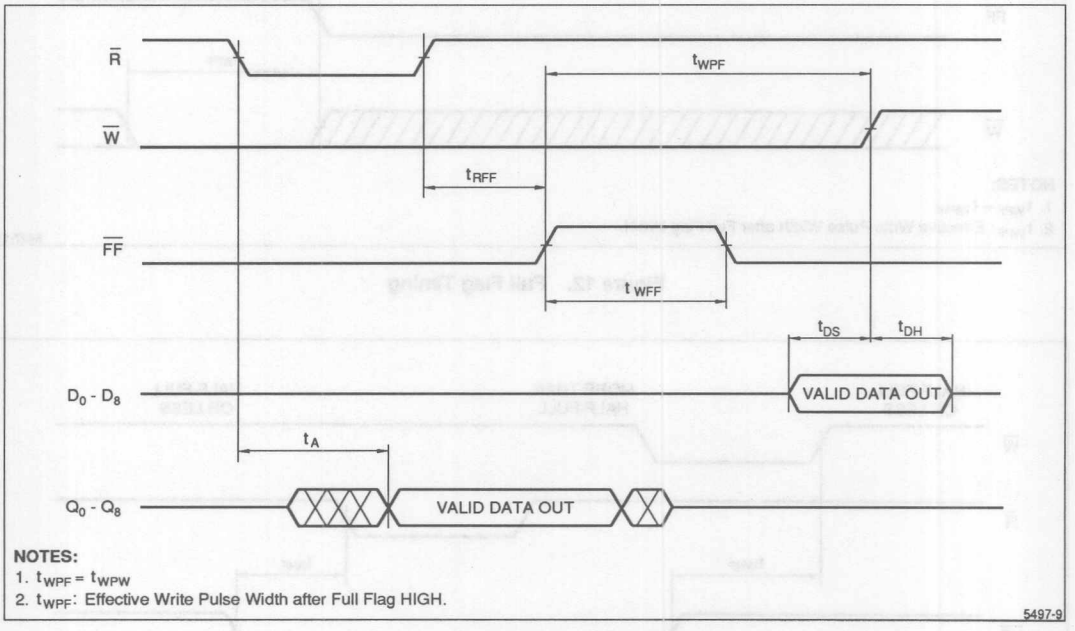


Figure 10. Write Data Flow-Through

TIMING DIAGRAMS (cont'd)

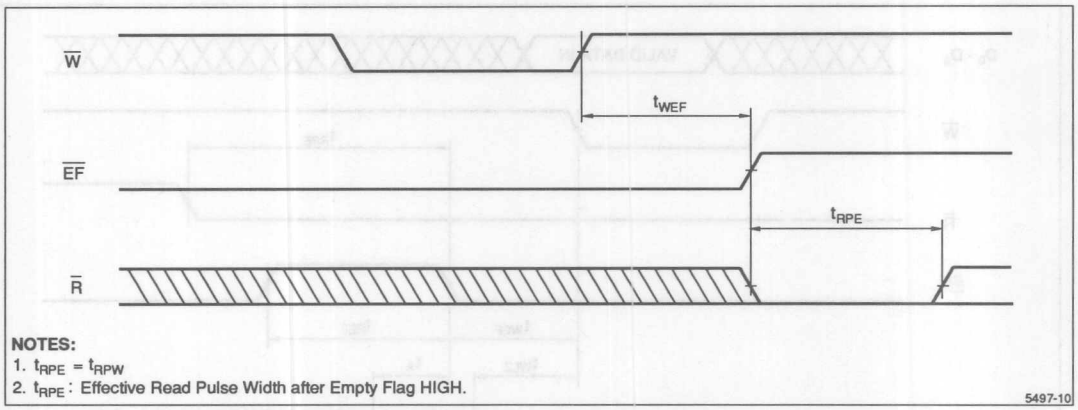


Figure 11. Empty Flag Timing

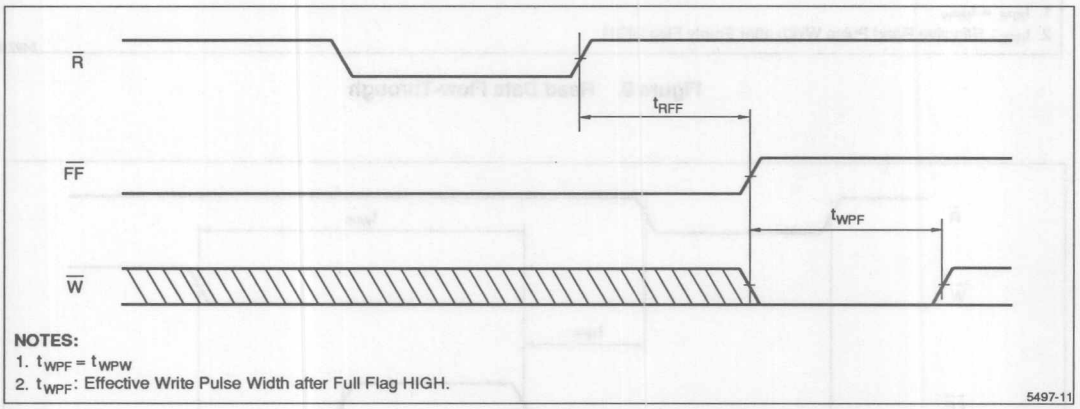


Figure 12. Full Flag Timing

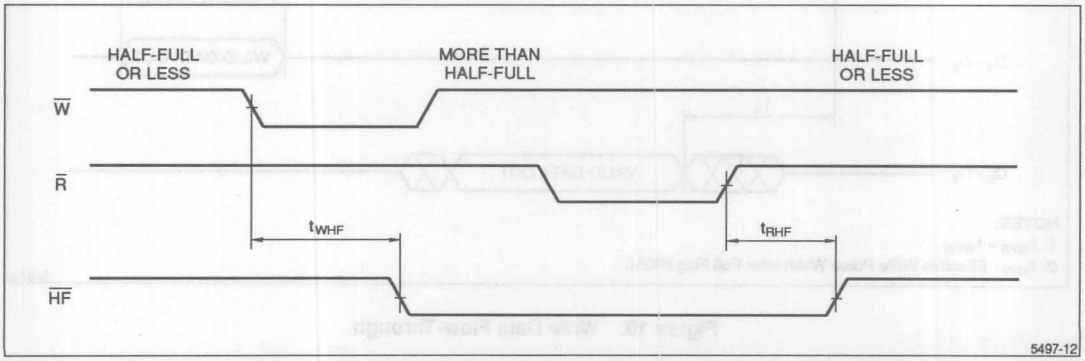


Figure 13. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)

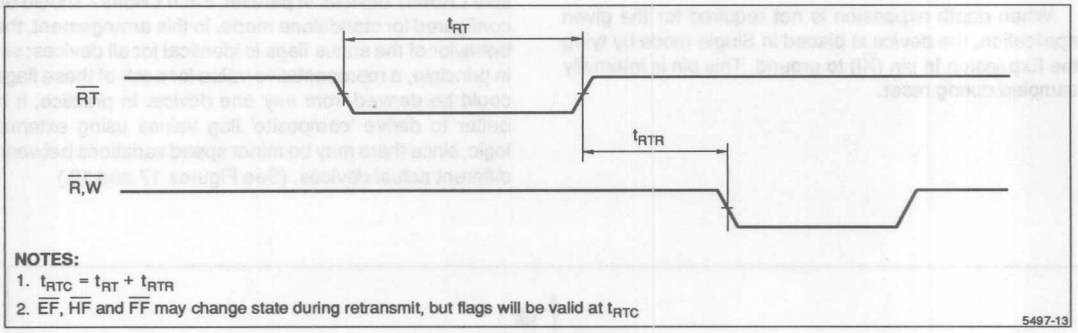


Figure 14. Retransmit Timing

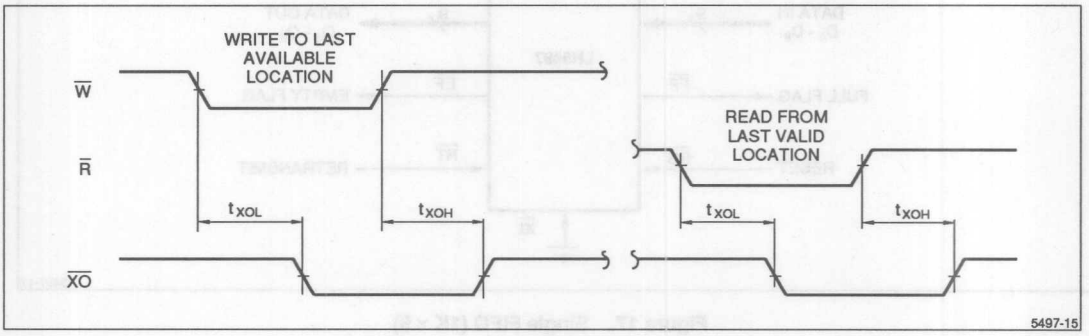


Figure 15. Expansion Out Timing

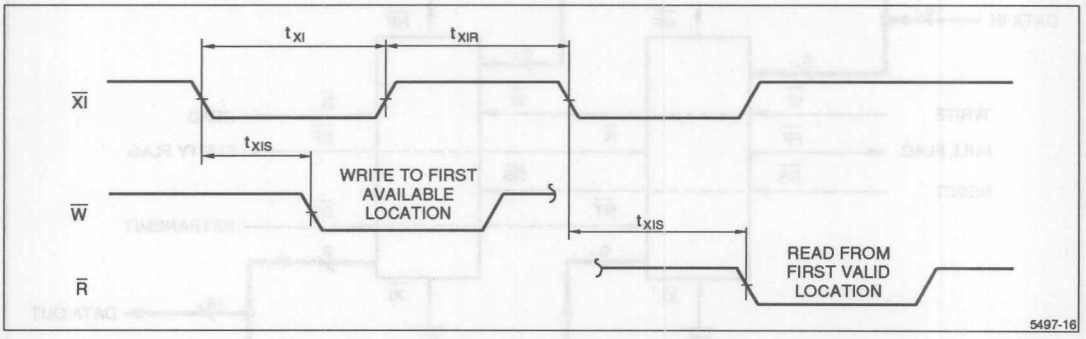


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in Single mode by tying the Expansion In pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word-width expansion is implemented by placing multiple LH5497 devices in parallel. Each LH5497 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 17 and 18.)

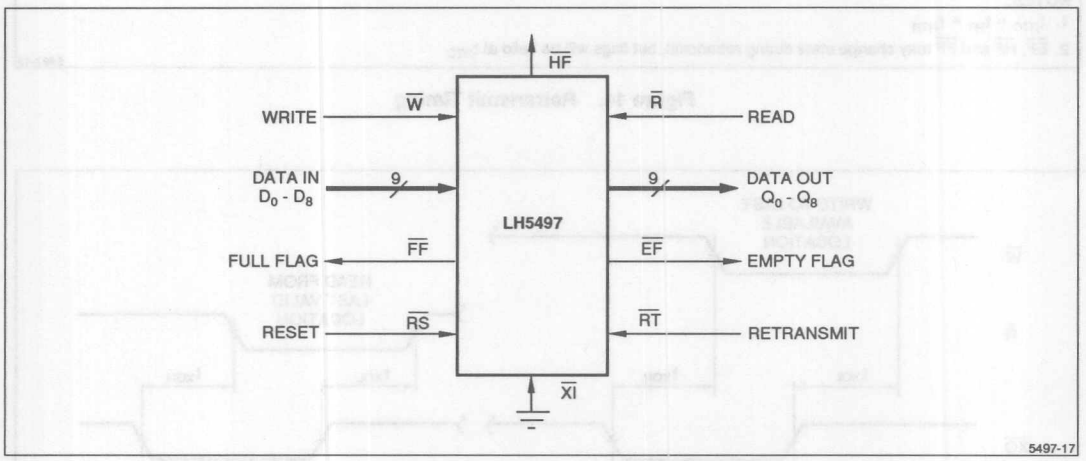


Figure 17. Single FIFO (1K × 9)

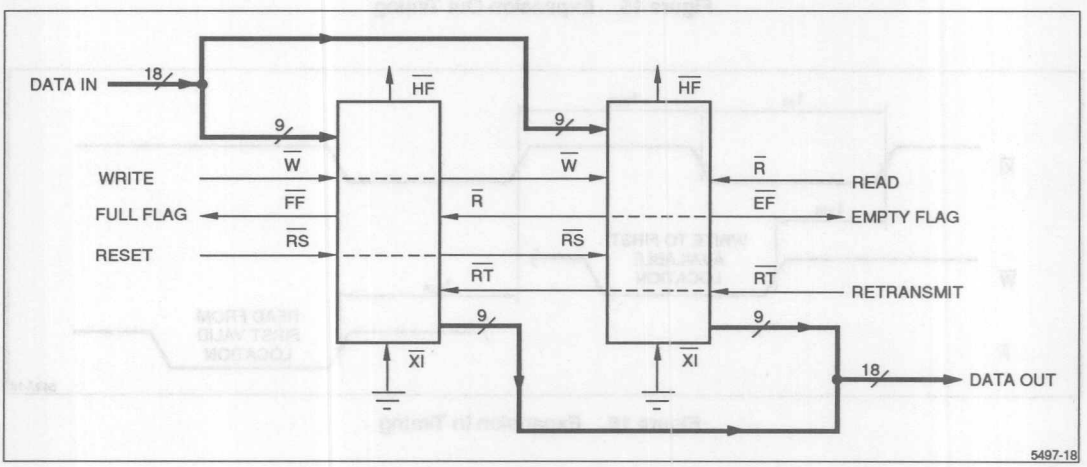


Figure 18. FIFO Width Expansion (1K × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in Expansion mode. In this arrangement, the FIFOs are connected in a circular fashion with the Expansion Out pin ($\overline{XO}$) of each device tied to the Expansion In pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the First Load pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In Expansion mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The Half-Full flag and Retransmit functions are not available in Depth Expansion mode.

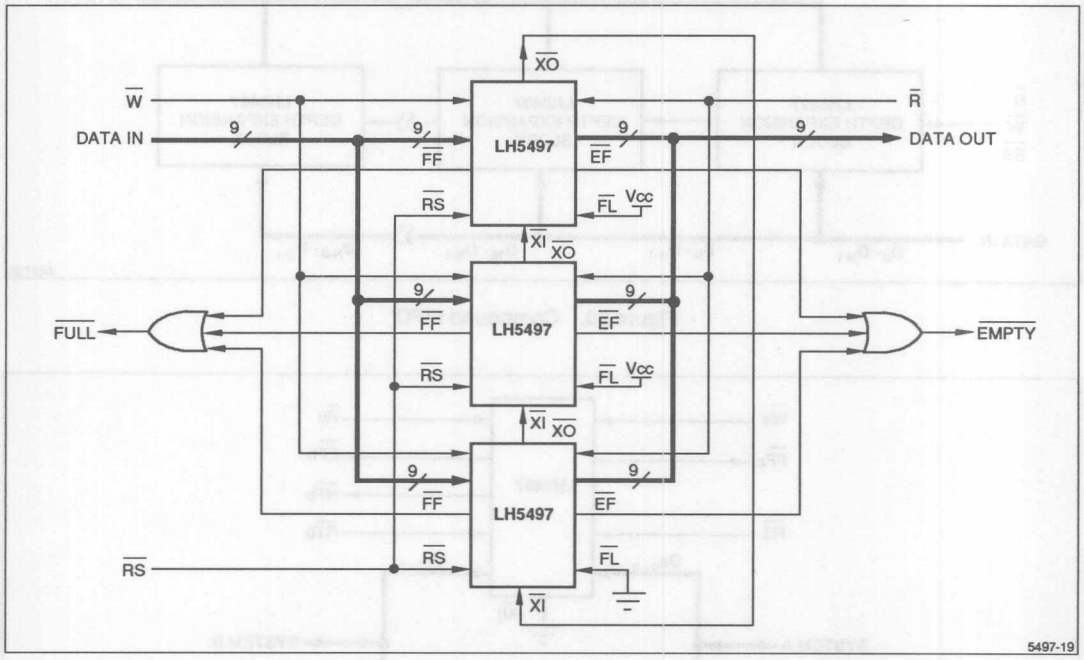


Figure 19. FIFO Depth Expansion (3072 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5497 devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

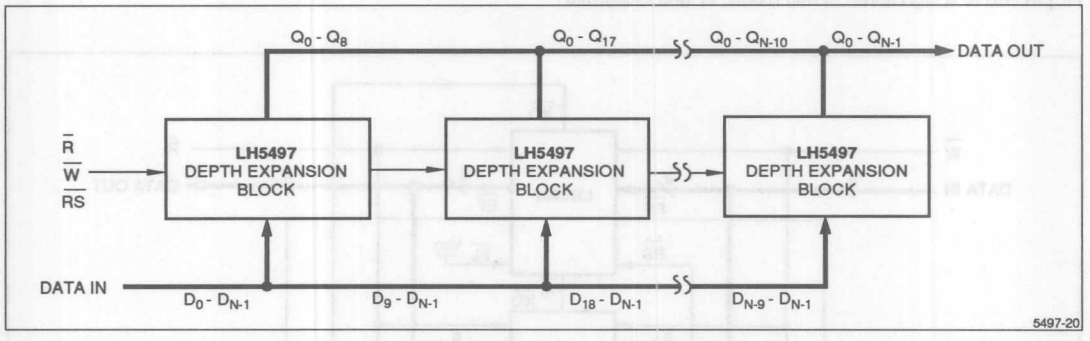


Figure 20. Compound FIFO

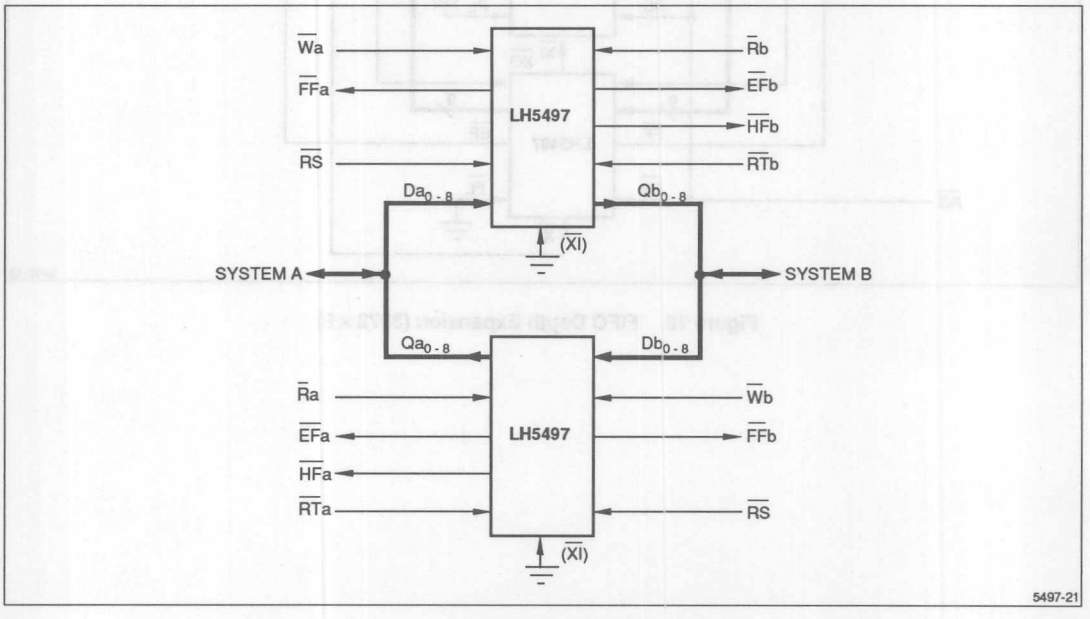
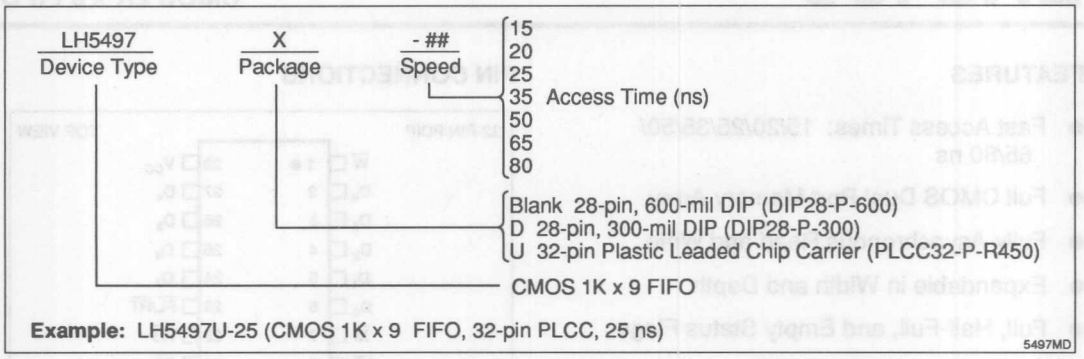


Figure 21. Bidirectional FIFO

ORDERING INFORMATION



LH5498

CMOS 2K × 9 FIFO

FEATURES

- Fast Access Times: 15/20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 300-mil DIP
  28-Pin, 600-mil DIP
  32-Pin PLCC
- Pin and Functionally Compatible with IDT7203

FUNCTIONAL DESCRIPTION

The LH5498 is a dual port memory with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, it provides fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. In addition, internal logic is provided for unlimited expansion in both word size and depth.

Read and Write operations automatically access sequential locations in memory in such a way that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e. Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion In and Expansion Out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

PIN CONNECTIONS

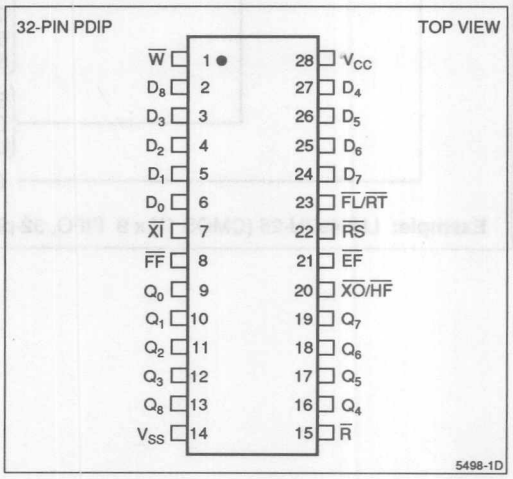


Figure 1. Pin Connections for DIP Package

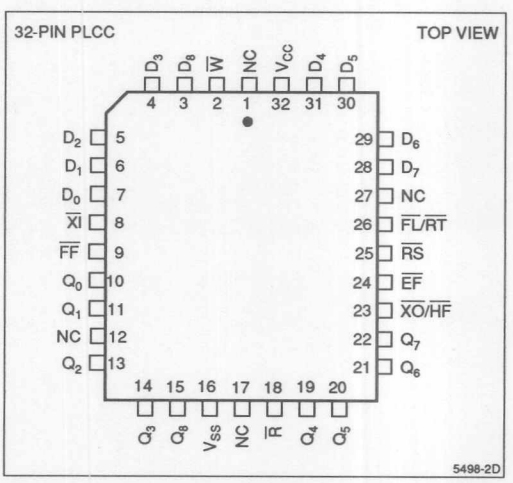


Figure 2. Pin Connections for PLCC Package

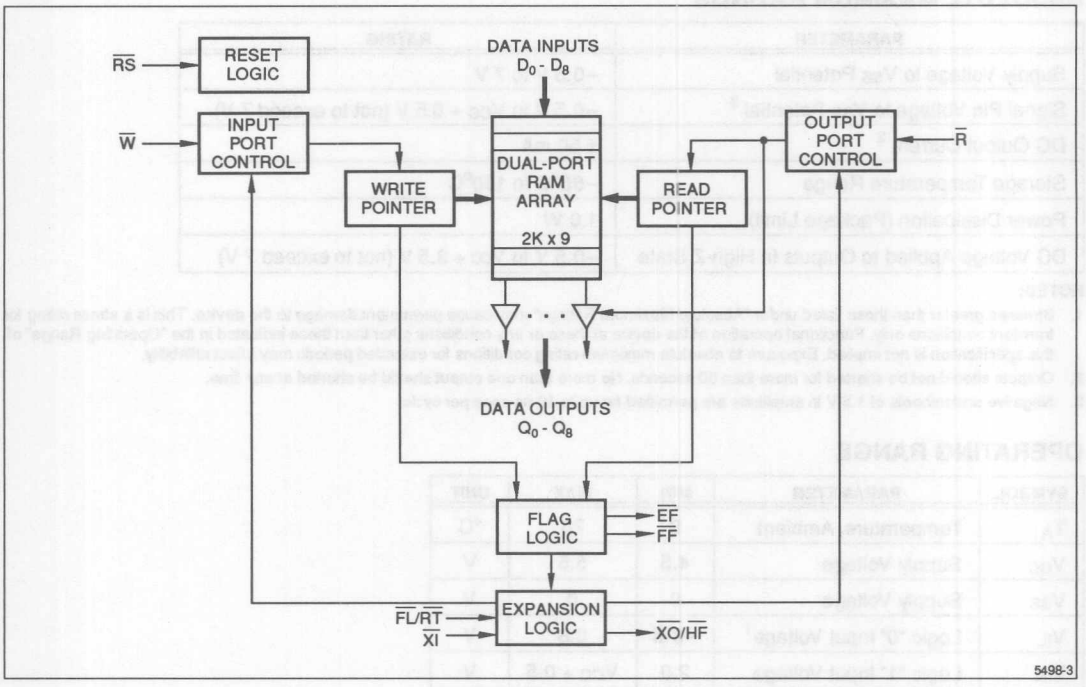


Figure 3. LH5498 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any conditions other than those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic "0" Input Voltage[1]	−0.5	0.8	V
V_{IH}	Logic "1" Input Voltage	2.0	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (OVER OPERATING RANGE)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		5	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
C_O MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{IN} = 0 V.

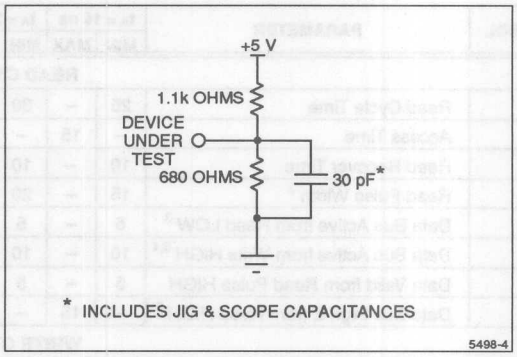


Figure 4. Output Load Circuit

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
RETRANSMIT TIMING																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING																
t_{EFL}	Reset LOW to Empty Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out LOW	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion In Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at "AC Test Condition" levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the Reset pin ($\overline{RS}$) is taken to a LOW state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in Single mode or Depth Expansion mode. A reset pulse is required when the device is first powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a HIGH state t_{RRSS} and t_{WRSS} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the Write ($\overline{W}$) pin. Data setup and hold times must be observed on the data-in ($D_0 - D_8$) pins. A write operation is only possible if the FIFO is not full, (i.e. the Full flag pin is HIGH). Writes may occur independently of any ongoing read operations.

At the falling edge of the first write after the memory is half filled, the Half-Full flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one-half the total capacity of the FIFO. The Half-Full flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The Full flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The Full flag will inhibit further writes until cleared by a valid read. The Full flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the Read ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The Empty flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the Read ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty flag will be momentarily deasserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains LOW, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the Write ($\overline{W}$) pin is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the Full flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be re-accessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 2048 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

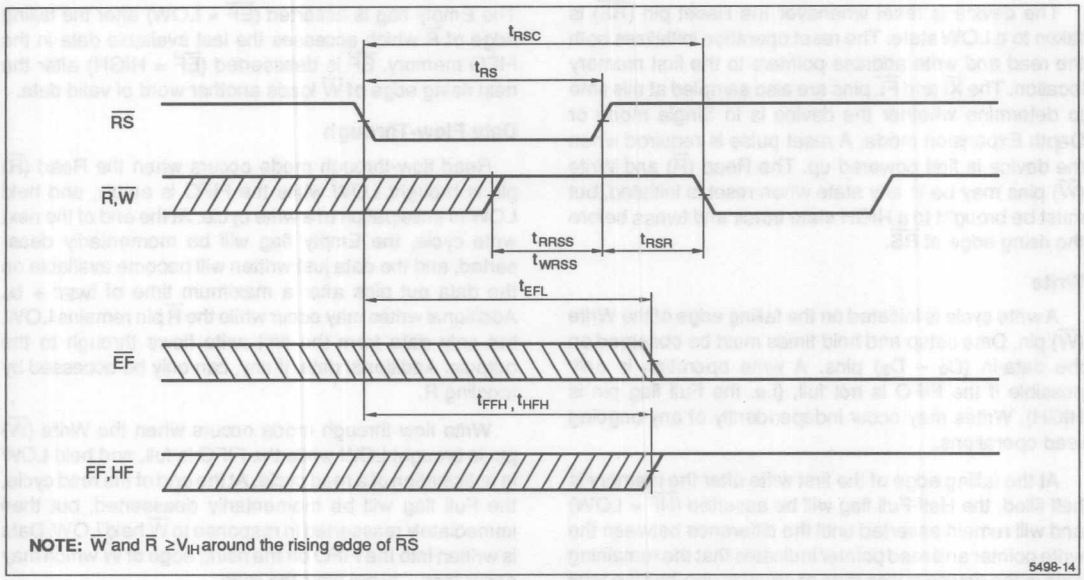


Figure 5. Reset Timing

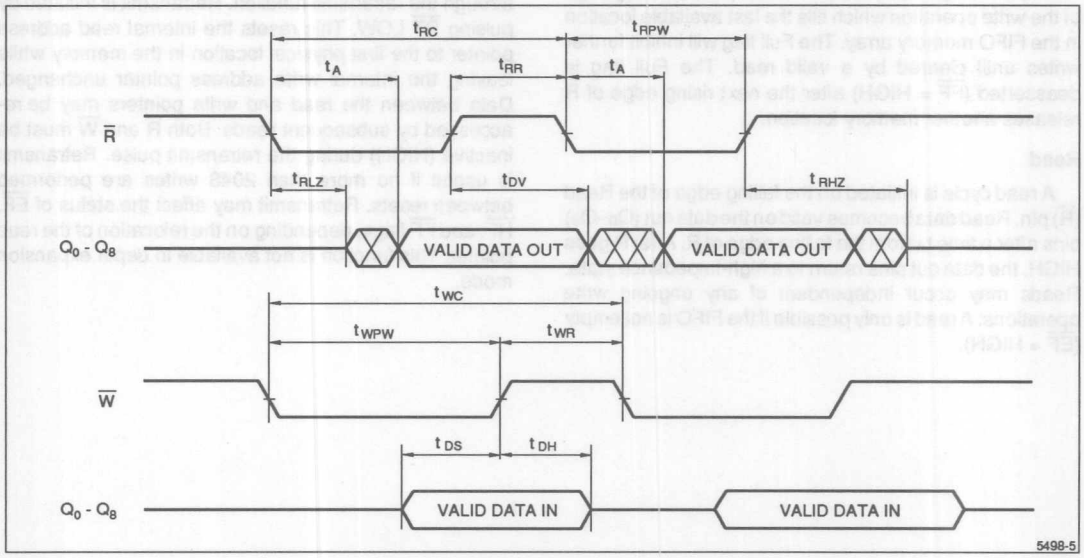


Figure 6. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

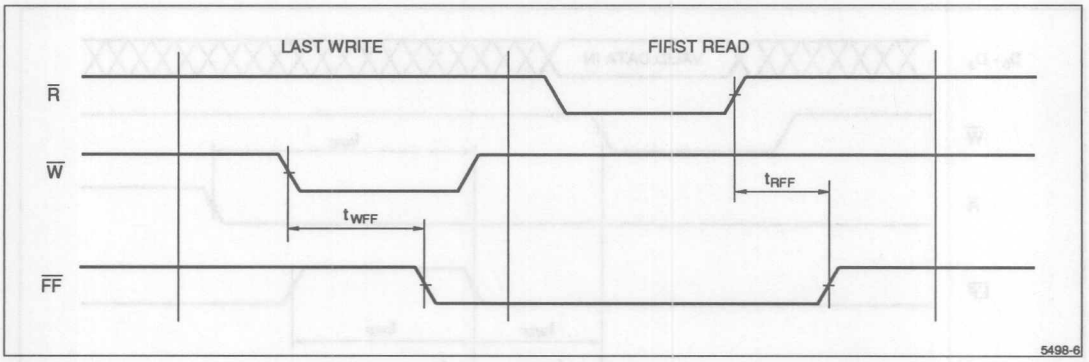


Figure 7. Full Flag from Last Write to First Read

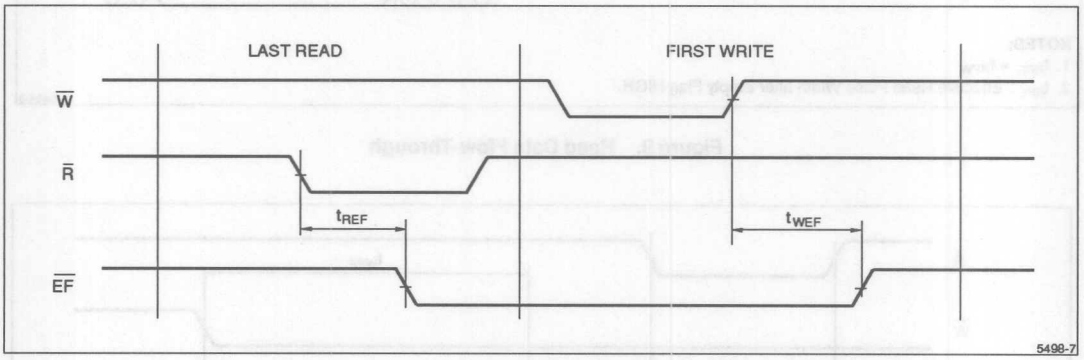


Figure 8. Empty Flag from Last Read to First Write

TIMING DIAGRAMS (cont'd)

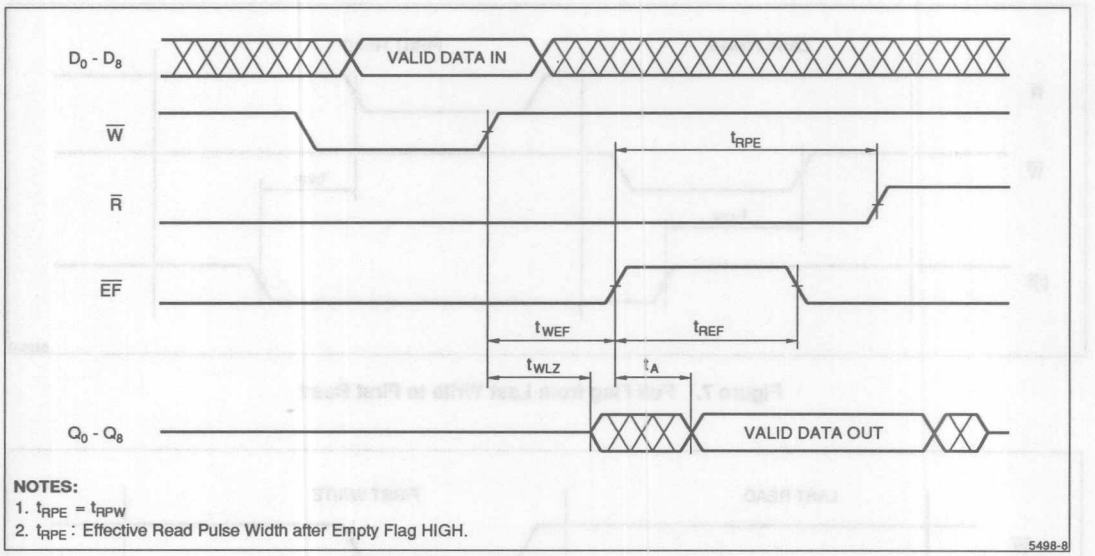


Figure 9. Read Data Flow-Through

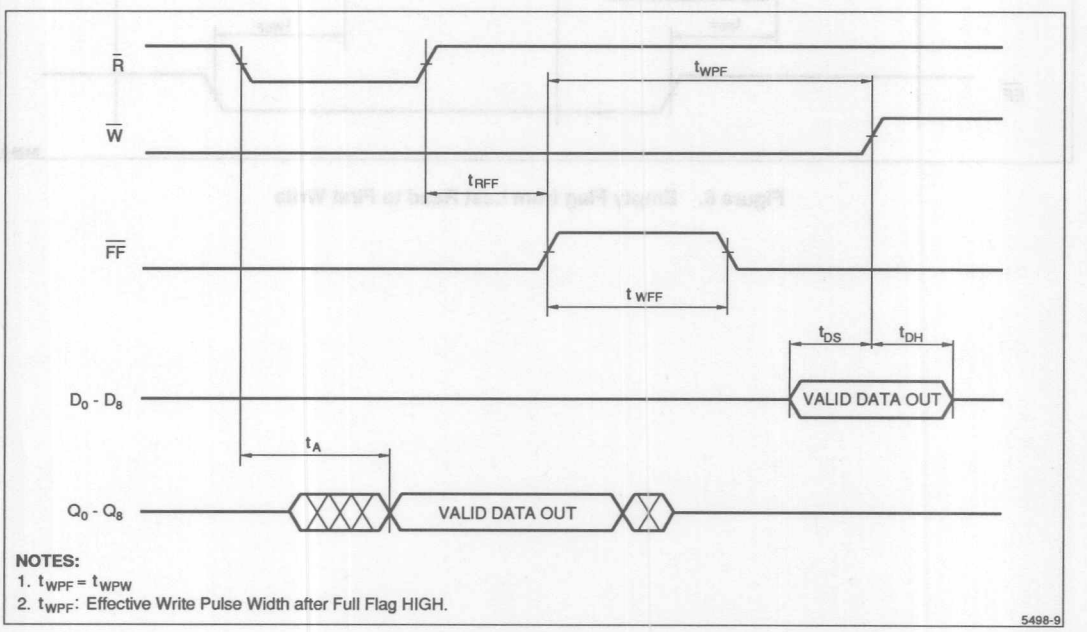


Figure 10. Write Data Flow-Through

TIMING DIAGRAMS (cont'd)

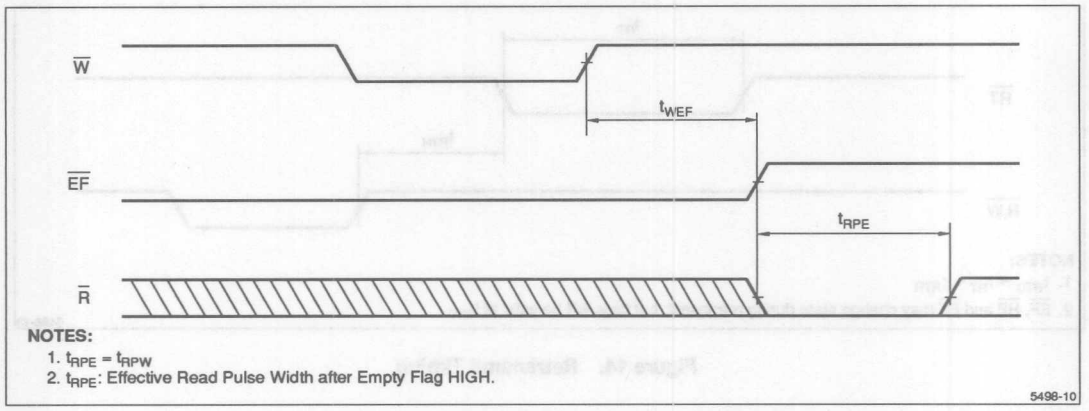


Figure 11. Empty Flag Timing

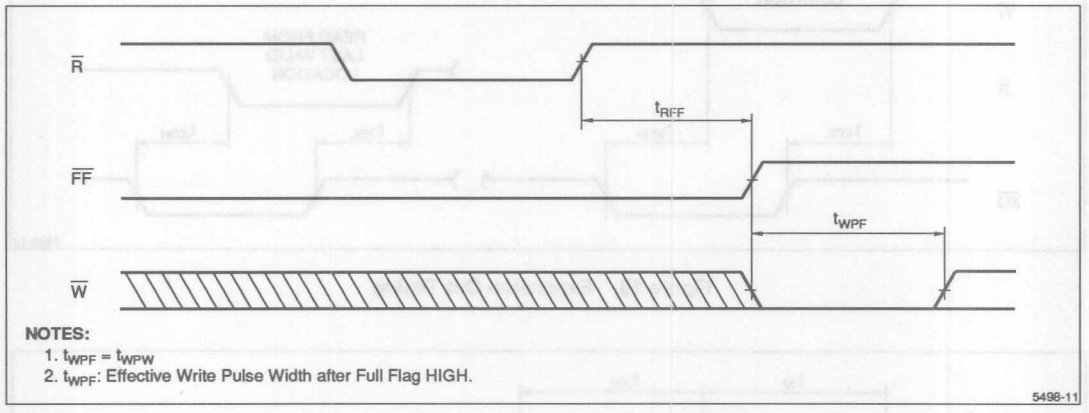


Figure 12. Full Flag Timing

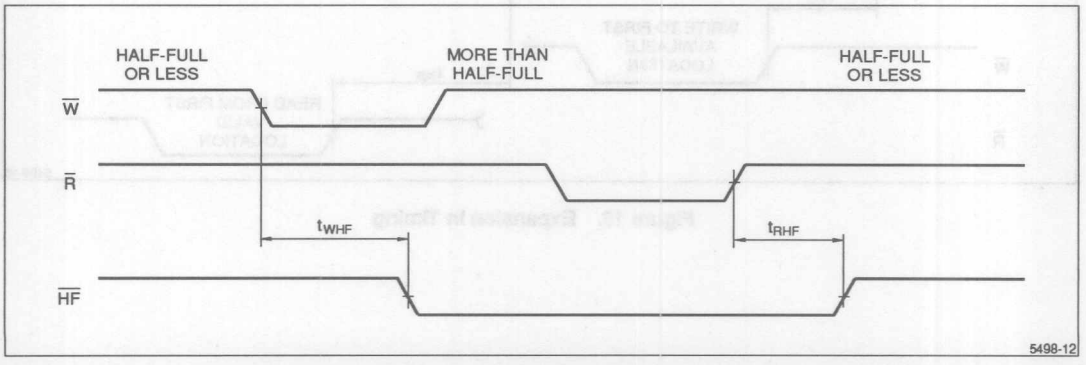


Figure 13. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)

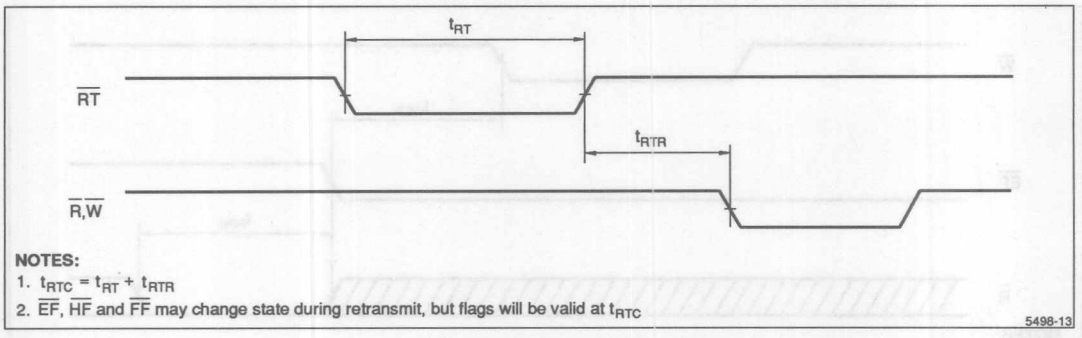


Figure 14. Retransmit Timing

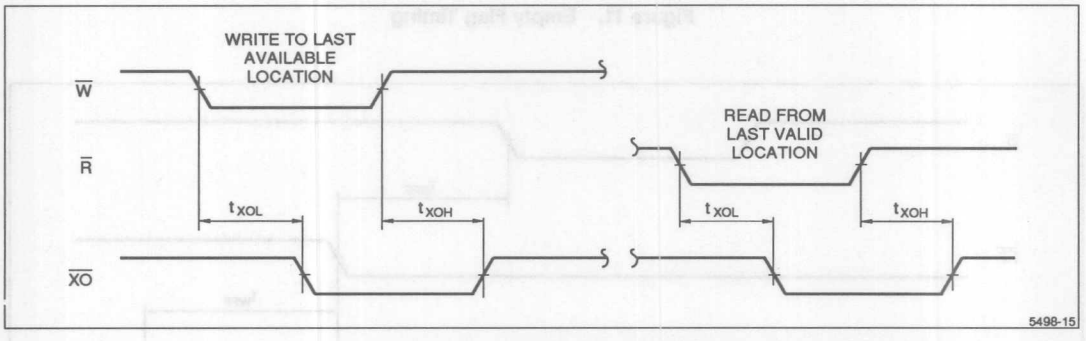


Figure 15. Expansion Out Timing

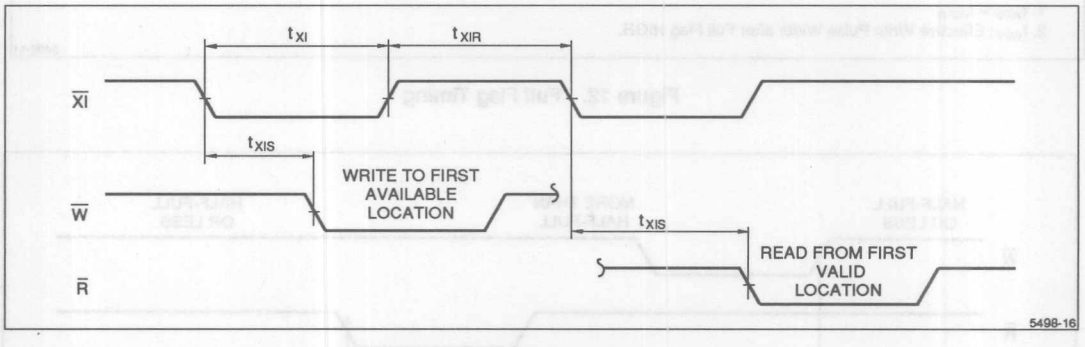


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in Single mode by tying the Expansion In pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word-width expansion is implemented by placing multiple LH5498 devices in parallel. Each LH5498 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 17 and 18.)

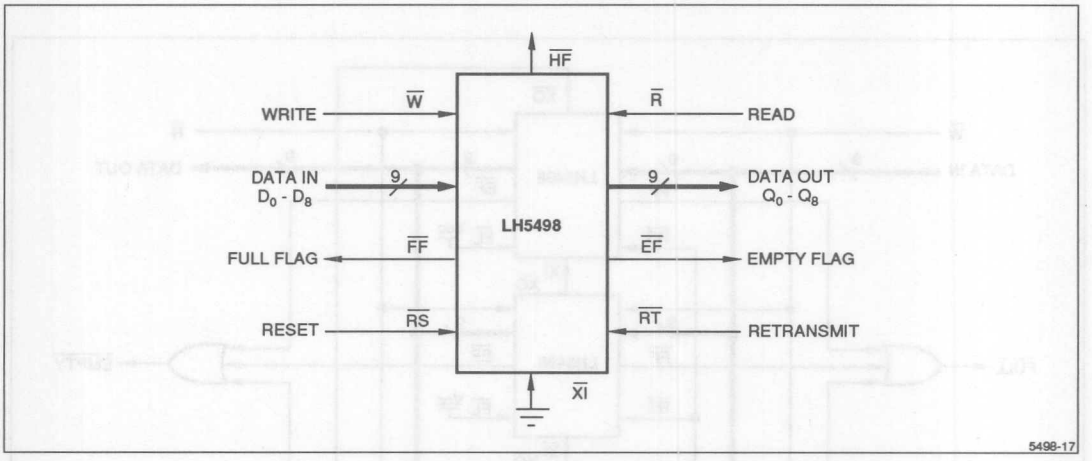


Figure 17. Single FIFO (2K × 9)

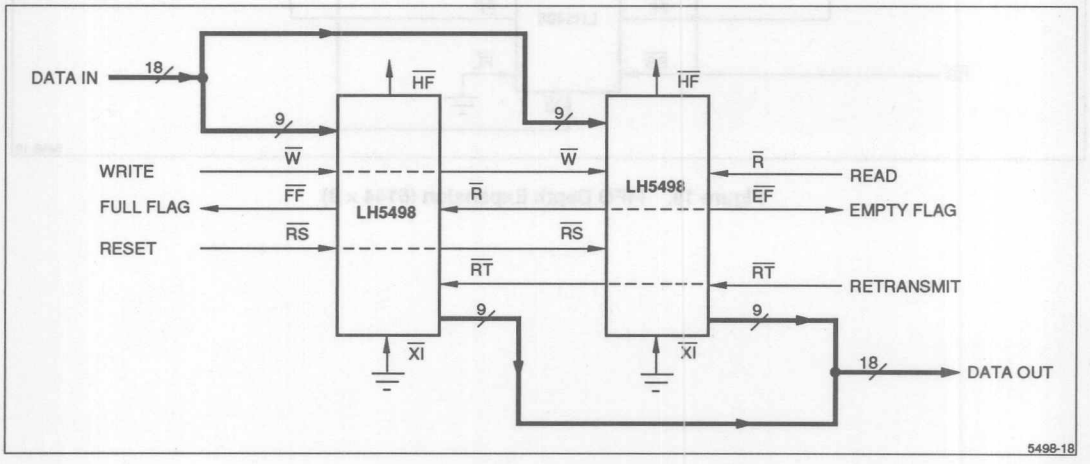


Figure 18. FIFO Width Expansion (2K × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in Expansion mode. In this arrangement, the FIFOs are connected in a circular fashion with the Expansion Out pin ($\overline{XO}$) of each device tied to the Expansion In pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the First Load pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In Expansion mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The Half-Full flag and Retransmit functions are not available in Depth Expansion mode.

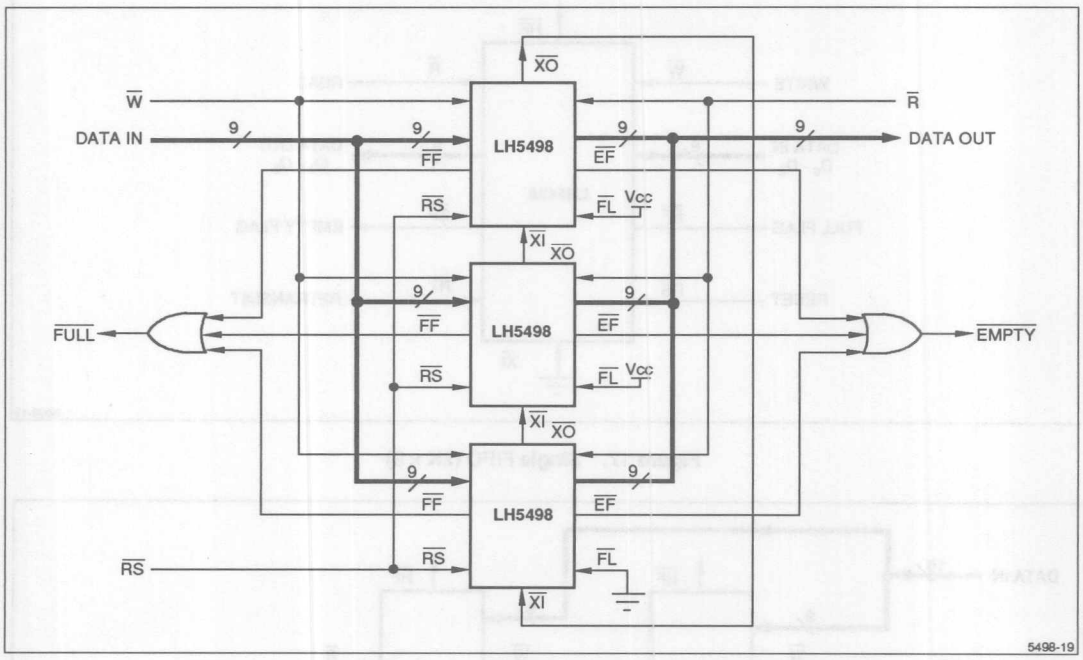


Figure 19. FIFO Depth Expansion (6144 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5498 devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

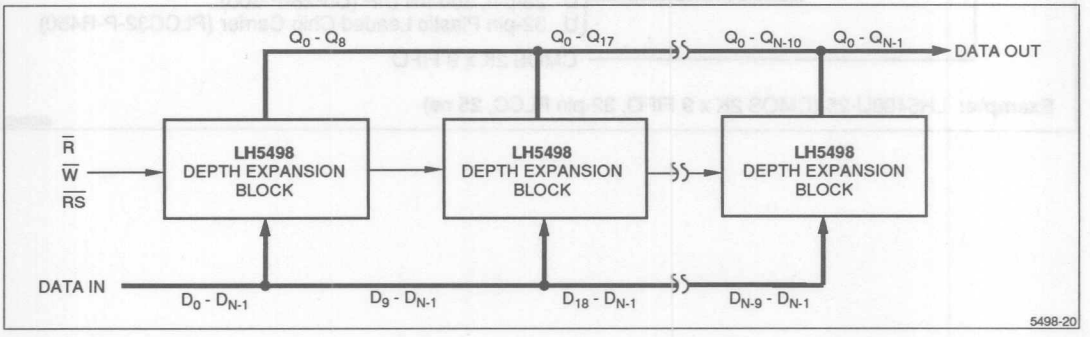


Figure 20. Compound FIFO

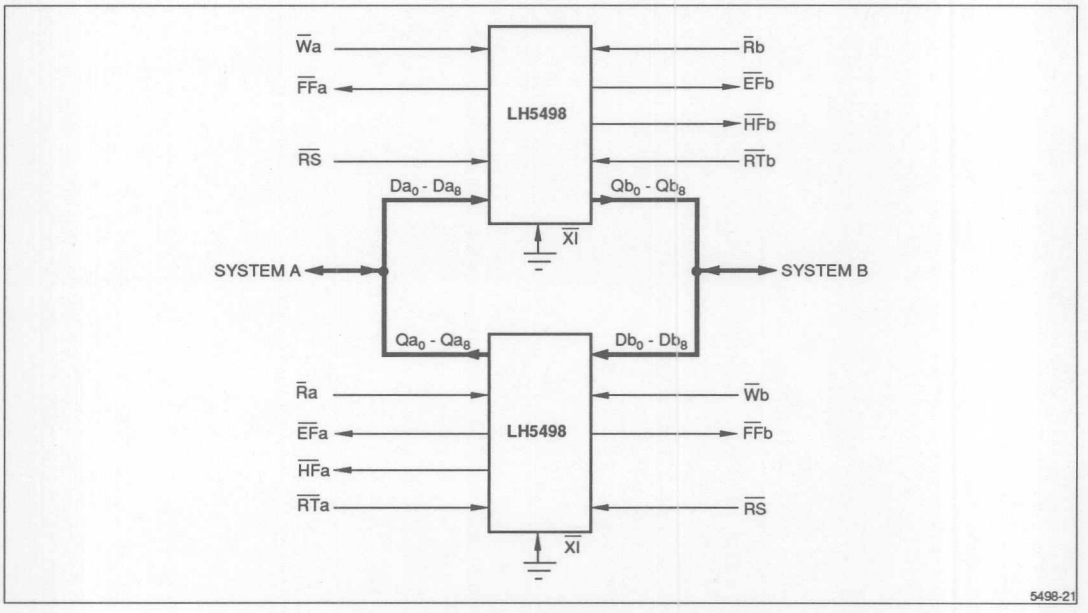
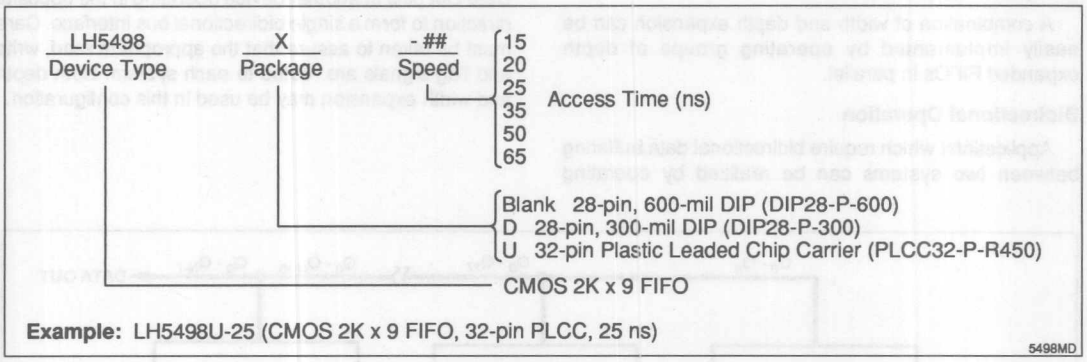


Figure 21. Bidirectional FIFO

ORDERING INFORMATION



LH5499

CMOS 4K × 9 FIFO

FEATURES

- Fast Access Times: 20/25/35/50/65/80 ns
- Full CMOS Dual Port Memory Array
- Fully Asynchronous Read and Write
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Read Retransmit Capability
- TTL Compatible I/O
- Packages:
  28-Pin, 600-mil DIP
  32-Pin, PLCC
- Pin and Functionally Compatible with IDT7204

FUNCTIONAL DESCRIPTION

The LH5499 is a dual port memory with internal addressing to implement a First-In, First-Out algorithm. Through an advanced dual port architecture, it provides fully asynchronous read/write operation. Empty, Full, and Half-Full status flags are provided to prevent data overflow and underflow. Internal logic is provided for unlimited expansion in both word size and depth.

Read and Write operations automatically access sequential locations in memory in such a way that data is read out in the same order that it was written, that is on a First-In, First-Out basis. Since the address sequence is internally predefined, no external address information is required for the operation of this device. A ninth data bit is provided for parity or control information often needed in communication applications.

Empty, Full, and Half-Full status flags monitor the extent to which data has been written into the FIFO, and prevent improper operations (i.e., Read if the FIFO is empty, or Write if the FIFO is full). A retransmit feature resets the Read address pointer to its initial position, thereby allowing repetitive readout of the same data. Expansion in and Expansion out pins implement an expansion scheme that allows individual FIFOs to be cascaded to greater depth without incurring additional latency (bubblethrough) delays.

PIN CONNECTIONS

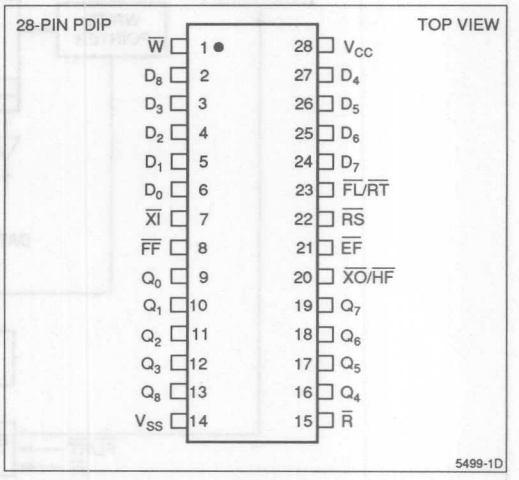


Figure 1. Pin Connections for PDIP Package

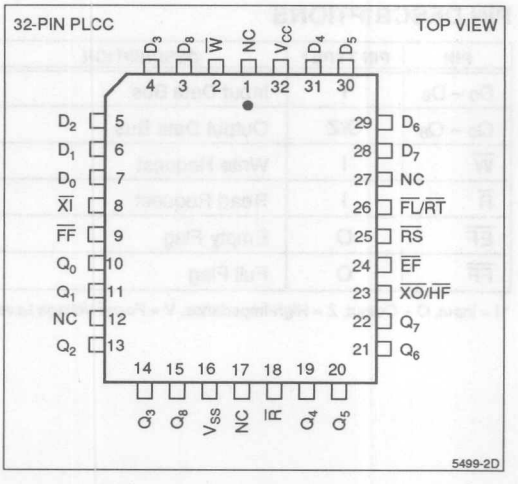


Figure 2. Pin Connections for PLCC Package

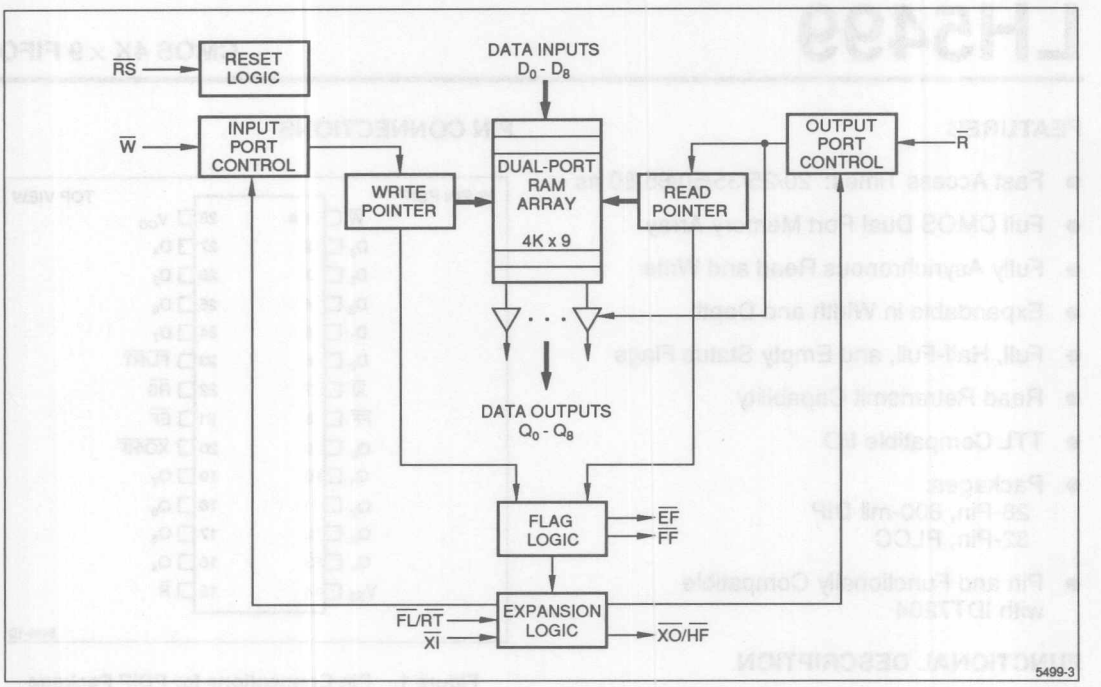


Figure 3. LH5499 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag

PIN	PIN TYPE *	DESCRIPTION
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to Vss Potential	−0.5 V to 7 V
Signal Pin Voltage to Vss Potential [3]	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)
DC Output Current [2]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to Vcc + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions above those indicated in the "Operating Range" of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic "0" Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic "1" Input Voltage	2.0	Vcc + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output High Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output Low Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 33 MHz		110	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		8	mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 4

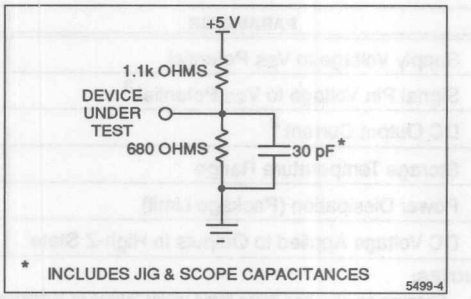


Figure 4. Output Load Caption

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
C_O MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING														
t_{RC}	Read Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recover Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING														
t_{WC}	Write Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING														
t_{RSC}	Reset Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	65	–	80	–	ns
RETRANSMIT TIMING [5]														
t_{RTC}	Retransmit Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING														
t_{EFL}	Reset LOW to Empty Flag LOW	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset LOW to Half-Full and Full Flags HIGH	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	25	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	30	–	35	–	45	–	65	–	80	–	100	ns
EXPANSION TIMING														
t_{XOL}	Expansion Out LOW	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements performed at "AC Test Condition" levels.
2. Pulse widths less than minimum value are not allowed.
3. Values guaranteed by design not currently tested.
4. Only applies to read data flow-through mode.
5. See also Note 3, Figure 13.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the Reset pin ($\overline{RS}$) is taken to a LOW state. The reset operation initializes both the read and write address pointers to the first memory location. The $\overline{XI}$ and $\overline{FL}$ pins are also sampled at this time to determine whether the device is in Single mode or Depth Expansion mode. A reset pulse is required when the device is first powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) pins may be in any state when reset is initiated, but must be brought to a HIGH state t_{RPW} and t_{WPW} before the rising edge of $\overline{RS}$.

Write

A write cycle is initiated on the falling edge of the Write ($\overline{W}$) pin. Data setup and hold times must be observed on the data in (D_0 – D_8) pins. A write operation is only possible if the FIFO is not full, (i.e. the Full flag pin is HIGH). Writes may occur independently of any ongoing read operations.

At the falling edge of the first write after the memory is half filled, the Half-Full flag will be asserted ($\overline{HF}$ = LOW) and will remain asserted until the difference between the write pointer and read pointer indicates that the remaining data in the device is less than or equal to one half the total capacity of the FIFO. The Half-Full flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$.

The Full flag is asserted ($\overline{FF}$ = LOW) at the falling edge of the write operation which fills the last available location in the FIFO memory array. The Full flag will inhibit further writes until cleared by a valid read. The Full flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location.

Read

A read cycle is initiated on the falling edge of the Read ($\overline{R}$) pin. Read data becomes valid on the data out (Q_0–Q_8) pins after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data out pins return to a high-impedance state. Reads may occur independent of any ongoing write operations. A read is only possible if the FIFO is not empty ($\overline{EF}$ = HIGH).

The internal read and write address pointers are maintained by the device such that consecutive read operations will access data in the same order as it was written. The Empty flag is asserted ($\overline{EF}$ = LOW) after the falling edge of $\overline{R}$ which accesses the last available data in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another word of valid data.

Data Flow-Through

Read flow-through mode occurs when the Read ($\overline{R}$) pin is brought LOW while the FIFO is empty, and held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty flag will be momentarily de-asserted, and the data just written will become available on the data out pins after a maximum time of $t_{WEF} + t_A$. Additional writes may occur while the $\overline{R}$ pin remains LOW, but only data from the first write flows through to the outputs. Additional data, if any, can only be accessed by toggling $\overline{R}$.

Write flow-through mode occurs when the Write ($\overline{W}$) pin is brought LOW while the FIFO is full, and held LOW in anticipation of a read cycle. At the end of the read cycle, the Full flag will be momentarily deasserted, but then immediately reasserted in response to $\overline{W}$ held LOW. Data is written into the FIFO on the rising edge of $\overline{W}$ which may occur $t_{RFF} + t_{WPW}$ after the read.

Retransmit

The FIFO can be made to reread previously read data through the retransmit function. Retransmit is initiated by pulsing $\overline{RT}$ LOW. This resets the internal read address pointer to the first physical location in the memory while leaving the internal write address pointer unchanged. Data between the read and write pointers may be reaccessed by subsequent reads. Both $\overline{R}$ and $\overline{W}$ must be inactive (HIGH) during the retransmit pulse. Retransmit is useful if no more than 4096 writes are performed between resets. Retransmit may affect the status of $\overline{EF}$, $\overline{HF}$, and $\overline{FF}$ flags, depending on the relocation of the read pointer. This function is not available in depth expansion mode.

TIMING DIAGRAMS

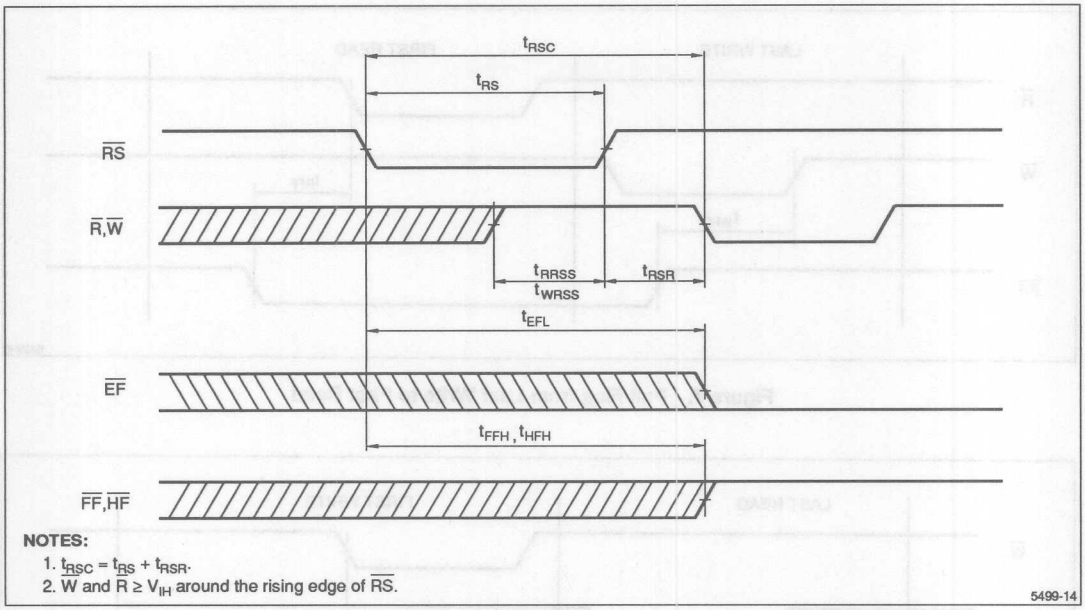


Figure 5. Reset Timing

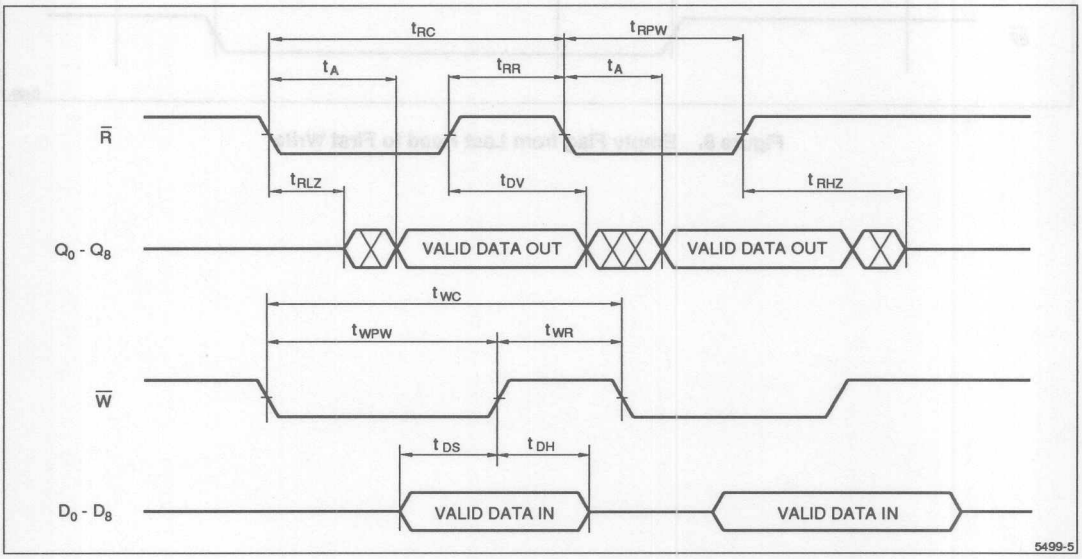


Figure 6. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

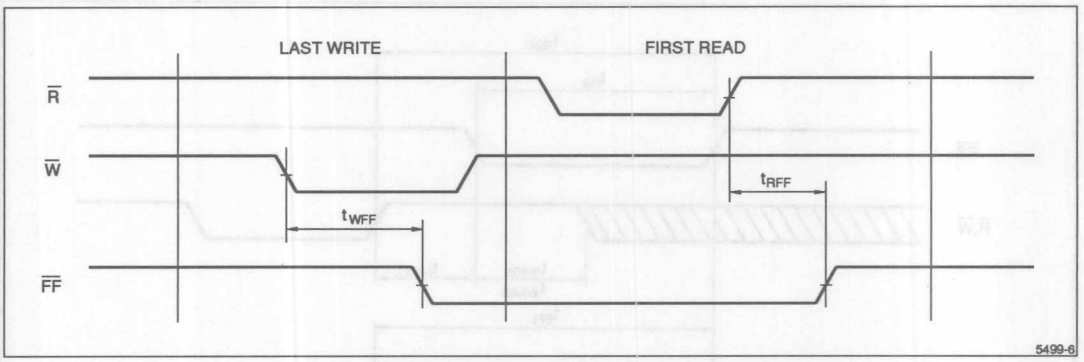


Figure 7. Full Flag from Last Write to First Read

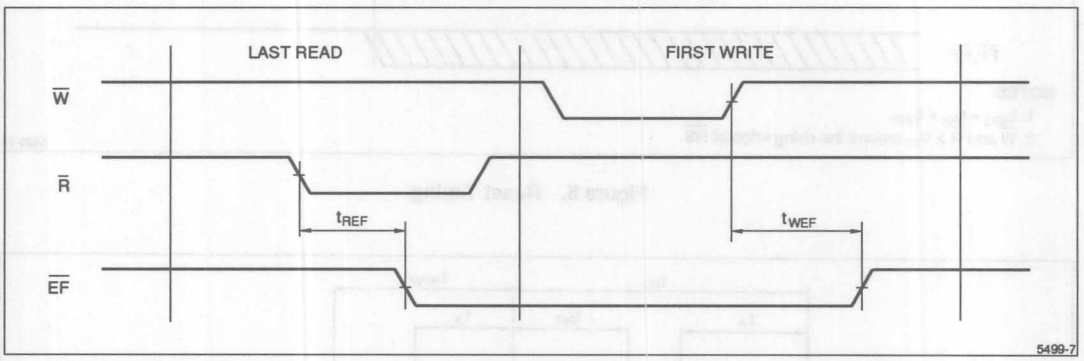


Figure 8. Empty Flag from Last Read to First Write

TIMING DIAGRAMS (cont'd)

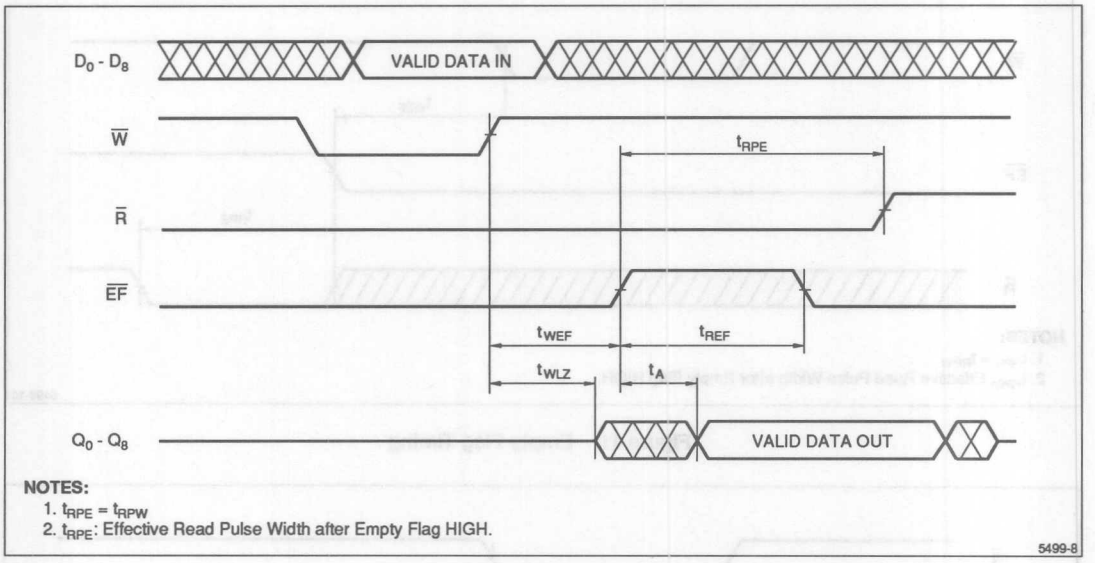


Figure 9. Read Data Flow-Through

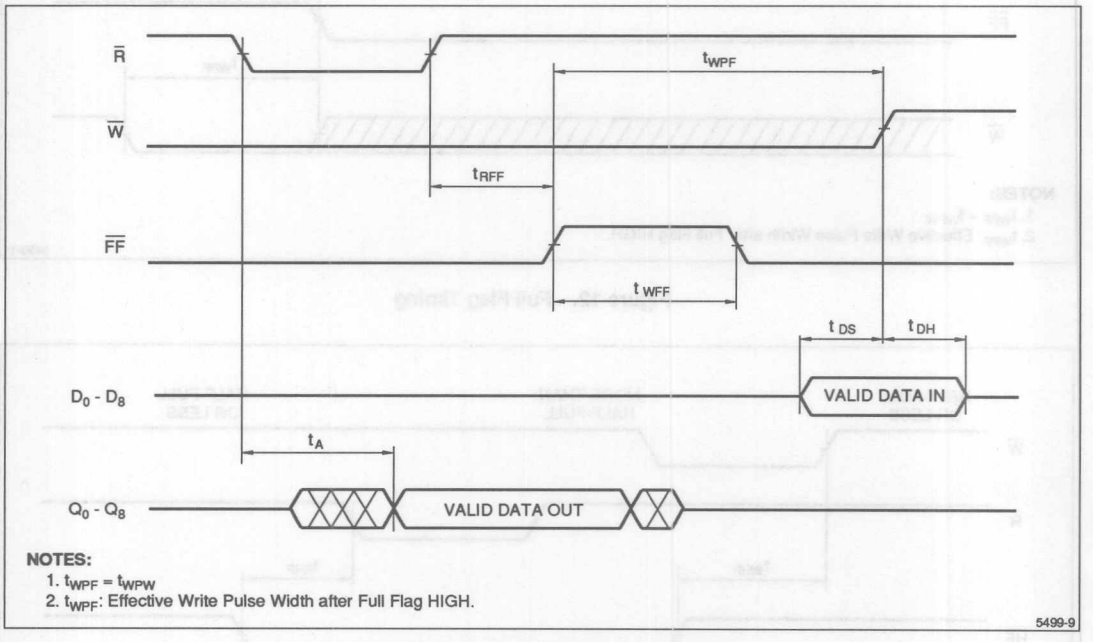


Figure 10. Write Data Flow-Through

TIMING DIAGRAMS (cont'd)

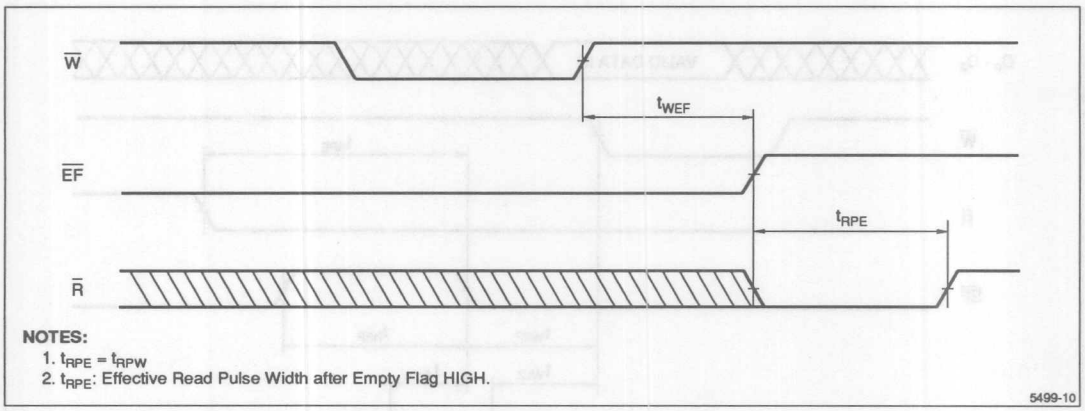


Figure 11. Empty Flag Timing

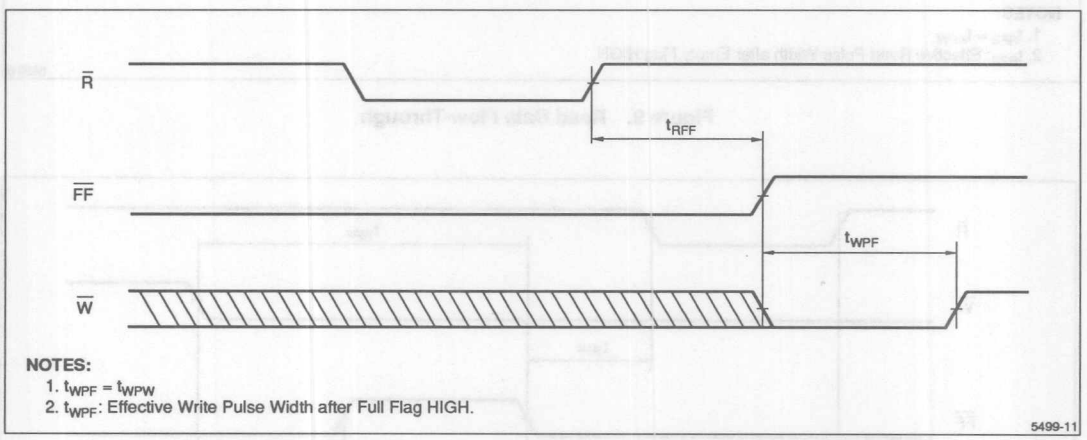


Figure 12. Full Flag Timing

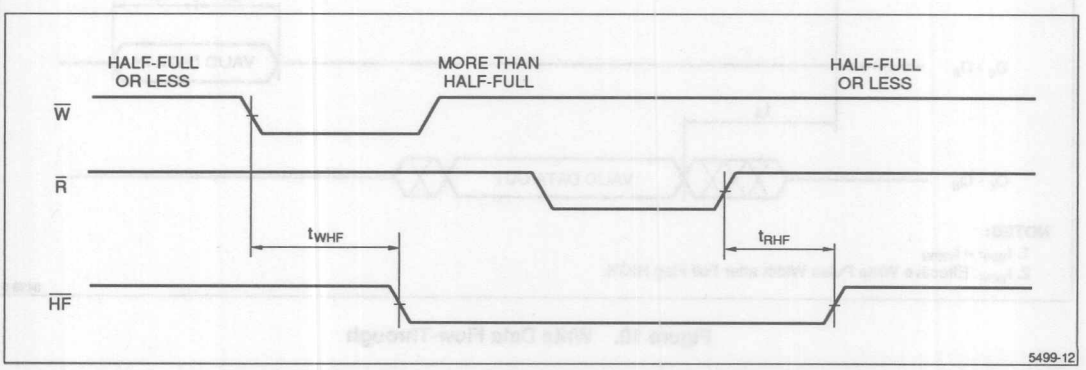
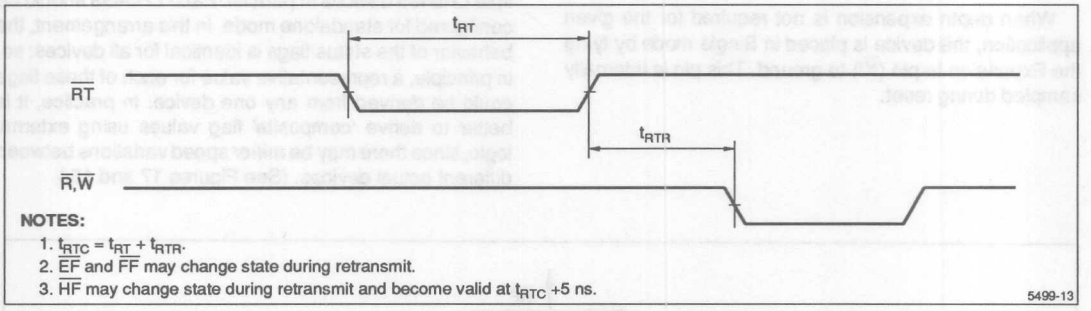


Figure 13. Half-Full Flag Timing

TIMING DIAGRAMS (cont'd)



NOTES:

1. $t_{RTC} = t_{RT} + t_{RTR}$.
2. $\overline{EF}$ and $\overline{FF}$ may change state during retransmit.
3. $\overline{HF}$ may change state during retransmit and become valid at t_{RTC} +5 ns.

Figure 14. Retransmit Timing

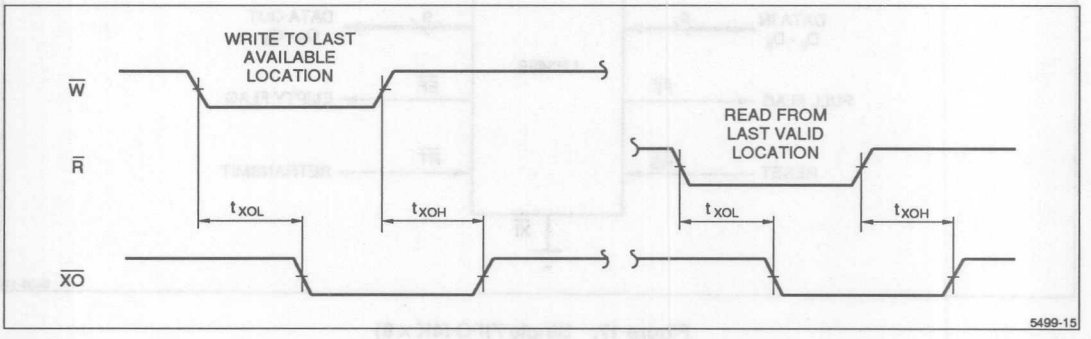


Figure 15. Expansion Out Timing

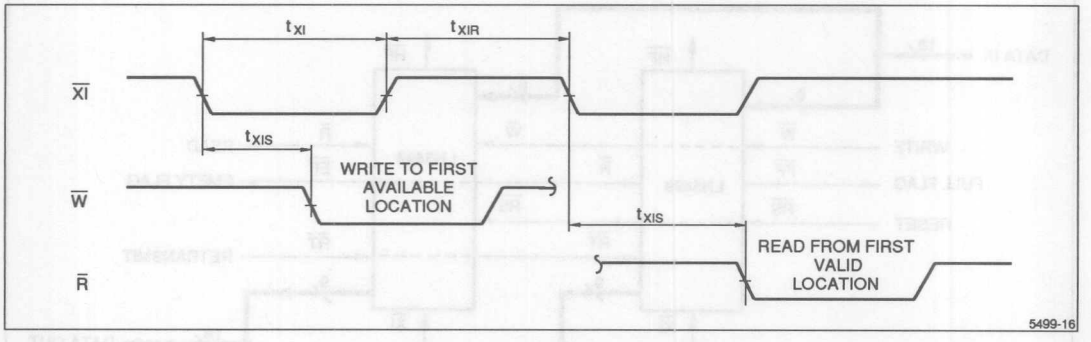


Figure 16. Expansion In Timing

OPERATIONAL MODES

Single Device Configuration

When depth expansion is not required for the given application, the device is placed in Single mode by tying the Expansion In pin ($\overline{XI}$) to ground. This pin is internally sampled during reset.

Width Expansion

Word-width expansion is implemented by placing multiple LH5499 devices in parallel. Each LH5499 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 17 and 18.)

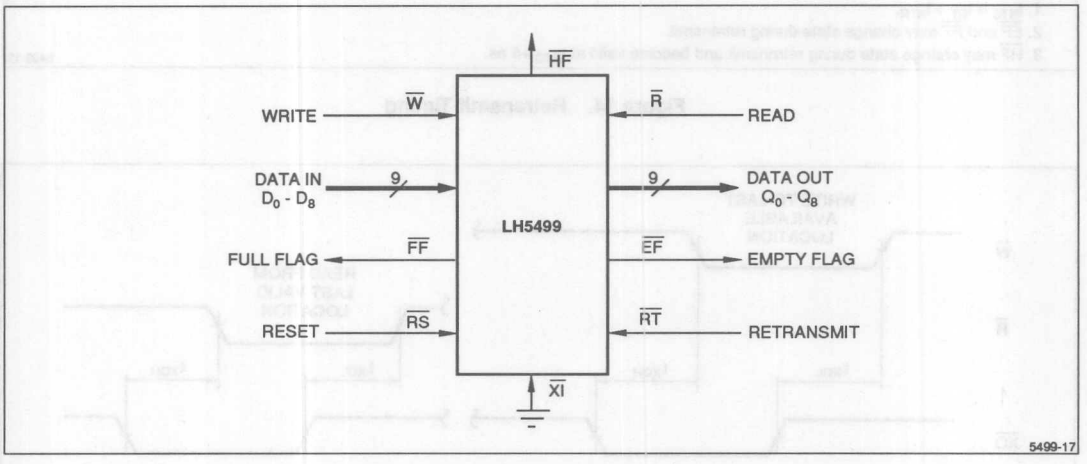


Figure 17. Single FIFO (4K × 9)

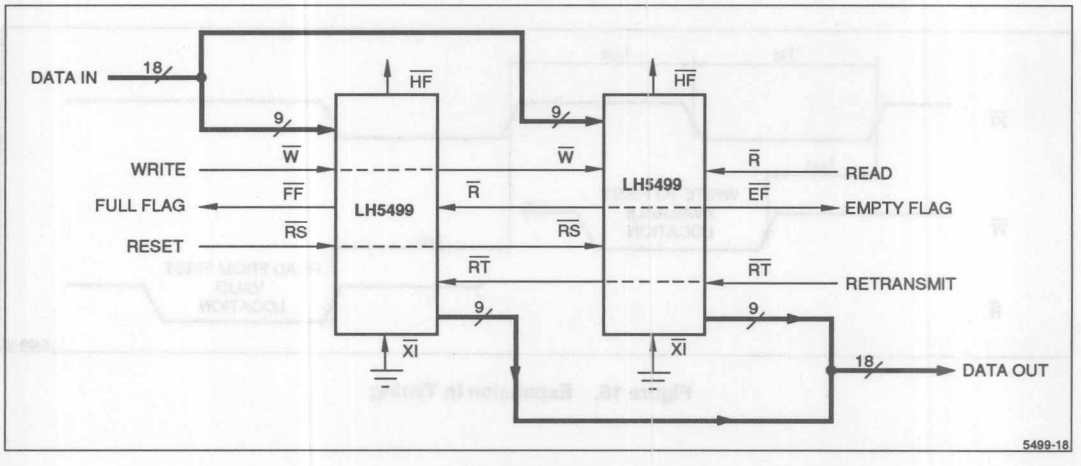


Figure 18. FIFO Width Expansion (4K × 18)

OPERATIONAL MODES (cont'd)

Depth Expansion

Depth expansion is implemented by configuring the required number of FIFOs in Expansion mode. In this arrangement, the FIFOs are connected in a circular fashion with the Expansion Out pin ($\overline{XO}$) of each device tied to the Expansion In pin ($\overline{XI}$) of the next device. One FIFO in this group must be designated as the first load device. This is accomplished by tying the First Load pin ($\overline{FL}$) of this device to ground. All other devices must have their $\overline{FL}$ pin tied to a high level. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while internal logic controls the steering of data. Only one FIFO will be enabled for any given read cycle, so the common Data Out pins of all devices are wire-ORed together. Likewise, the common Data In pins of all devices are tied together.

In Expansion mode, external logic is required to generate a composite Full or Empty flag. This is achieved by ORing the $\overline{FF}$ pins of all devices and ORing the $\overline{EF}$ pins of all devices respectively. The Half-Full flag and Retransmit functions are not available in Depth Expansion mode.

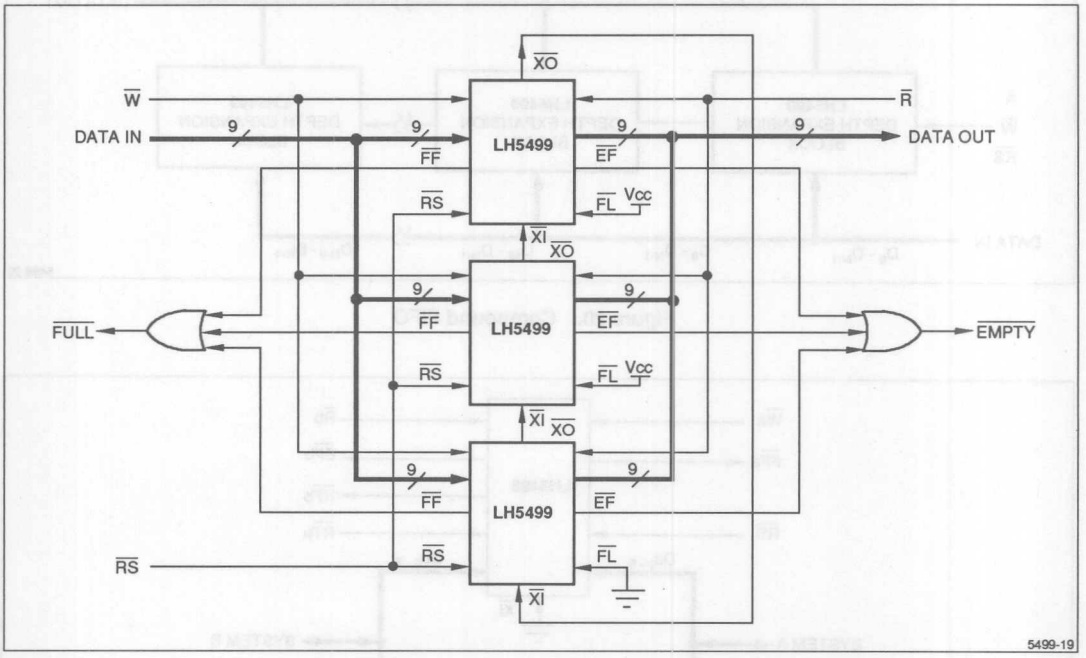


Figure 19. FIFO Depth Expansion (12288 × 9)

OPERATIONAL MODES (cont'd)

Compound Expansion

A combination of width and depth expansion can be easily implemented by operating groups of depth expanded FIFOs in parallel.

Bidirectional Operation

Applications which require bidirectional data buffering between two systems can be realized by operating LH5499 devices in parallel but opposite directions. The Data In pins of a device may be tied to the corresponding Data Out pins of another device operating in the opposite direction to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write and flag signals are routed to each system. Both depth and width expansion may be used in this configuration.

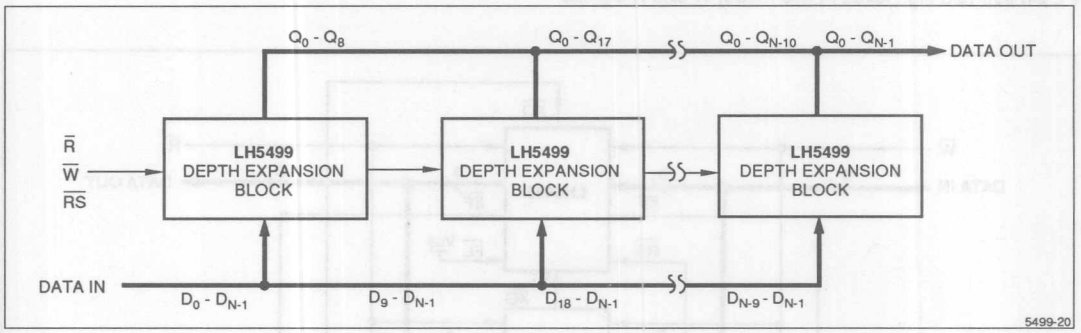


Figure 20. Compound FIFO

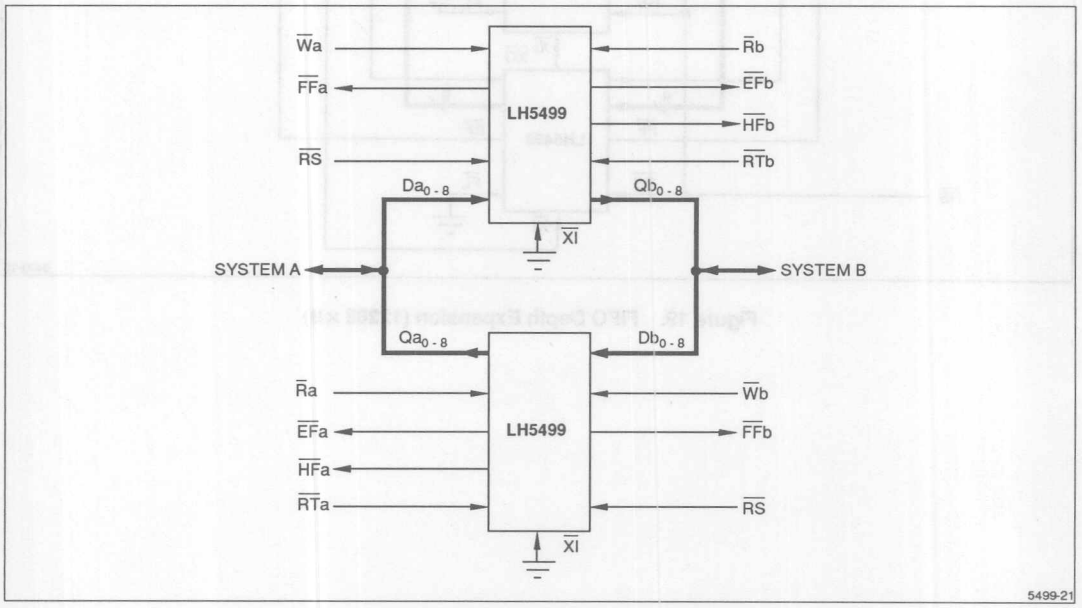
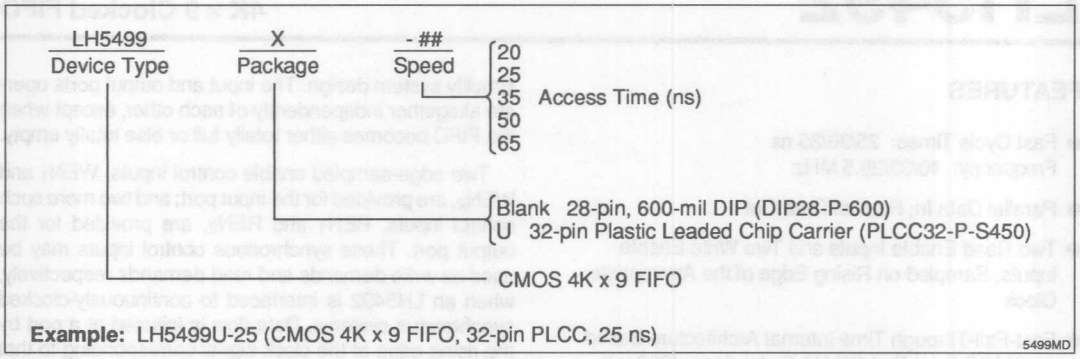


Figure 21. Bidirectional FIFO

ORDERING INFORMATION



LH5492

4K × 9 Clocked FIFO

FEATURES

- Fast Cycle Times: 25/30/35 ns
  Frequency: 40/33/28.5 MHz
- Parallel Data In; Parallel Data Out
- Two Read Enable Inputs and Two Write Enable Inputs, Sampled on Rising Edge of the Appropriate Clock
- Fast-Fall-Through Time Internal Architecture Based on CMOS Dual-Port SRAM Technology, 4096 × 9
- Independently-Synchronized Operation of Input Port and Output Port
- Full, Half-Full, Almost-Empty/Full, and Empty Flags
- Three-State Outputs with Output Enable
- May be Used for Bidirectional Bus Interfaces
- May be Used to Interface between Buses of Different Word Widths
- Reset/Reread Capability
- TTL and CMOS Compatible I/O
- 32-Pin PLCC Package

FUNCTIONAL DESCRIPTION

The LH5492 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port RAM technology, capable of containing up to 4096 nine-bit words. A single LH5492 FIFO can input and output nine-bit bytes; it has one nine-bit parallel input (write) port, and one nine-bit parallel output (read) port. Multiple write enables and read enables support paralleling LH5492s for greater-word-width operation, in order to achieve a *wider* 'effective FIFO.' The paralleled LH5492 combination remains capable of performing all of the operations which a standalone LH5492 can perform. Thus, if two LH5492s are paralleled, the combination can input and output 18-bit halfwords. This paralleling scheme extends to an *arbitrary* number of paralleled LH5492s, although some external logic is required for more than two.

The LH5492 architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals; they do not need to be synchronized with each other in any way. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design. The input and output ports operate altogether independently of each other, except when the FIFO becomes either totally full or else totally empty.

Two edge-sampled enable control inputs, WEN_1 and WEN_2, are provided for the input port; and two more such control inputs, REN_1 and REN_2, are provided for the output port. These synchronous control inputs may be used as write demands and read demands respectively, when an LH5492 is interfaced to continuously-clocked synchronous systems. Data flow is initiated at a port by the rising edge of the clock signal corresponding to that port, and is gated only by the appropriate edge-sampled enable control input signal(s).

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Half-Full, Almost-Empty/Full, and Empty. The Almost-Empty/Full flag is asserted whenever the internal memory is either within eight locations of 'empty,' or else within eight locations of 'full.' The Half-Full flag serves to distinguish the 'almost-empty' condition from the 'almost-full' condition. Also, during fully-synchronous operation, the Full flag may be tied directly to WEN_1 or to WEN_2, and the Empty flag likewise may be tied directly to REN_1 or REN_2, in order to prevent overrunning or underrunning the internal FIFO boundaries. (See Figure 10.)

PIN CONNECTIONS

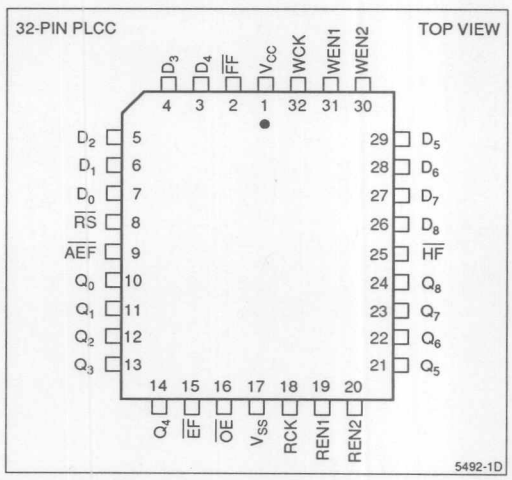


Figure 1. Pin Connections for PLCC Package

FUNCTIONAL DESCRIPTION (cont'd)

Alternatively, the enabling of write or read operations may be controlled entirely by external system logic, while the flags serve strictly as system interrupts. This design approach works well when the input port clock and the output port clock are not synchronized to each other.

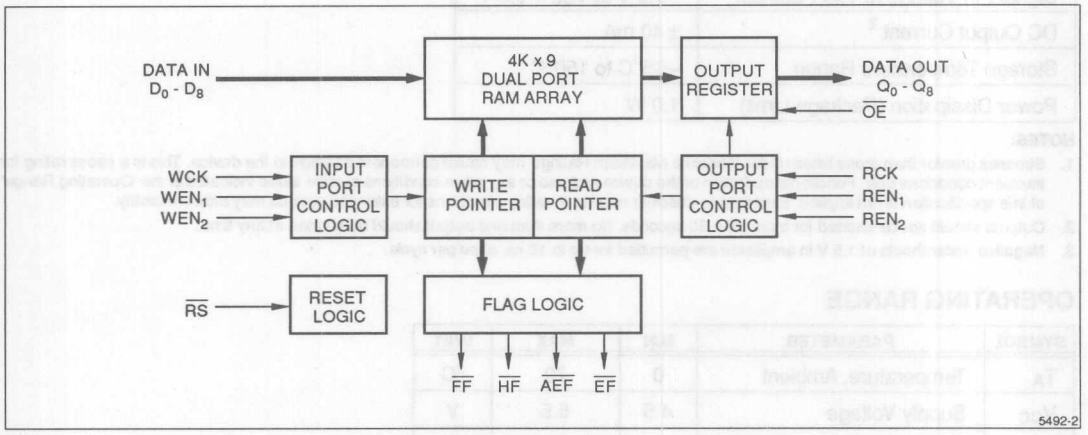


Figure 2. LH5492 Block Diagram

SIGNAL/PIN DESCRIPTIONS

PIN	SIGNAL NAME/DESCRIPTION
$\overline{RS}$	Reset. An assertive-LOW input which initializes the internal address pointers and flags.
WCK	Write Clock. A free-running clock input for write operations.
RCK	Read Clock. A free-running clock input for read operations.
$D_0 - D_8$	Data Inputs. $D_0 - D_8$ are sampled on the rising edge of WCK, whenever both WEN_1 and WEN_2 are being asserted.
$Q_0 - Q_8$	Data Outputs. $Q_0 - Q_8$ are updated following the rising edge of RCK, whenever both REN_1 and REN_2 are being asserted.
WEN_1	Write Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
WEN_2	Write Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
REN_1	Read Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both REN_1 and REN_2 must be asserted in order to enable a read operation.
REN_2	Read Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both REN_1 and REN_2 must be asserted in order to enable a read operation.
$\overline{FF}$	Full Flag. An assertive-LOW output indicating when the FIFO is full.
$\overline{HF}$	Half-Full Flag. An assertive-LOW output indicating when the FIFO is more than half full.
$\overline{AEF}$	Almost-Empty/Full. An assertive-LOW output indicating when the FIFO either is within eight locations of full, or else is within eight locations of empty.
$\overline{EF}$	Empty Flag. An assertive-LOW output indicating when the FIFO is empty.
$\overline{OE}$	Output Enable. An assertive-LOW signal which, when asserted, places the data outputs $Q_0 - Q_8$ in a low-impedance state.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential[3]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−10	10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at f_C = max		150	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		25	mA

NOTE:

1. I_{CC} and I_{CC2} are dependent upon actual output loading and cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1. 5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

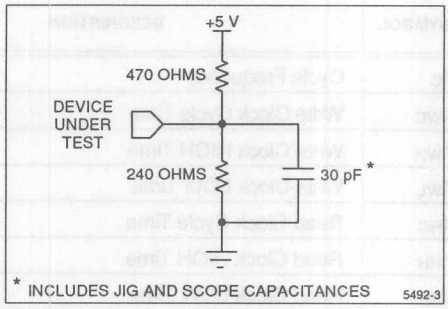


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_O (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DESCRIPTION	-25		-30		-35		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_C	Cycle Frequency	–	40	–	33.3	–	28.5	MHz
t_{WC}	Write Clock Cycle Time	25	–	30	–	35	–	ns
t_{WH}	Write Clock HIGH Time	10	–	12	–	14	–	ns
t_{WL}	Write Clock LOW Time	10	–	12	–	14	–	ns
t_{RC}	Read Clock Cycle Time	25	–	30	–	35	–	ns
t_{RH}	Read Clock HIGH Time	10	–	12	–	14	–	ns
t_{RL}	Read Clock LOW Time	10	–	12	–	14	–	ns
t_{DS}	Data Setup Time to Rising Clock	10	–	10	–	10	–	ns
t_{DH}	Data Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_{ES}	Enable Setup Time to Rising Clock	10	–	10	–	10	–	ns
t_{EH}	Enable Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_A	Data Output Access Time	–	20	–	22	–	25	ns
t_{OH}	Output Hold Time from Rising RCK	5	–	5	–	5	–	ns
t_{QL}	$\overline{OE}$ to Data Outputs Low-Z [2]	1	–	1	–	1	–	ns
t_{QZ}	$\overline{OE}$ to Data Outputs High-Z [2]	–	10	–	11	–	12	ns
t_{OE}	Output Enable to Data Valid	–	10	–	11	–	12	ns
t_{EF}	Clock to Empty Flag Valid	–	20	–	22	–	25	ns
t_{FF}	Clock to Full Flag Valid	–	20	–	22	–	25	ns
t_{HF}	Clock to Half Flag Valid	–	35	–	37	–	40	ns
t_{AEF}	Clock to AEF Flag Valid	–	35	–	37	–	40	ns
t_{RS}	Reset Pulse Width	25	–	30	–	35	–	ns
t_{RSS}	Reset Setup Time [3]	10	–	12	–	15	–	ns
t_{RF}	Reset LOW to Flag Valid	–	30	–	32	–	35	ns
t_{RQ}	Reset to Data Outputs LOW	–	20	–	22	–	25	ns
t_{FRL}	First Read Latency [4]	18	–	19	–	20	–	ns
t_{FWL}	First Write Latency [5]	18	–	19	–	20	–	ns

NOTES:

1. All timing measurements performed at 'AC Test Condition' levels.
2. Value guaranteed by design; not currently production tested.
3. t_{RSS} need not be met *unless* either a rising edge of WCK occurs while WEN_1 and WEN_2 both are being asserted, or else a rising edge of RCK occurs while REN_1 and REN_2 both are being asserted.
4. t_{FRL} is the minimum first-write-to-first read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condition, which is required to assure successful writing of data.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous reset input ($\overline{RS}$) is asserted, i.e., taken to a LOW state. A reset operation is required after power up, before the first write operation occurs. The reset operation initializes both the read and write address pointers to the first physical memory location. After the falling edge of $\overline{RS}$, the status flags ($\overline{FF}$, $\overline{HF}$, $\overline{AEF}$, and $\overline{EF}$) are updated to indicate a valid empty condition.

Write and/or read operations need not be deactivated during a reset operation, but failure to do so requires observance of the Reset Setup Time (t_{RSS}) to assure that the first write and/or first read following reset will occur predictably.

If no read operations have been performed following a reset operation, then the 'previous data' word being held in the output register consists of all zeroes. This data word is seen on the output bus ($Q_0 - Q_8$) whenever the output enable ($\overline{OE}$) is being held LOW.

Write

A write operation consists of storing parallel data from the data inputs to the FIFO memory array. A write operation is initiated on the rising edge of the Write Clock input (WCK), whenever both of the edge-sampled Write Enable inputs (WEN_1 and WEN_2) are held HIGH for the prescribed setup times and hold times. Setup times and hold times must also be observed for the Data In pins (D_0–D_8).

When a full condition is reached, write operations should be ceased, in order to prevent overwriting unread data. The state of the four status flags has no direct effect on write operations; that is, the execution of write operations is gated only by WEN_1 and WEN_2, and the internal logic of the LH5492 itself has no interlock to prevent overrunning valid data after the internal write pointer 'wraps around' and catches up to the read pointer – and passes it, if writing is continued. Figure 10 illustrates how such an interlock may be implemented by means of external connections.

Following the first read operation from a full FIFO, another memory location becomes freed up, and the Full Flag is deasserted ($\overline{FF}$ = HIGH). The next write operation should begin no earlier than a First Write Latency time (t_{FWL}) after the first read operation from a full FIFO, in order to assure that a correct data word is written into the FIFO memory.

Read

A read operation consists of loading parallel data from the FIFO memory array to the output register. A read operation is initiated on the rising edge of the Read Clock input (RCK), whenever both of the edge-sampled Read Enable inputs (REN_1 and REN_2) are held HIGH for the prescribed setup times and hold times. Read data becomes valid on the Data Out pins ($Q_0 - Q_8$) by a time t_A after the rising edge of RCK, provided that the Output Enable ($\overline{OE}$) is being held LOW. $\overline{OE}$ is an assertive-LOW asynchronous input. When $\overline{OE}$ is taken LOW, the $Q_0 - Q_8$ outputs are driven (i.e., are in a low-Z state) within a minimum time t_{OL}. When $\overline{OE}$ is taken HIGH, the $Q_0 - Q_8$ outputs are in a high-Z state within a maximum time t_{OZ}.

When an empty condition is reached, read operations should be ceased, until a valid write operation(s) has loaded additional data into the FIFO. The state of the four status flags has no direct effect on read operations; that is, the execution of read operations is gated only by REN_1 and REN_2, and the internal logic of the LH5492 itself has no interlock to prevent underrunning valid data after the internal read pointer 'wraps around' and catches up to the write pointer – and passes it, if reading is continued. Figure 10 illustrates how such an interlock may be implemented by means of external connections.

Following the first write to an empty FIFO, the Empty Flag ($\overline{EF}$) is deasserted ($\overline{EF}$ = HIGH). The next read operation should begin no earlier than a First Read Latency time (t_{FRL}) from the first write operation into an empty FIFO, in order to ensure that correct read data is retrieved.

Status Flags

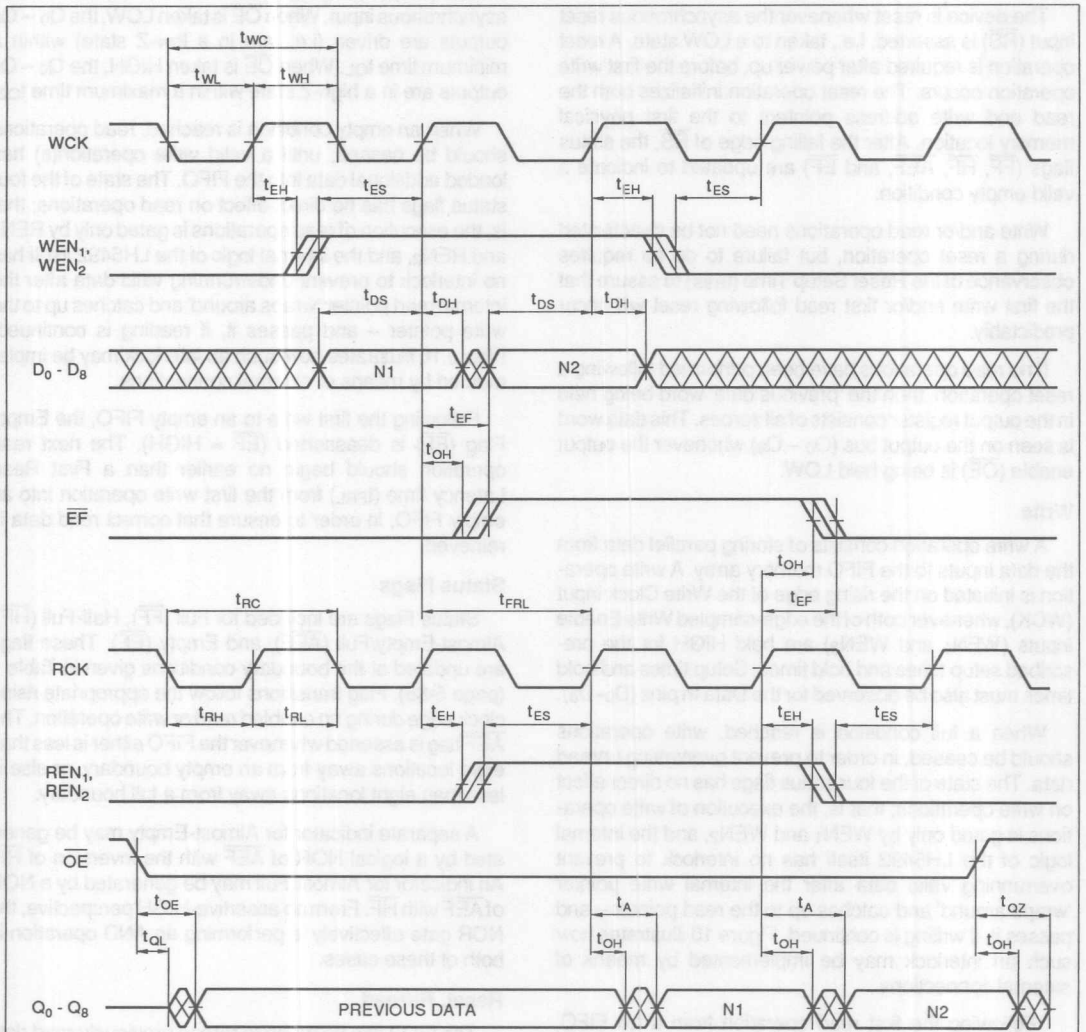
Status Flags are included for Full ($\overline{FF}$), Half-Full ($\overline{HF}$), Almost-Empty/Full ($\overline{AEF}$), and Empty ($\overline{EF}$). These flags are updated at the boundary conditions given in Table 1 (page 5-85). Flag transitions follow the appropriate rising clock edge during an enabled read or write operation. The $\overline{AEF}$ flag is asserted whenever the FIFO either is less than eight locations away from an empty boundary, or else is less than eight locations away from a full boundary.

A separate indicator for Almost-Empty may be generated by a logical NOR of $\overline{AEF}$ with the inversion of $\overline{HF}$. An indicator for Almost-Full may be generated by a NOR of $\overline{AEF}$ with $\overline{HF}$. From an assertive-HIGH perspective, the NOR gate effectively is performing an AND operation in both of these cases.

Reset, Reread

The FIFO can be made to reread previously read data through a reset operation, which initializes the internal read-address and write-address pointers to the first physical location in the FIFO memory (location zero). The status flags are updated to indicate an empty condition; but up to 4096 data words which previously had been written into and/or read from the FIFO still then remain in the FIFO memory array. The status flags may be ignored, and data may be reaccessed by subsequent read operations. The First Read Latency (t_{FRL}) specification does not apply to reset/reread operations, since no new data words are being written to the FIFO following the reset operation.

TIMING DIAGRAMS



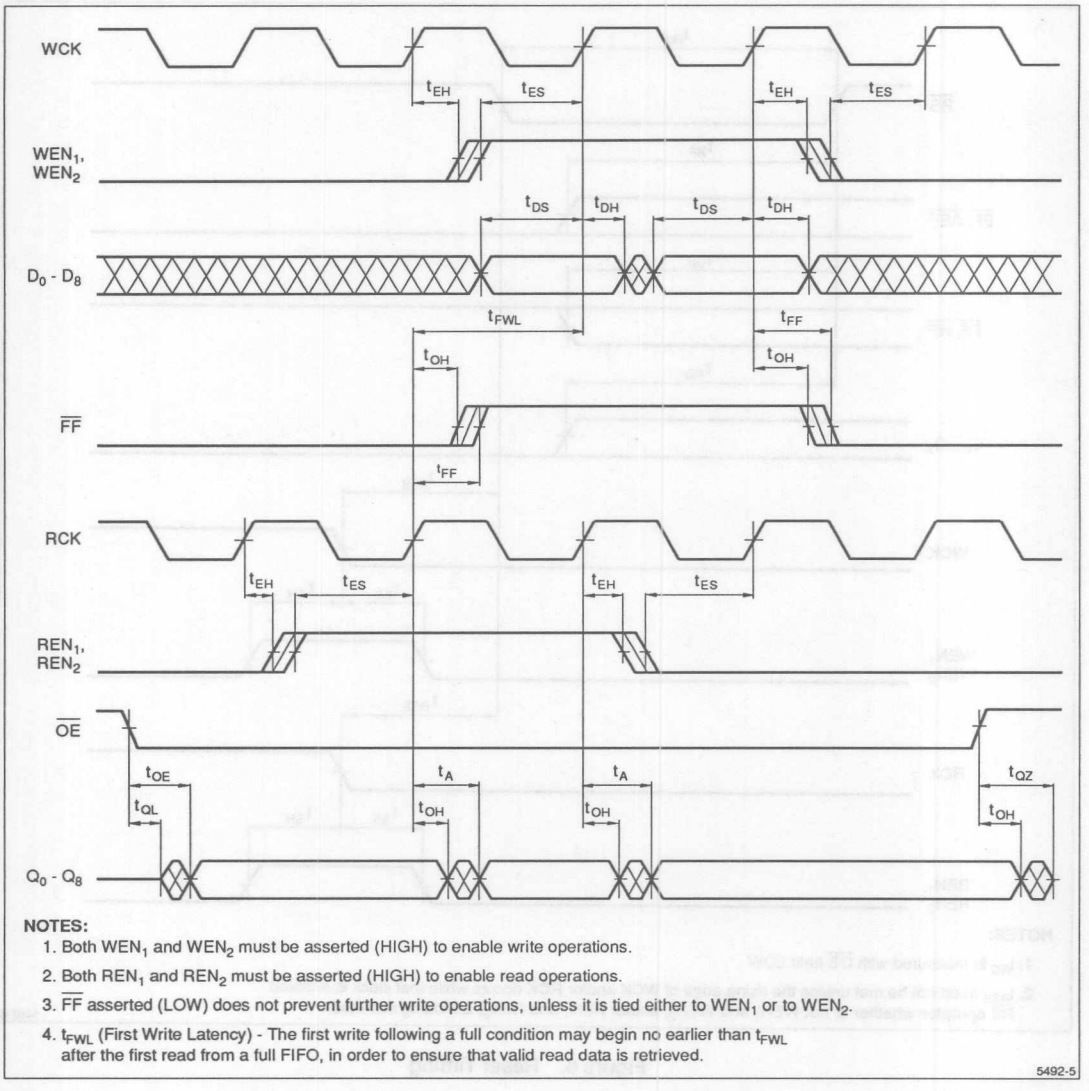
NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{EF}$ asserted (LOW) does not prevent further read operations, unless it is tied either to REN_1 or to REN_2.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to assure valid data is retrieved. This specification does not apply to reset/reread applications, in which the status of FIFO flags is ignored.
5. Immediately following a reset operation, the 'previous data' will be all bits LOW.

5492-4

Figure 4. Write and Read Operation in a Near-Empty Condition

TIMING DIAGRAMS (cont'd)



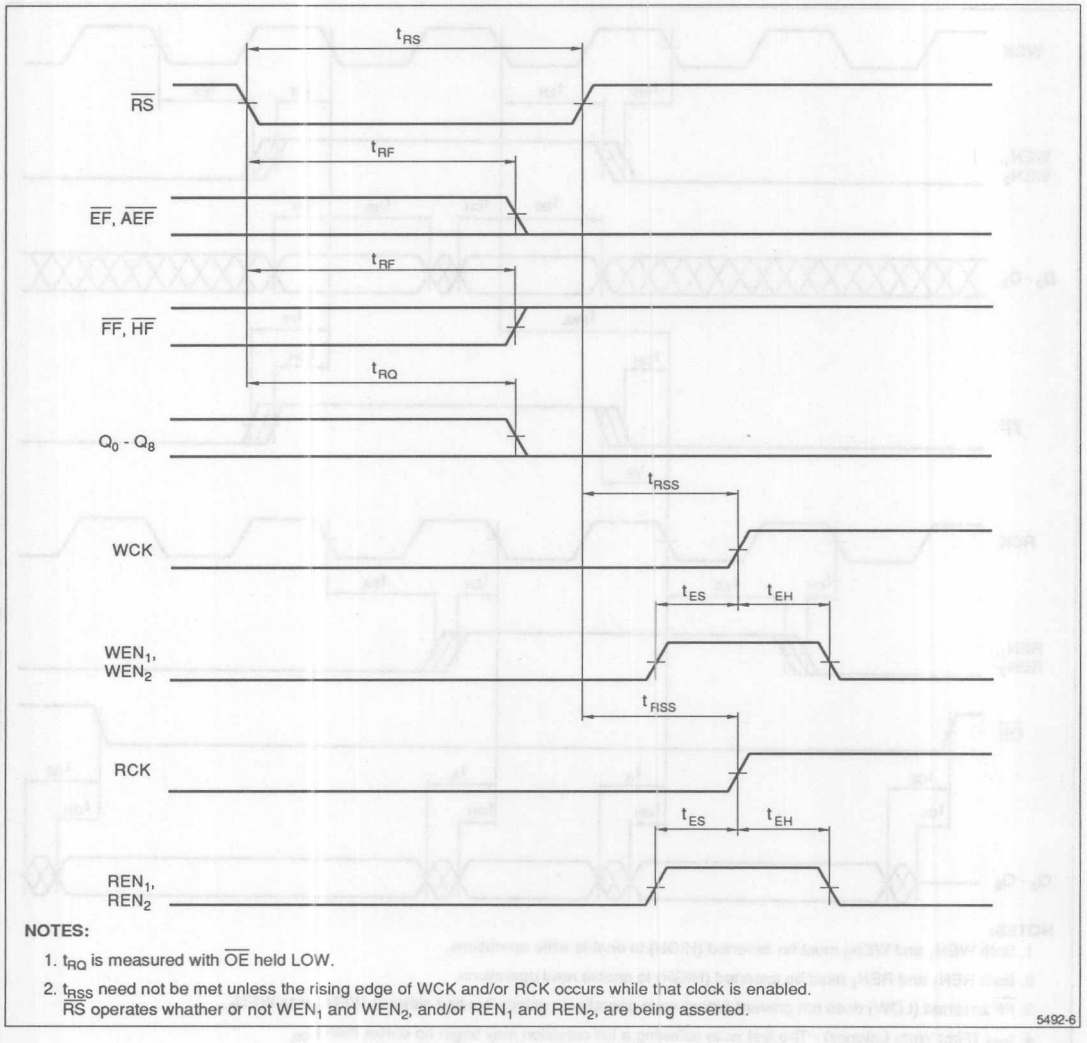
NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{FF}$ asserted (LOW) does not prevent further write operations, unless it is tied either to WEN_1 or to WEN_2.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, in order to ensure that valid read data is retrieved.

5492-5

Figure 5. Read and Write Operation in a Near-Full Condition

TIMING DIAGRAMS (cont'd)



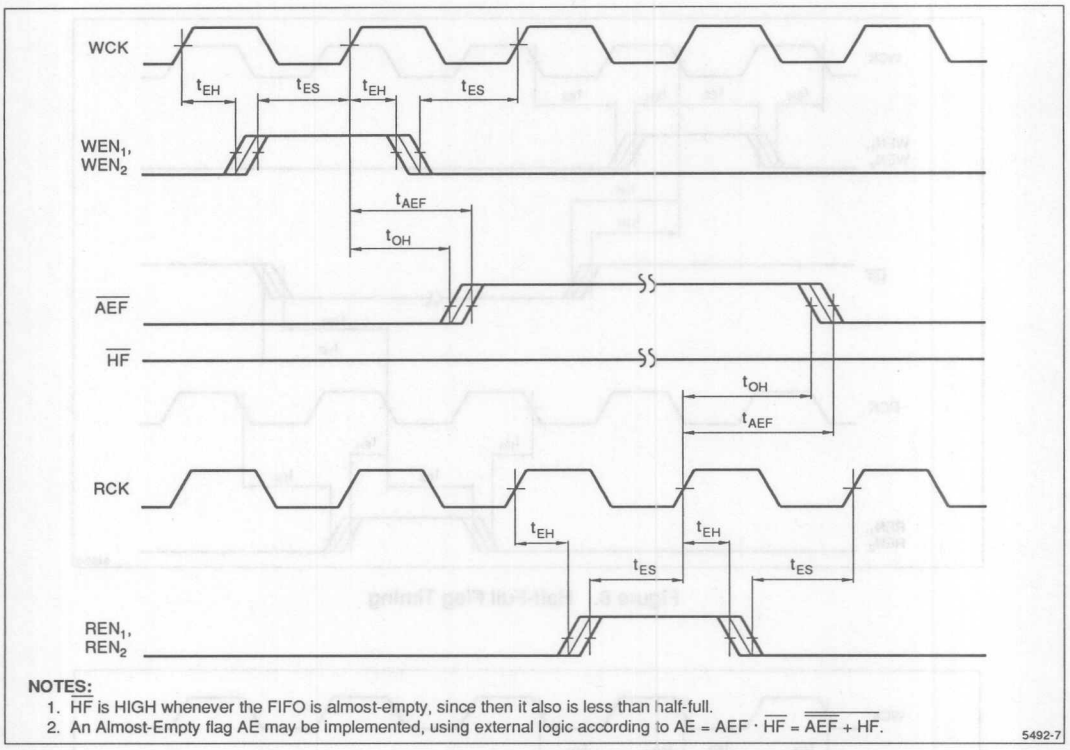
NOTES:

1. t_{RQ} is measured with $\overline{OE}$ held LOW.
2. t_{RSS} need not be met unless the rising edge of WCK and/or RCK occurs while that clock is enabled. $\overline{RS}$ operates whether or not WEN_1 and WEN_2, and/or REN_1 and REN_2, are being asserted.

5492-6

Figure 6. Reset Timing

TIMING DIAGRAMS (cont'd)



NOTES:
1. $\overline{HF}$ is HIGH whenever the FIFO is almost-empty, since then it also is less than half-full.
2. An Almost-Empty flag AE may be implemented, using external logic according to $AE = AEF \cdot \overline{HF} = \overline{\overline{AEF} + HF}$.

5492-7

Figure 7. Almost-Empty Flag Timing

Table 1. Flag Definitions

FLAG STATUS				VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
$\overline{EF}$	AEF	$\overline{HF}$	$\overline{FF}$	min	max	min	max
0	0	1	1	4096	4096	0	0
1	0	1	1	4089	4095	1	7
1	1	1	1	2048	4088	8	2047
1	1	0	1	8	2047	2048	4088
1	0	0	1	1	7	4089	4095
1	0	0	0	0	0	4096	4096

TIMING DIAGRAMS (cont'd)

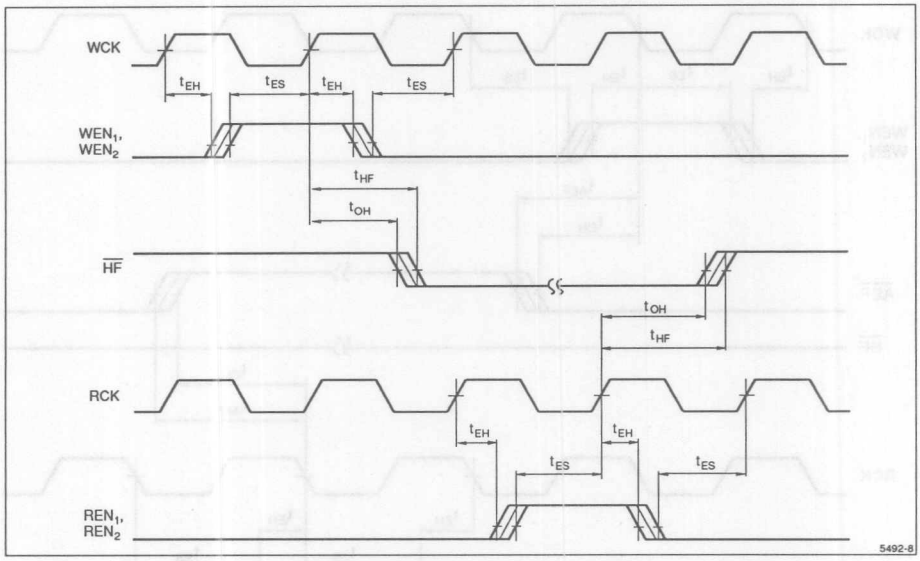
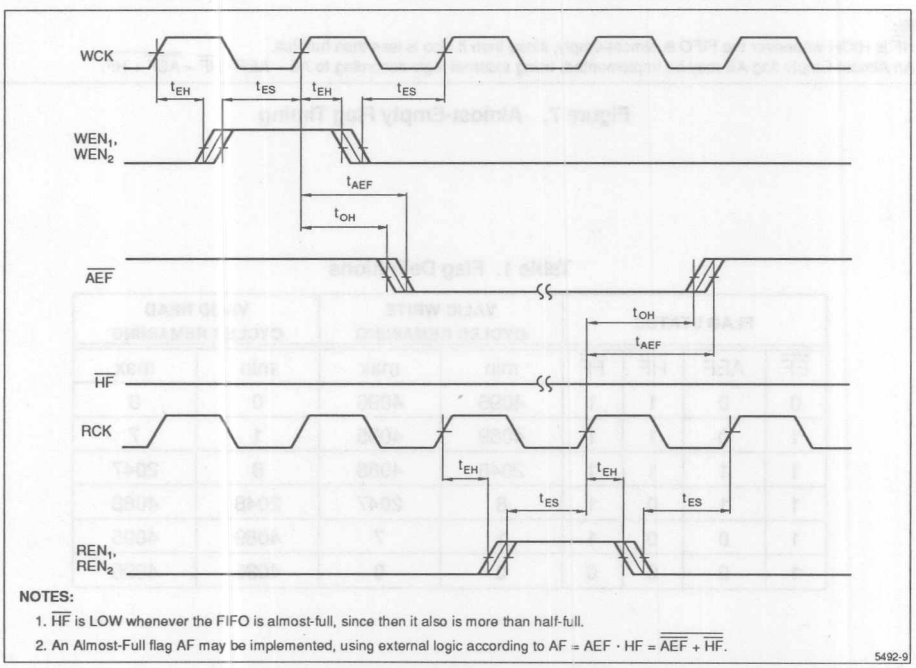


Figure 8. Half-Full Flag Timing



NOTES:

1. $\overline{HF}$ is LOW whenever the FIFO is almost-full, since then it also is more than half-full.
2. An Almost-Full flag AF may be implemented, using external logic according to AF = AEF · HF = $\overline{\overline{AEF} + \overline{HF}}$.

Figure 9. Almost-Full Flag Timing

OPERATIONAL MODES

Synchronous Read and Write Operations

Read and Write operations may be performed in synchronism with each other by deriving WCK and RCK from a *common* system clock. In this case, the Write Enable (WEN_1 and WEN_2) and Read Enable (REN_1 and REN_2) inputs all get sampled at the same clock rising edge.

This type of synchronous read/write operation ensures that flag outputs always satisfy the required setup and hold times for the WEN_1, WEN_2, REN_1, and REN_2 inputs. Thus, the Full Flag output ($\overline{FF}$) may be tied directly to either WEN_1 or WEN_2, to prevent 'overrun' write operations when the full condition is reached, while the other Write Enable input remains available for system control. Likewise, the Empty Flag output ($\overline{EF}$) may be tied directly to either REN_1 or REN_2, to prevent 'underrun' read operations when the empty condition is reached, while the other Read Enable input remains available for system control.

Asynchronous Read and Write Operations

Write operations and read operations also may be performed completely asynchronously, relative to each other, when the WCK input and the RCK input are derived from the clock signals of *different* systems. Under these conditions, status-flag transitions occur relative to two unpredictably-related clock edges. Therefore, these flags should not be used to drive Write Enable or Read Enable inputs directly, since they do not always satisfy valid setup times and hold times.

Instead, it is recommended that these enable signals be *controlled* by the user, in order to ensure that adequate setup times and hold times are maintained. If the FIFO becomes either completely full or completely empty, then some synchronization between read and write operations at the full or empty boundaries becomes necessary to prevent timing violations.

When the FIFO is operating in this manner, the Almost-Empty/Full flag and the Half-Full flag should be used to provide some advance warning, to avoid overrunning or underruning a FIFO internal boundary. Typically, these flags are used as system interrupts. When an interrupt is received by the faster of the two systems, a predefined block of data then may be transferred at the maximum data rate, as long as there is known to be sufficient room for it. In this way the full and empty boundaries are never reached, and yet maximum data throughput is maintained.

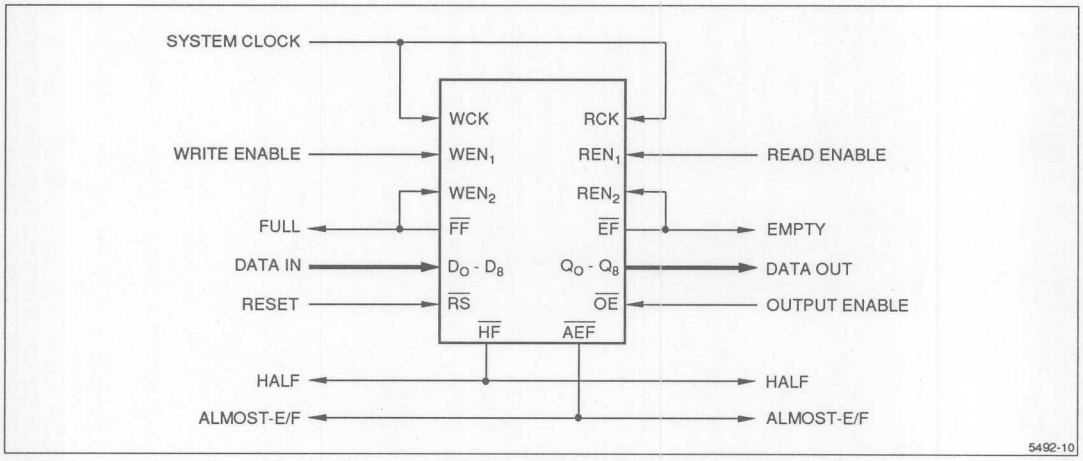


Figure 10. Synchronous Operation

OPERATIONAL MODES (cont'd)

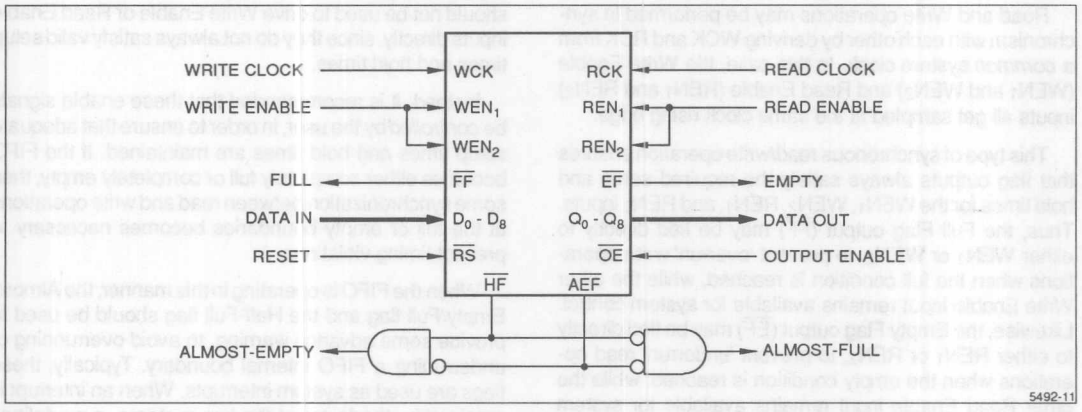


Figure 11. Asynchronous Operation

OPERATIONAL MODES (cont'd)

Depth Expansion

Increased FIFO depth may be realized by using multiple LH5492 devices. The availability of two enable control inputs for each port assists in this expansion. For either the input port or the output port, one enable input may be used for system control, while the other is driven by decode logic to direct the flow of data. Typically, this decode logic alternates accesses sequentially from one device to the next. Status flags are then derived from the last device in the sequence. The simplest form of this decode logic consists of a single toggle flipflop, which alternates access between two devices for every enabled clock cycle as shown in Figure 13.

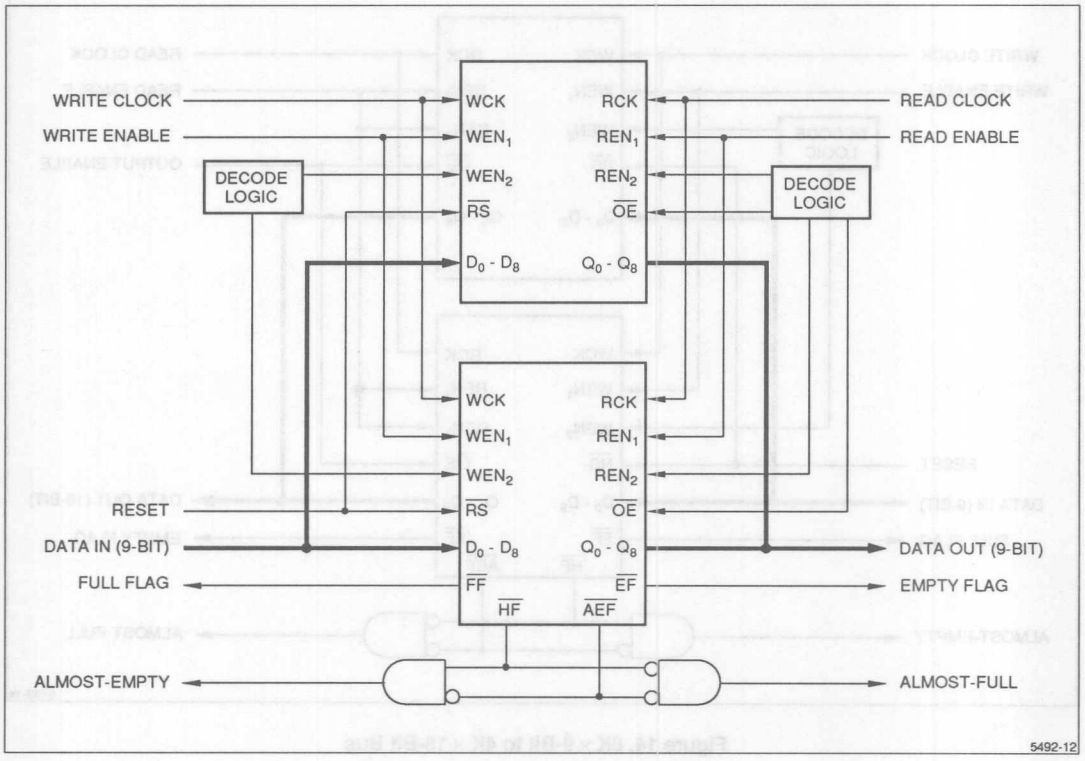


Figure 12. FIFO Depth Expansion (8192 × 9)

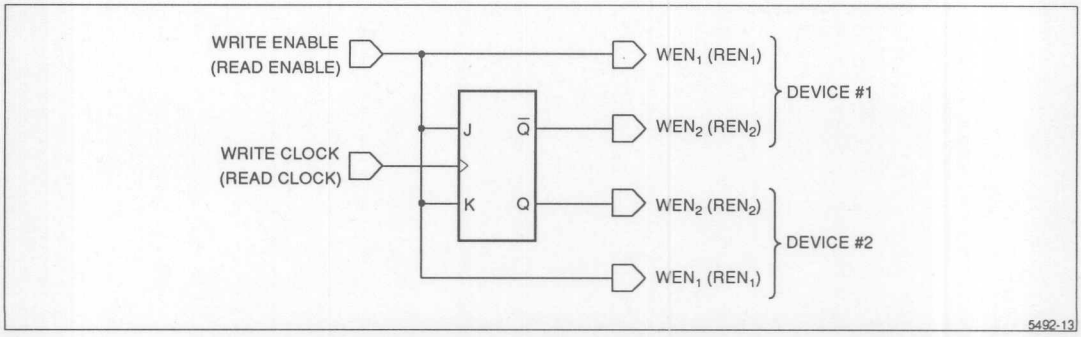


Figure 13. Simple Decode Logic

OPERATIONAL MODES (cont'd)

Interface Between Different Bus Widths

Applications which require interface between system buses of different word widths also may be implemented with multiple LH5492 devices. Essentially, one port may be configured for greater FIFO depth, while the other port is configured for greater word width. Referring to Figures 14 and 15, the wide-word port accesses data simultaneously from multiple devices, while the narrow-word port uses decode logic to direct the flow of data between two or more devices.

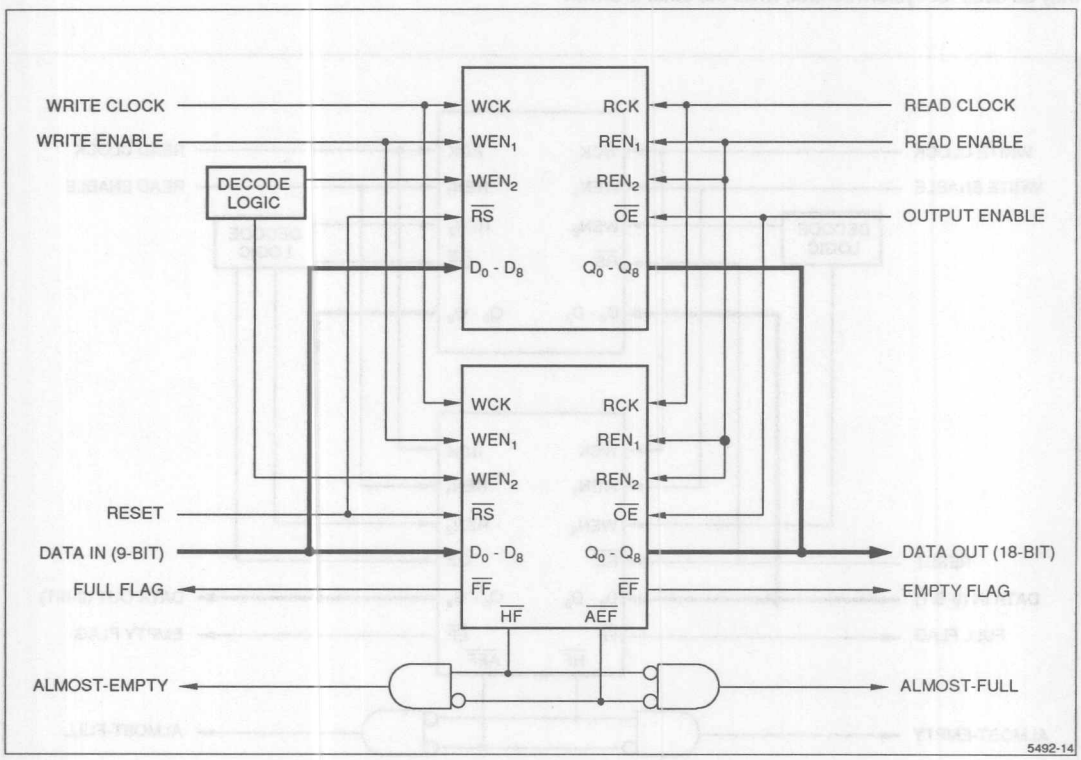


Figure 14. 8K × 9-Bit to 4K × 18-Bit Bus

OPERATIONAL MODES (cont'd)

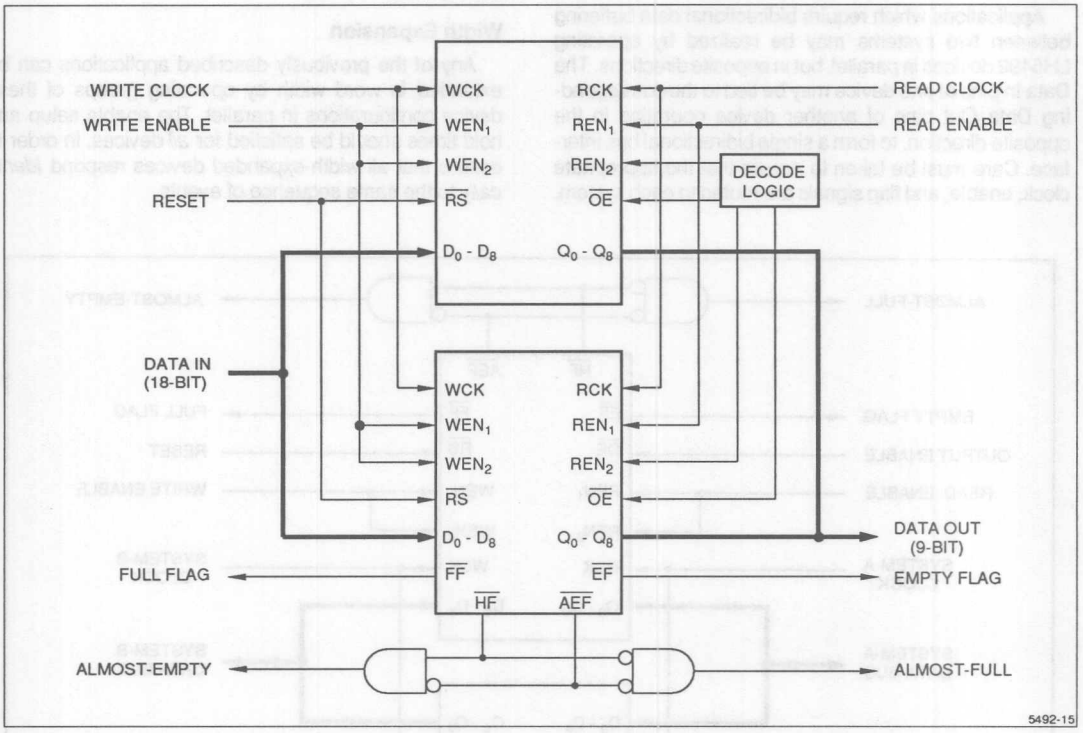


Figure 15. 4K × 18-Bit to 8K × 9-Bit Bus

OPERATIONAL MODES (cont'd)

Bidirectional Operation

Applications which require bidirectional data buffering between two systems may be realized by operating LH5492 devices in parallel, but in opposite directions. The Data In pins of one device may be tied to the corresponding Data Out pins of another device operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate clock, enable, and flag signals are routed to each system. The extra enable control signals may be used to extend FIFO depth, or to interface bidirectional buses of different word widths.

Width Expansion

Any of the previously described applications can be extended in word width by operating groups of these device configurations in parallel. The enable setup and hold times should be satisfied for *all* devices, in order to ensure that all width-expanded devices respond *identically* to the same sequence of events.

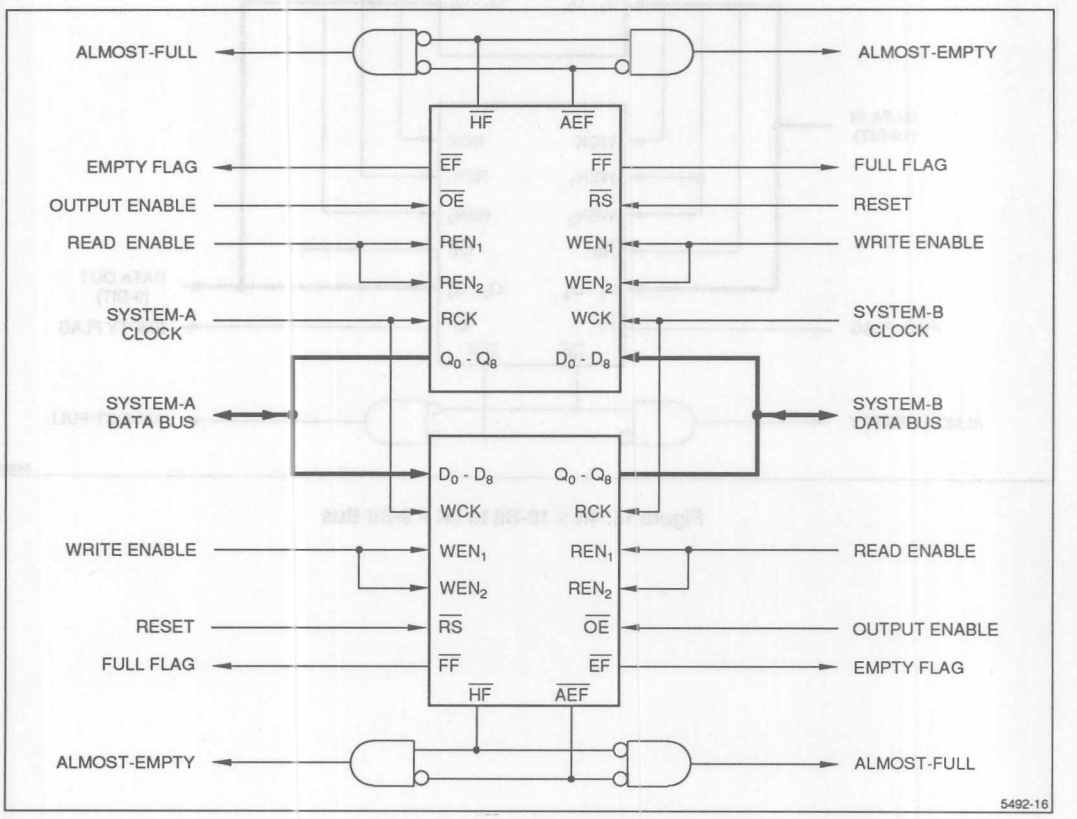
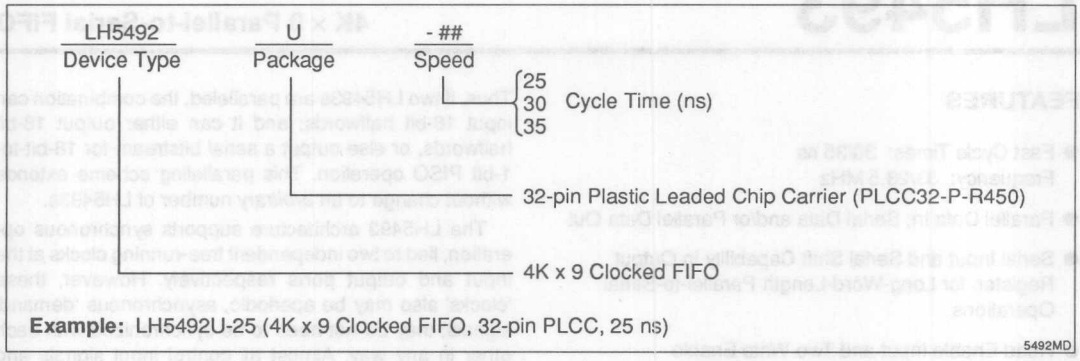


Figure 16. Bidirectional Operation

ORDERING INFORMATION



LH5493

4K × 9 Parallel-to-Serial FIFO

FEATURES

- Fast Cycle Times: 30/35 ns
  Frequency: 33/28.5 MHz
- Parallel Data In; Serial Data and/or Parallel Data Out
- Serial Input and Serial Shift Capability in Output Register, for Long-Word-Length Parallel-to-Serial Operations
- Read Enable Input and Two Write Enable Inputs, Sampled on Rising Edge of the Appropriate Clock
- Fast-Fall-Through Time Internal Architecture Based on CMOS Dual-Port SRAM Technology, 4096 × 9
- Fully Asynchronous Read and Write Operations
- Full, Half-Full, Almost-Empty/Full, and Empty Flags
- Reset/Reread Capability
- TTL/CMOS-Compatible I/O
- 32-Pin PLCC Package

FUNCTIONAL DESCRIPTION

The LH5493 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS RAM technology, capable of containing up to 4096 nine-bit words. One LH5493 FIFO can input nine-bit bytes; and it can either output nine-bit bytes in parallel, or else output a serial bitstream. Thus, a single LH5493 is capable of nine-bit-to-one-bit PISO (Parallel-In, Serial-Out) operation.

An LH5493 has one 9-bit parallel input (write) port, and one nine-bit parallel output (read) port. And there is one one-bit serial input, which supports paralleling LH5493s for greater-word-width PISO operation. This serial input also allows additional control bits to be inserted at will into the serial output bitstream. There is no serial output port as such; *any* individual bit position in the parallel output register may be chosen as the serial-output data path, according to the desired time phase of the output bitstream.

The LH5493 architecture supports a very convenient method of *paralleling* multiple FIFOs for PISO operation, without any additional logic being needed, in order to achieve a *wider* 'effective FIFO.' The paralleled LH5493 combination remains capable of performing all of the operations which a standalone LH5493 can perform. Thus, if two LH5493s are paralleled, the combination can input 18-bit halfwords; and it can either output 18-bit halfwords, or else output a serial bitstream for 18-bit-to-1-bit PISO operation. This paralleling scheme extends without change to an *arbitrary* number of LH5493s.

The LH5493 architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals; they do not need to be synchronized with each other in any way. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design. The input and output ports operate altogether independently of each other, except when the FIFO becomes either totally full or else totally empty.

Two edge-sampled enable control inputs, WEN_1 and WEN_2, are provided for the input port; and one such control input, REN, is provided for the output port. These synchronous control inputs may be used as write demands and read demands respectively, when an LH5493 is interfaced to continuously-clocked synchronous systems. Data flow is initiated at a port by the rising edge of the clock signal corresponding to that port, and is gated only by the appropriate edge-sampled enable control input signal(s).

PIN CONNECTIONS

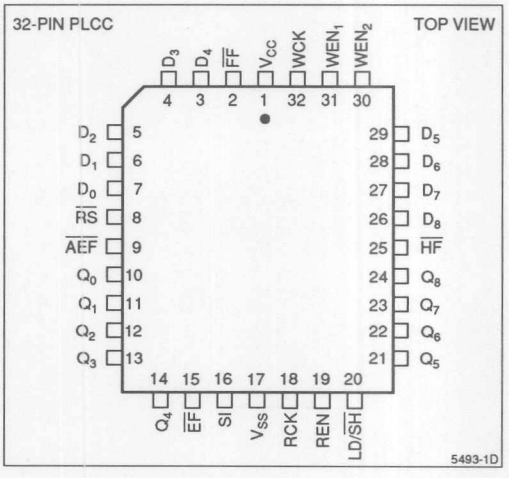


Figure 1. Pin Connections for PLCC Package

FUNCTIONAL DESCRIPTION (cont'd)

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Half-Full, Almost-Empty/Full, and Empty. The Almost-Empty/Full flag is asserted whenever the internal memory is either within eight locations of 'empty,' or else within eight locations of 'full.' The Half-Full flag serves to distinguish the 'almost-empty' condition from the 'almost-full' condition. Also, during fully-synchronous operation, the Full flag may be tied directly to WEN_1 or to WEN_2, and the Empty flag likewise may be tied directly to REN, in order to prevent overrunning or underrunning the internal FIFO boundaries. (See Figure 11.)

Alternatively, the enabling of write or read operations may be controlled entirely by external system logic, while the flags serve strictly as system interrupts. This design approach works well when the input port clock and the output port clock are not synchronized to each other.

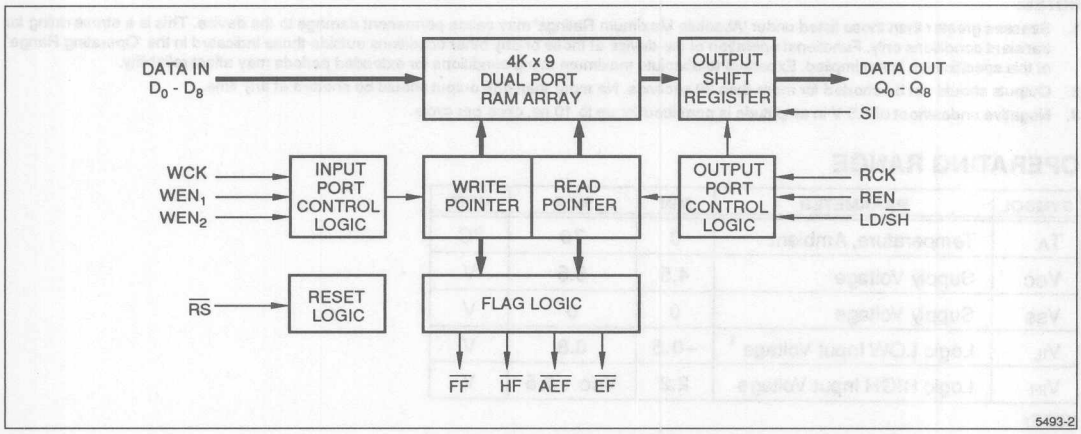


Figure 2. LH5493 Block Diagram

SIGNAL PIN DESCRIPTIONS

PIN	SIGNAL NAME/DESCRIPTION
$\overline{RS}$	Reset. An assertive-LOW input which initializes the internal address pointers and flags.
WCK	Write Clock. A free-running clock input for write operations.
RCK	Read Clock. A free-running clock input for read operations.
SI	Serial Input. A serial data input to allow paralleled PISO operation of multiple devices.
$D_0 - D_8$	Data Inputs. $D_0 - D_8$ are sampled on the rising edge of WCK, whenever both WEN_1 and WEN_2 are being asserted..
$Q_0 - Q_8$	Data Outputs. $Q_0 - Q_8$ are updated following the rising edge of RCK, whenever REN is being asserted.
WEN_1	Write Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
WEN_2	Write Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO. Both WEN_1 and WEN_2 must be asserted in order to enable a write operation.
REN	Read Enable. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO.
LD/$\overline{SH}$	Read Load/Shift. An input signal which is sampled on the rising edge of RCK to control the loading or shifting of data in the output register.
$\overline{FF}$	Full Flag. An assertive-LOW output indicating when the FIFO is full.
$\overline{HF}$	Half-Full Flag. An assertive-LOW output indicating when the FIFO is more than half full.
$\overline{AEF}$	Almost-Empty/Full. An assertive-LOW output indicating when the FIFO either is within eight locations of full, or else is within eight locations of empty.
$\overline{EF}$	Empty Flag. An assertive-LOW output indicating when the FIFO is empty.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential[3]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at f_C = max		150	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		25	mA

NOTE:

1. I_{CC} and I_{CC2} are dependent upon actual output loading and cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

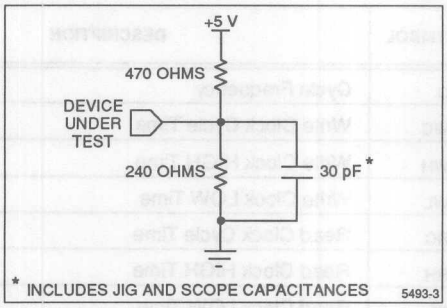


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	7 pF
C_O (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DESCRIPTION	-25		-30		-35		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_C	Cycle Frequency	–	40	–	33.3	–	28.5	MHz
t_{WC}	Write Clock Cycle Time	25	–	30	–	35	–	ns
t_{WH}	Write Clock HIGH Time	10	–	12	–	14	–	ns
t_{WL}	Write Clock LOW Time	10	–	12	–	14	–	ns
t_{RC}	Read Clock Cycle Time	25	–	30	–	35	–	ns
t_{RH}	Read Clock HIGH Time	10	–	12	–	14	–	ns
t_{RL}	Read Clock LOW Time	10	–	12	–	14	–	ns
t_{DS}	Data Setup Time to Rising Clock	10	–	10	–	10	–	ns
t_{DH}	Data Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_{ES}	Enable Setup Time to Rising Clock	10	–	10	–	10	–	ns
t_{EH}	Enable Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_A	Data Output Access Time	–	20	–	22	–	25	ns
t_{OH}	Output Hold Time from Rising RCK	5	–	5	–	5	–	ns
t_{EF}	Clock to Empty Flag Valid	–	20	–	22	–	25	ns
t_{FF}	Clock to Full Flag Valid	–	20	–	22	–	25	ns
t_{HF}	Clock to Half-Full Flag Valid	–	35	–	37	–	40	ns
t_{AEF}	Clock to AEF Flag Valid	–	35	–	37	–	40	ns
t_{RS}	Reset Pulse Width	25	–	30	–	35	–	ns
t_{RSS}	Reset Setup Time [3]	10	–	12	–	15	–	ns
t_{RF}	Reset LOW to Flag Valid	–	30	–	32	–	35	ns
t_{RQ}	Reset to Data Outputs LOW	–	20	–	22	–	25	ns
t_{FRL}	First Read Latency [4]	18	–	19	–	20	–	ns
t_{FWL}	First Write Latency [5]	18	–	19	–	20	–	ns

NOTES:

1. All timing measurements performed at 'AC Test Condition' levels.
2. Value guaranteed by design; not currently production tested.
3. t_{RSS} need not be met *unless* either a rising edge of WCK occurs while WEN_1 and WEN_2 both are being asserted, or else a rising edge of RCK occurs while REN is being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condtion, which is required to assure successful write.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous reset input ($\overline{RS}$) is asserted, i.e., taken to a LOW state. A reset operation is required after power up, before the first write operation occurs. The reset operation initializes both the read and write address pointers to the first physical memory location. After the falling edge of $\overline{RS}$, the status flags ($\overline{FF}$, $\overline{HF}$, $\overline{AEF}$, and $\overline{EF}$) are updated to indicate a valid empty condition.

Read, shift, and/or write operations need not be deactivated during a reset operation. However, failure to do so requires observance of the Reset Setup Time (t_{RSS}), to assure that the first write and/or first read following a reset operation will occur predictably.

If no read operations have been performed following a reset operation, then the 'previous data' word being held in the output register and seen on the output bus ($Q_0 - Q_8$) consists of all zeroes.

Write

A write operation consists of storing parallel data from the data inputs to the FIFO memory array. A write operation is initiated on the rising edge of the Write Clock input (WCK), whenever both of the edge-sampled Write Enable inputs (WEN_1 and WEN_2) are held HIGH for the prescribed setup times and hold times. Setup times and hold times must also be observed for the Data In inputs ($D_0 - D_8$).

When a full condition is reached, write operations should be ceased, in order to prevent overwriting unread data. The state of the status flags has no direct effect on write operations; that is, the execution of write operations is gated only by WEN_1 and WEN_2, and the internal logic of the LH5493 itself has no interlock to prevent overrunning valid data after the internal write pointer 'wraps around' and catches up to the read pointer – and passes it, if writing is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

Following the first read operation from a full FIFO, another memory location is freed up, and the Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency (t_{FWL}) after the first read operation from a full FIFO, in order to ensure that the write operation is successful.

Read

A read operation consists of loading parallel data from the FIFO memory array to the output register. A read operation is initiated on the rising edge of the Read Clock input (RCK), whenever both the edge-sampled Read Enable input (REN) and the Load/Shift input (LD/$\overline{SH}$) are held HIGH for the prescribed setup times and hold times. Read data becomes valid at the Data Out outputs ($Q_0 - Q_8$) by a time t_A after the rising edge of RCK. A shift of data in the output register is performed whenever REN is held HIGH and LD/$\overline{SH}$ is held LOW on the rising edge of RCK. Data is shifted in the MSB-to-LSB direction, with data from the Serial Input (SI) replacing the contents of bit position Q_8.

When an empty condition is reached, read operations should be ceased, until a valid write operation(s) has loaded additional data into the FIFO. The state of the four status flags has no direct effect on read or shift operations; that is, the execution of read or shift operations is gated only by REN and LD/$\overline{SH}$, and the internal logic of the LH5493 itself has no interlock to prevent underrunning valid data after the internal read pointer catches up to the write pointer – and passes it, if reading is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

When an empty condition is reached, shift operations may continue; but read operations should be ceased, until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the Empty Flag will be deasserted ($\overline{EF}$ = HIGH). The first read operation should begin no earlier than a First Read Latency time (t_{FRL}) from the first write to an empty FIFO, in order to ensure that correct read data is retrieved.

Status Flags

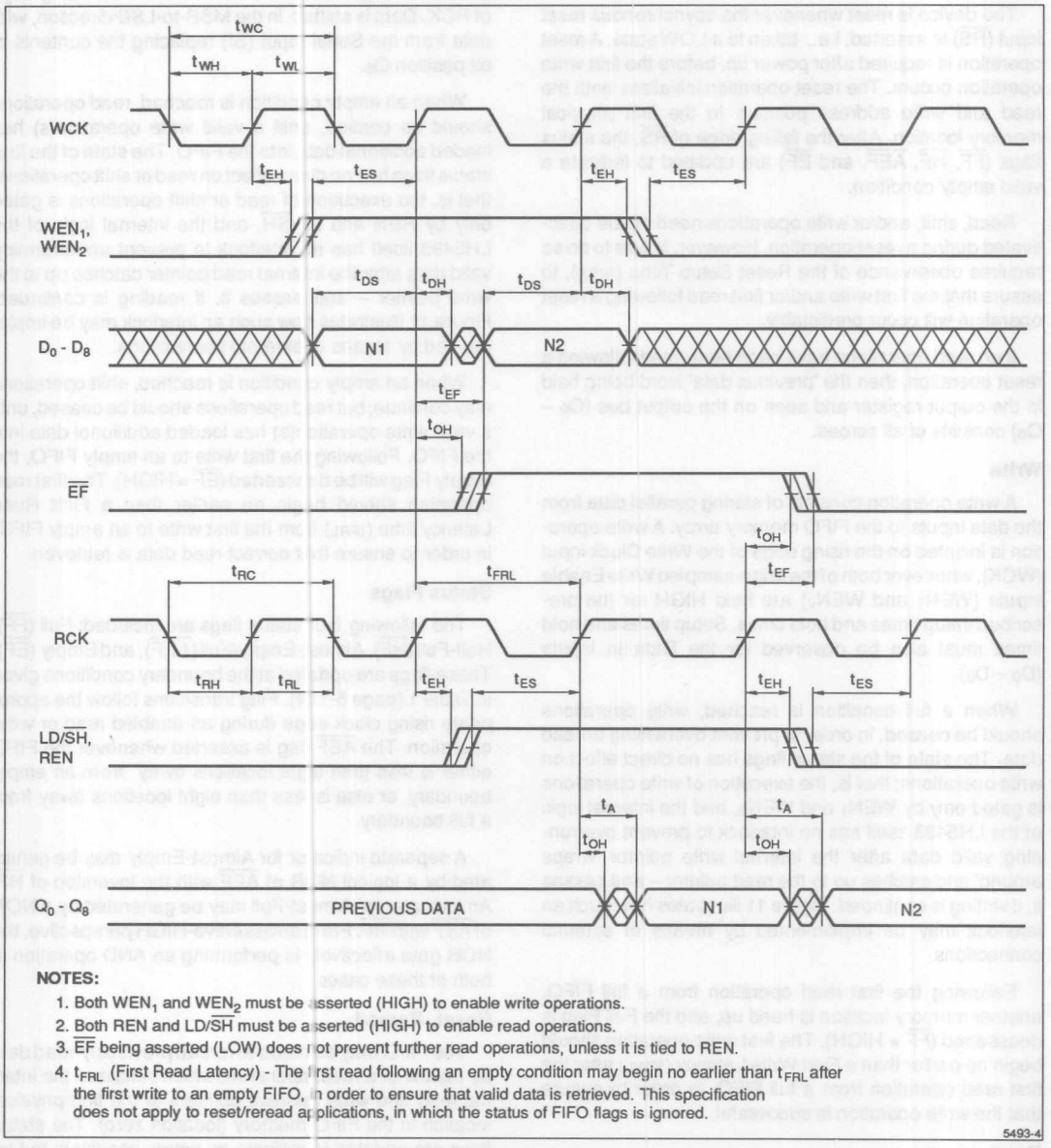
The following four status flags are included: Full ($\overline{FF}$), Half-Full ($\overline{HF}$), Almost-Empty/Full ($\overline{AEF}$), and Empty ($\overline{EF}$). These flags are updated at the boundary conditions given in Table 1 (page 5-104). Flag transitions follow the appropriate rising clock edge during an enabled read or write operation. The $\overline{AEF}$ flag is asserted whenever the FIFO either is less than eight locations away from an empty boundary, or else is less than eight locations away from a full boundary.

A separate indicator for Almost-Empty may be generated by a logical NOR of $\overline{AEF}$ with the inversion of $\overline{HF}$. An indicator for Almost-Full may be generated by a NOR of $\overline{AEF}$ with $\overline{HF}$. From an assertive-HIGH perspective, the NOR gate effectively is performing an AND operation in both of these cases.

Reset, Reread

The FIFO may be made to reread previously-read data by means of a reset operation, which initializes the internal read and write address pointers to the first physical location in the FIFO memory (location zero). The status flags are updated to indicate an empty condition; but up to 4096 words of old data, which previously had been written into and/or read from the FIFO, still remain in the memory array. The status flags may be ignored, and data may be reaccessed by subsequent read operations. The First Read Latency (t_{FRL}) specification does not apply to reset/reread operations, since no new data words are being written to the FIFO following the reset operation.

TIMING DIAGRAMS



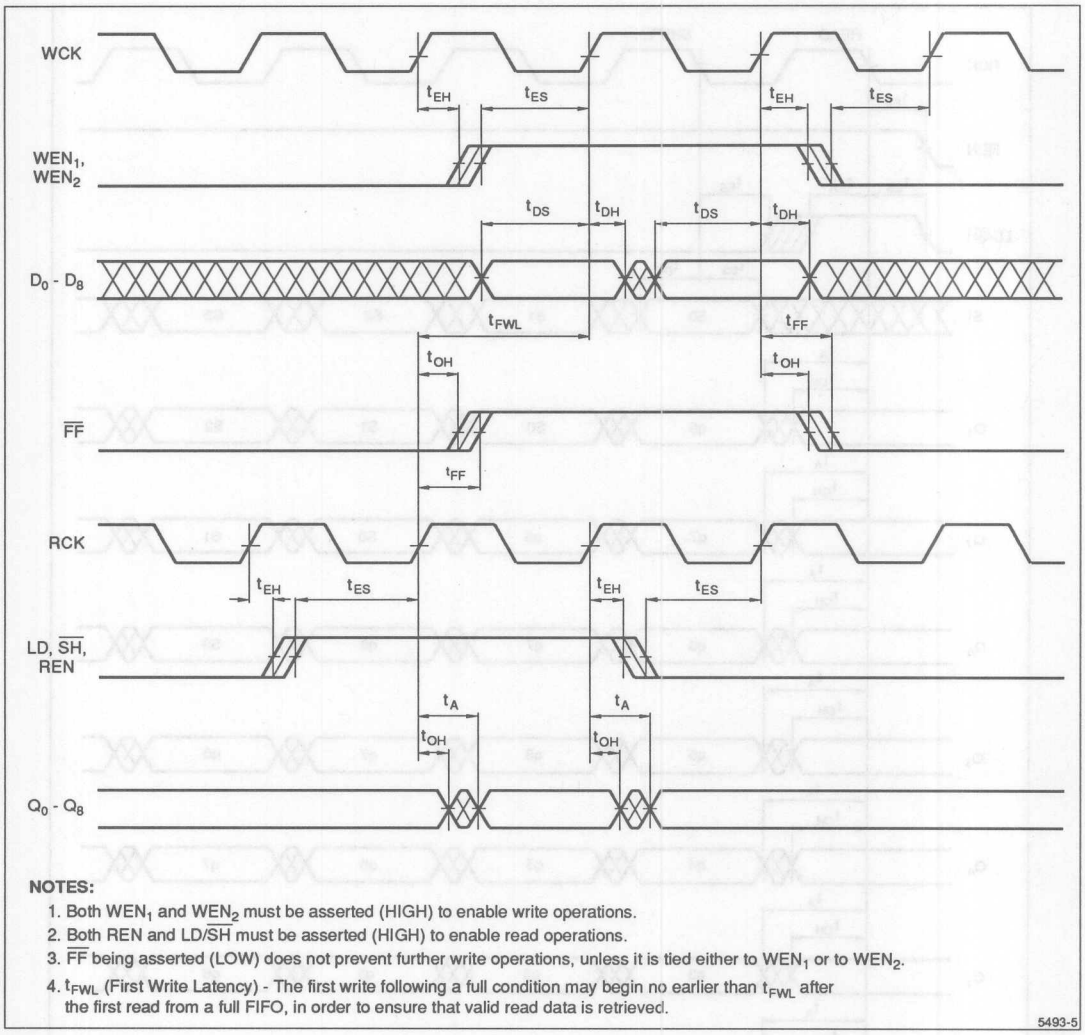
NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN and LD/$\overline{SH}$ must be asserted (HIGH) to enable read operations.
3. $\overline{EF}$ being asserted (LOW) does not prevent further read operations, unless it is tied to REN.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, in order to ensure that valid data is retrieved. This specification does not apply to reset/reread applications, in which the status of FIFO flags is ignored.

5493-4

Figure 4. Write and Read Operation in a Near-Empty Condition

TIMING DIAGRAMS (cont'd)



NOTES:

1. Both WEN_1 and WEN_2 must be asserted (HIGH) to enable write operations.
2. Both REN and LD/$\overline{SH}$ must be asserted (HIGH) to enable read operations.
3. $\overline{FF}$ being asserted (LOW) does not prevent further write operations, unless it is tied either to WEN_1 or to WEN_2.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, in order to ensure that valid read data is retrieved.

5493-5

Figure 5. Write and Read Operation in a Near-Full Condition

TIMING DIAGRAMS (cont'd)

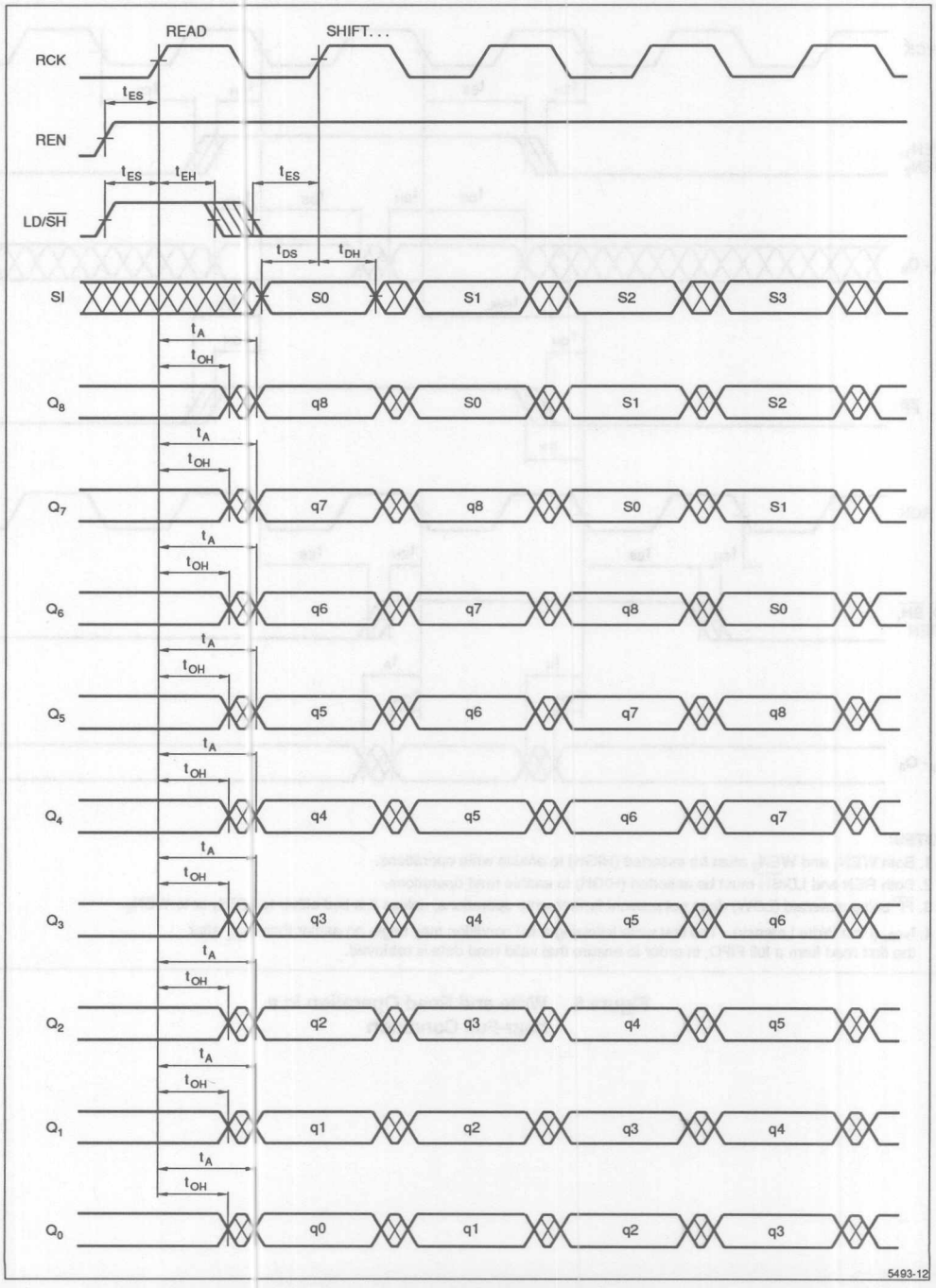
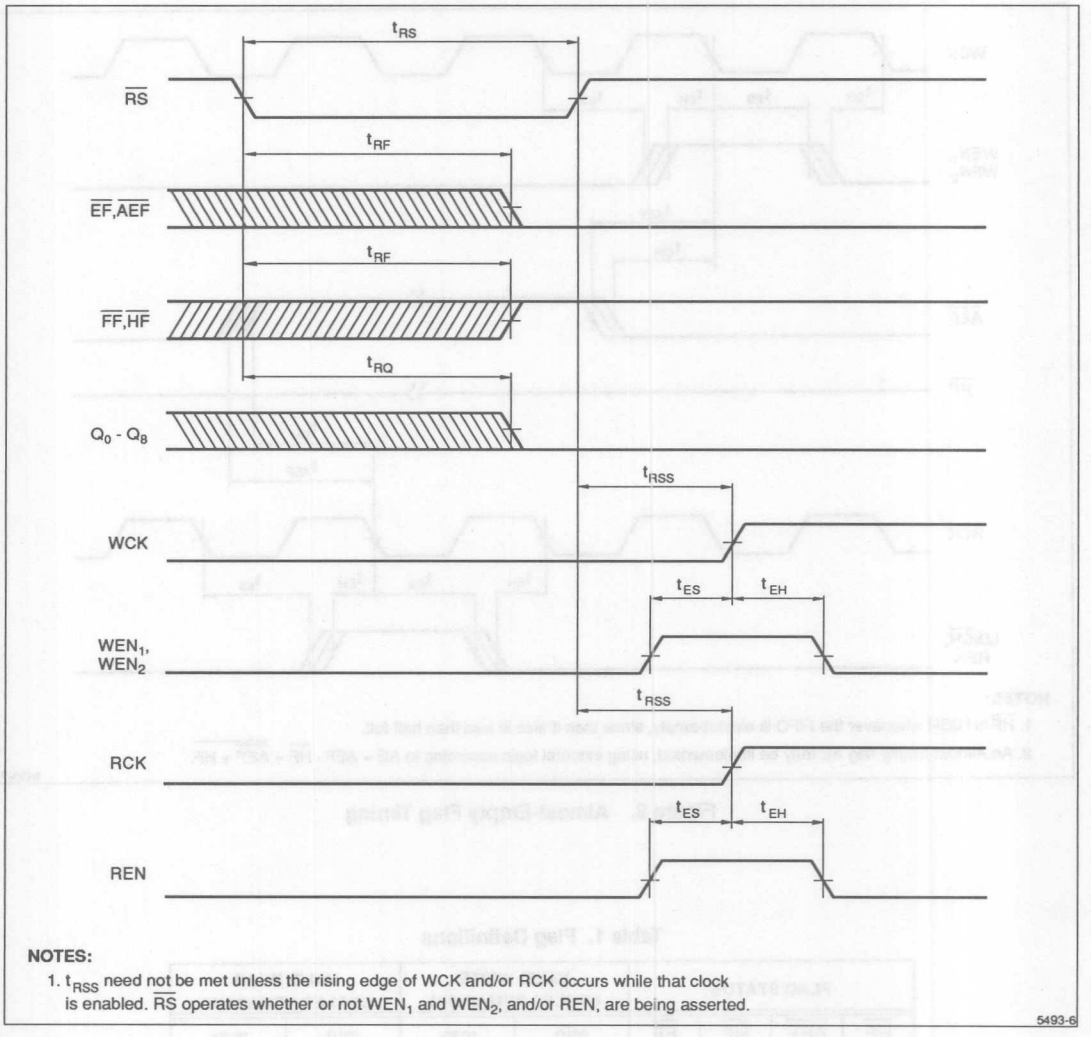


Figure 6. Serial Shift/Read Timing

TIMING DIAGRAMS (cont'd)

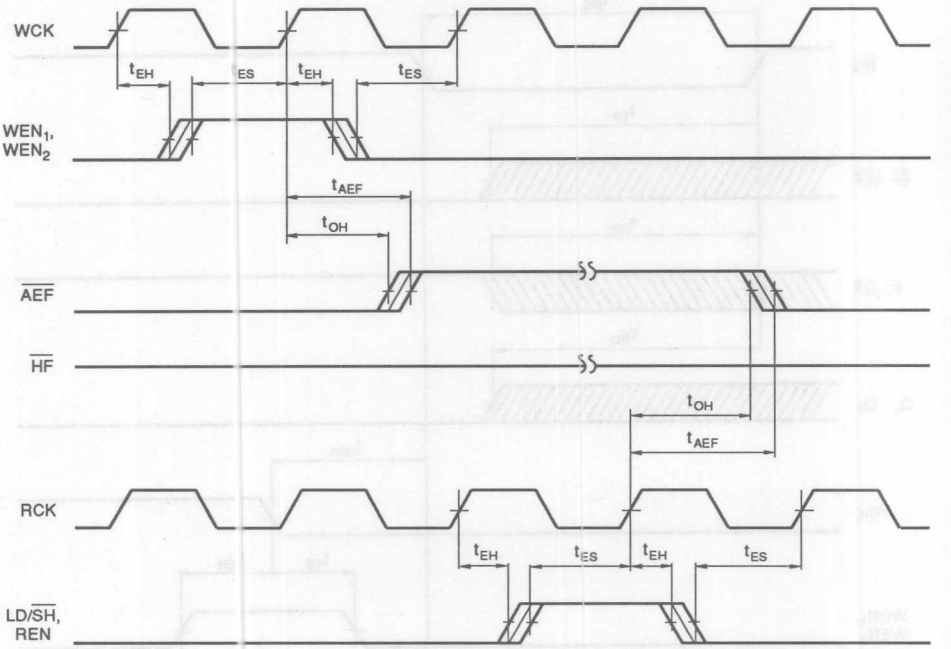


NOTES:

1. t_{RSS} need not be met unless the rising edge of WCK and/or RCK occurs while that clock is enabled. $\overline{RS}$ operates whether or not WEN_1 and WEN_2, and/or REN, are being asserted.

Figure 7. Reset Timing

TIMING DIAGRAMS (con'd)



NOTES:

1. $\overline{HF}$ is HIGH whenever the FIFO is almost-empty, since then it also is less than half-full.
2. An Almost-Empty flag AE may be implemented, using external logic according to $AE = AEF \cdot \overline{HF} = \overline{\overline{AEF} + HF}$.

5493-7

Figure 8. Almost-Empty Flag Timing

Table 1. Flag Definitions

FLAG STATUS				VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
$\overline{EF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{FF}$	min	max	min	max
0	0	1	1	4096	4096	0	0
1	0	1	1	4089	4095	1	7
1	1	1	1	2048	4088	8	2048
1	1	0	1	8	2047	2049	4088
1	0	0	1	1	7	4089	4095
1	0	0	0	0	0	4096	4096

TIMING DIAGRAMS (cont'd)

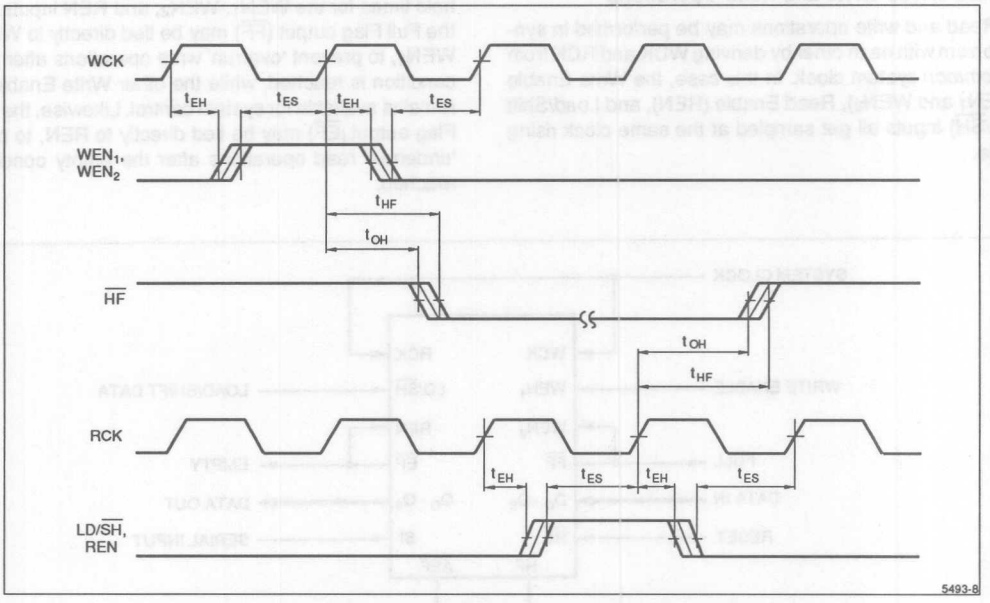
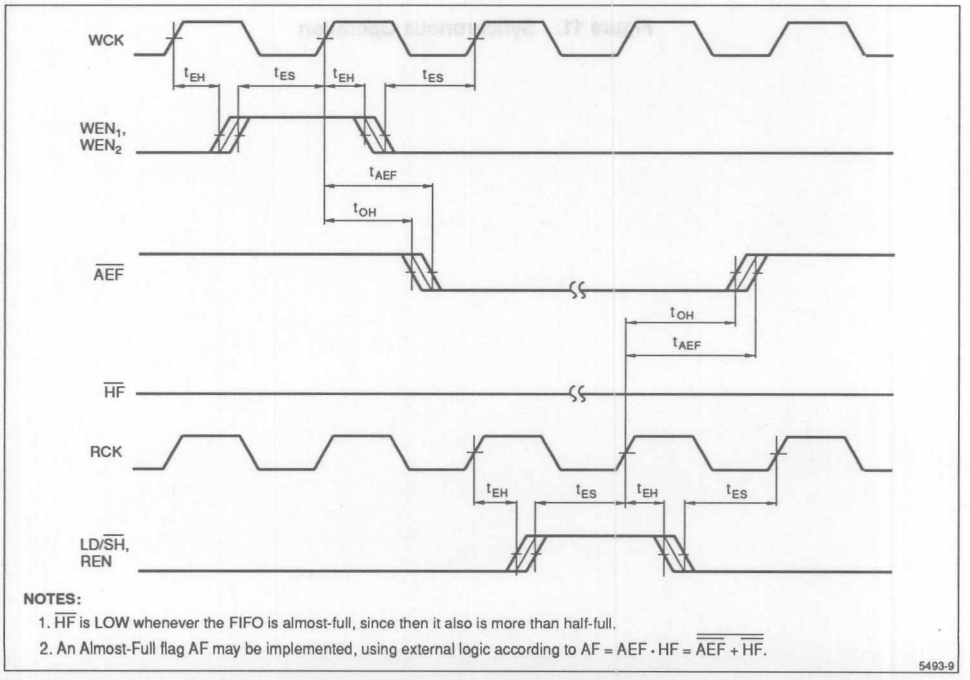


Figure 9. Half-Full Flag Timing



NOTES:

1. $\overline{HF}$ is LOW whenever the FIFO is almost-full, since then it also is more than half-full.
2. An Almost-Full flag AF may be implemented, using external logic according to $AF = AEF \cdot HF = \overline{\overline{AEF} + \overline{HF}}$.

Figure 10. Almost-Full Flag Timing

OPERATIONAL MODES

Synchronous Write and Read Operations

Read and write operations may be performed in synchronism with each other by deriving WCK and RCK from a *common* system clock. In this case, the Write Enable (WEN_1 and WEN_2), Read Enable (REN), and Load/Shift ($LD/\overline{SH}$) inputs all get sampled at the same clock rising edge.

This type of synchronous read/write operation ensures that flag outputs always satisfy the required setup and hold times for the WEN_1, WEN_2, and REN inputs. Thus, the Full Flag output ($\overline{FF}$) may be tied directly to WEN_1 or WEN_2, to prevent 'overrun' write operations after the full condition is reached, while the other Write Enable input remains available for system control. Likewise, the Empty Flag output ($\overline{EF}$) may be tied directly to REN, to prevent 'underrun' read operations after the empty condition is reached.

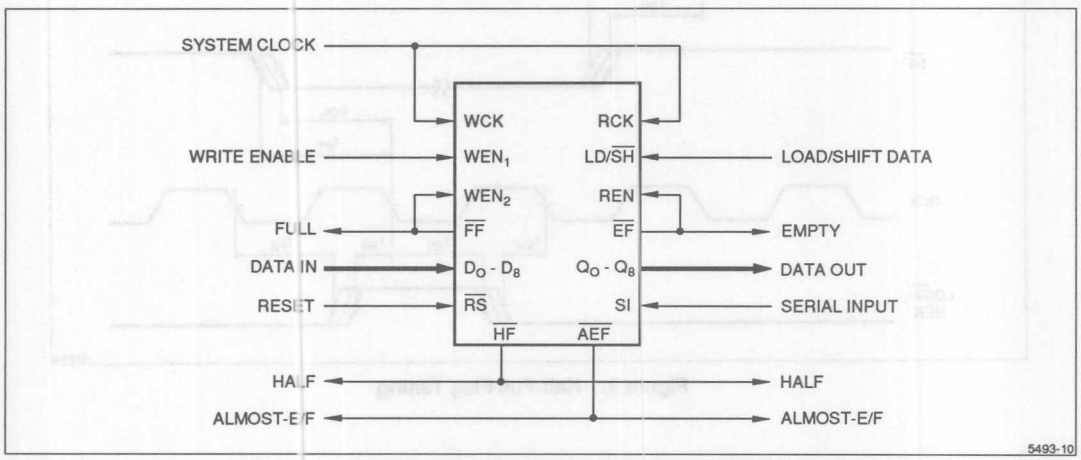


Figure 11. Synchronous Operation

OPERATIONAL MODES (cont'd)

Asynchronous Write and Read Operations

Write operations and read operations may be performed completely asynchronously with respect to each other, when the WCK input and the RCK input are derived from the clock signals of *different* systems. Under these conditions, status-flag transitions occur relative to two unpredictably-related clock edges. Therefore, these flags should not be used to drive Write Enable or Read Enable inputs directly, since they do not always satisfy valid setup times and hold times.

Instead, it is recommended that these enable signals be *controlled* by the user to ensure that adequate setup times and hold times are maintained. If the FIFO becomes either completely full or completely empty, then some synchronization between read and write operations at the full or empty boundaries becomes necessary to prevent timing violations.

When the FIFO is operating in this manner, the Almost-Empty/Full flag and the Half-Full flag should be used to provide some advance warning, to avoid overrunning or underrunning a FIFO internal boundary. Typically, these flags are used as system interrupts. When an interrupt is received by the faster of the two systems, a predefined block of data then may be transferred at the maximum data rate, as long as there is known to be sufficient room for it. In this way the full and empty boundaries are never reached, and yet maximum data throughput is maintained.

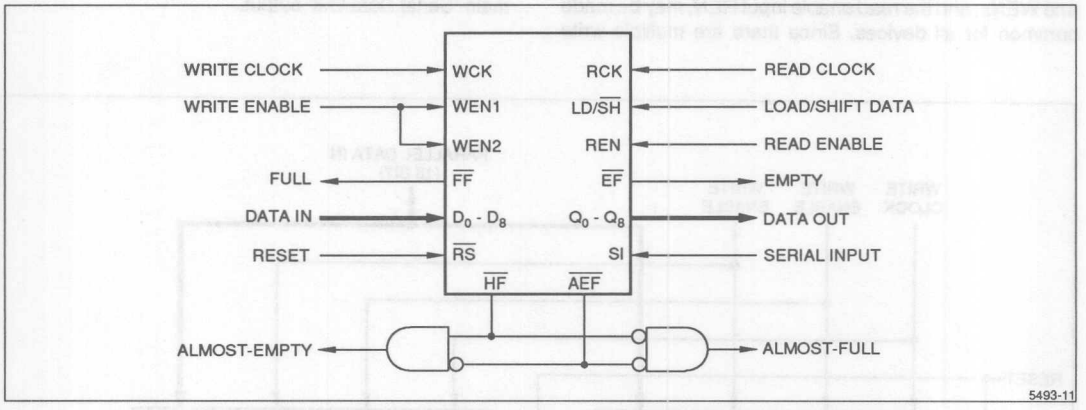


Figure 12. Asychronous Operation

OPERATIONAL MODES (cont'd)

Paralleled Operation

In paralleled operation, two or more LH5493 FIFOs are chained together into a wider 'effective FIFO.' The Serial Input (SI) of the first device in the chain serves as the 'effective-FIFO' serial input. This 'effective-FIFO' serial input may be used to insert additional control bits into the serial data stream, or may be tied to a permanent logic LOW or HIGH signal if unused. The SI input of each subsequent device is connected to one of the Data Out outputs ($Q_8 - Q_0$) of the preceding device in the chain. The final 'effective-FIFO' serial output bitstream is taken from one of the Data Out outputs of the last device in the chain. By choosing different Data Out pins, an additional one to nine bits of width can be added per device.

In 'paralleled' operation, the write enable inputs WEN_1 and WEN_2, and the read enable input REN, may be made common for all devices. Since there are multiple write enable inputs, one of them on each FIFO device may be crosscoupled to the Full Flag on another FIFO device, or to the logic AND of several such Full Flags, in order to prevent any individual FIFO device from getting out of synchronization with the overall 'effective FIFO.' The approach is analogous to the method shown in Figure 11 for preventing an LH5493 from overrunning its internal FIFO boundaries. Implementing the equivalent measures during reading always requires some external logic, since each LH5493 has just one read enable input.

Word widths do not have to be a multiple of nine. For instance, making the following changes to the circuit of Figure 13 adapts it to handle 16-bit parallel data in. The D_0 input and the Q_0 output need not be used for either LH5493. The Q_1 output of the LH5493 on the left is connected to the SI input of the LH5493 on the right; and the Q_1 output of the LH5493 on the right becomes the main 'Serial Data Out' output.

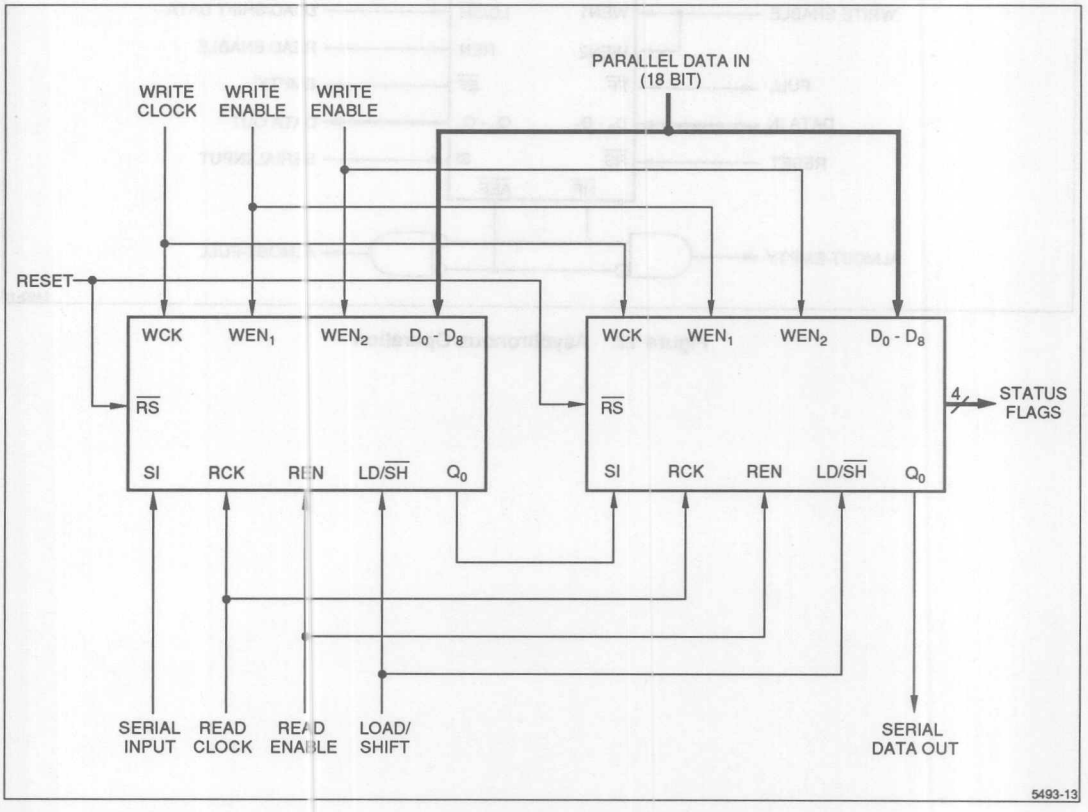
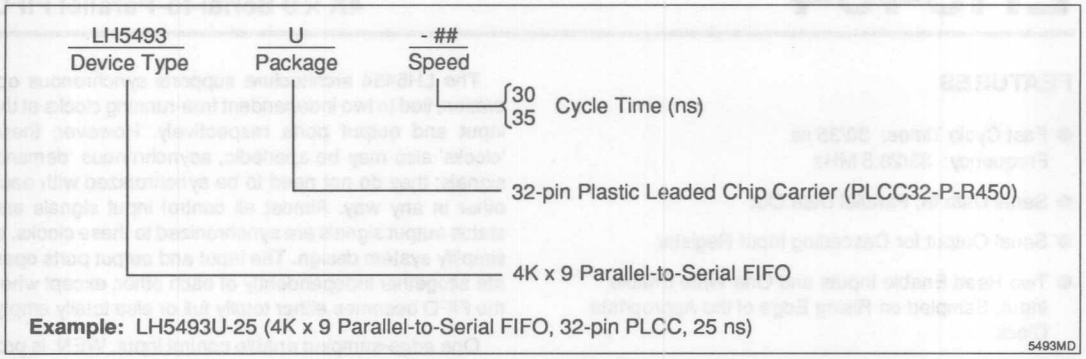


Figure 13. Paralleled Serial Operation (4096 × 18 Bit)

ORDERING INFORMATION



LH5494

4K × 9 Serial-to-Parallel FIFO

FEATURES

- Fast Cycle Times: 30/35 ns
  Frequency: 33/28.5 MHz
- Serial Data In; Parallel Data Out
- Serial Output for Cascading Input Register
- Two Read Enable Inputs and One Write Enable Input, Sampled on Rising Edge of the Appropriate Clock
- Fast-Fall-Through Time Internal Architecture Based on CMOS Dual-Port RAM Technology, 4096 × 9
- Fully Asynchronous Read and Write Operations
- Full, Half-Full, Almost-Empty/Full, and Empty Flags
- Three-State Outputs with Output Enable
- Reset/Reread Capability
- TTL and CMOS Compatible I/O
- 32-Pin PLCC Package

FUNCTIONAL DESCRIPTION

The LH5494 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS RAM technology, capable of containing up to 4096 nine-bit words. One LH5494 FIFO can input a serial bitstream, and output nine-bit bytes in parallel. Thus, a single LH5494 is capable of nine-bit-to-one-bit SIPO (Serial-In, Parallel-Out) operation.

An LH5494 has one one-bit serial input, and one nine-bit parallel output (read) port. And there is one one-bit serial output, which supports paralleling LH5494s for greater-word-width SIPO operation. This serial output also allows additional control bits to be inserted at will into the serial output bitstream.

The LH5494 architecture supports a very convenient method of *paralleling* multiple FIFOs for SIPO operation, without any additional logic being needed, in order to achieve a *wider* 'effective FIFO.' The paralleled LH5494 combination remains capable of performing all of the operations which a standalone LH5494 can perform. Thus, if two LH5494s are paralleled, the combination can input a serial bitstream and output 18-bit halfwords for 1-bit-to-18-bit SIPO operation. This paralleling scheme extends without change to an *arbitrary* number of LH5494s.

The LH5494 architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals; they do not need to be synchronized with each other in any way. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design. The input and output ports operate altogether independently of each other, except when the FIFO becomes either totally full or else totally empty.

One edge-sampled enable control input, WEN, is provided for the input port; and two such control inputs, REN_1 and REN_2, are provided for the output port. These synchronous control inputs may be used as write demands and read demands respectively, when an LH5494 is interfaced to continuously-clocked synchronous systems. Data flow is initiated at a port by the rising edge of the clock signal corresponding to that port, and is gated only by the appropriate edge-sampled enable control input signal(s).

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Half-Full, Almost-Empty/Full, and Empty. The Almost-Empty/Full flag is asserted whenever the internal memory is either within eight locations of 'empty,' or else within eight locations of 'full.' The Half-Full flag serves to distinguish the 'almost-empty' condition from the 'almost-full' condition. Also, during fully-synchronous operation, the Full flag

PIN CONNECTIONS

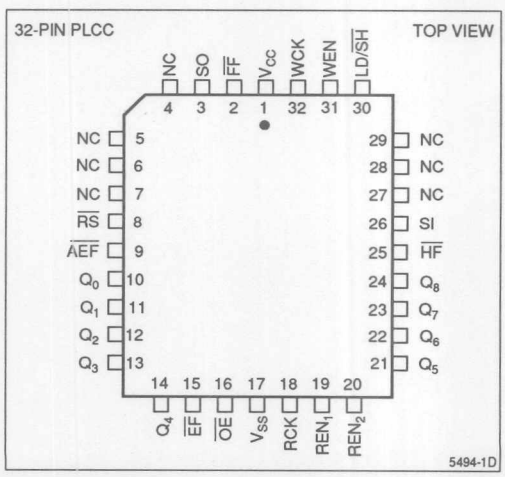


Figure 1. Pin Connections for PLCC Package

FUNCTIONAL DESCRIPTION (cont'd)

may be tied directly to WEN, and the Empty flag likewise may be tied directly to REN_1 or to REN_2, in order to prevent overrunning or underrunning the internal FIFO boundaries. (See Figure 11.)

Alternatively, the enabling of write or read operations may be controlled entirely by external system logic, while the flags serve strictly as system interrupts. This design approach works well when the input port clock and the output port clock are not synchronized to each other

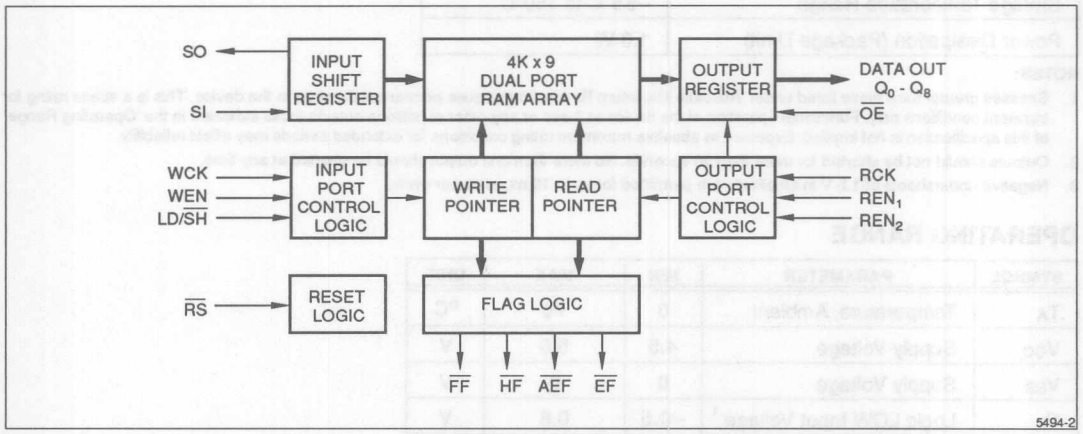


Figure 2. LH5494 Block Diagram

SIGNAL PIN DESCRIPTIONS

PIN	SIGNAL NAME/DESCRIPTION
$\overline{RS}$	Reset. An assertive-LOW input which initializes the internal address pointers and flags.
WCK	Write Clock. A free-running clock input for Write operations.
RCK	Read Clock. A free-running clock input for Read operations.
SI	Serial Input. SI is sampled on the rising edge of WCK, whenever WEN is being asserted.
SO	Serial Output. A serial data output signal, to allow paralleled SIPO operation of multiple devices.
$Q_0 - Q_8$	Data Outputs. $Q_0 - Q_8$ are updated following the rising edge of RCK, whenever REN_1 and REN_2 are both being asserted.
WEN	Write Enable. An assertive-HIGH input signal which is sampled on the rising edge of WCK to control the flow of data into the FIFO.
LD/$\overline{SH}$	Load/Shift. An input signal which is sampled on the rising edge of WCK to control the load of parallel data from Input Shift Register into the FIFO.
REN_1	Read Enable 1. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both REN_1 and REN_2 must be asserted in order to enable a read operation.
REN_2	Read Enable 2. An assertive-HIGH input signal which is sampled on the rising edge of RCK to control the flow of data out of the FIFO. Both REN_1 and REN_2 must be asserted in order to enable a read operation.
$\overline{FF}$	Full Flag. An assertive-LOW output indicating when the FIFO is full.
$\overline{HF}$	Half-Full Flag. An assertive-LOW output indicating when the FIFO is more than half full.
$\overline{AEF}$	Almost-Empty/Full. An assertive-LOW output indicating when the FIFO either is within eight locations of full, or else is within eight locations of empty.
$\overline{EF}$	Empty Flag. An assertive-LOW output indicating, when asserted, when the FIFO is empty.
$\overline{OE}$	Output Enable. An assertive-LOW signal which, when asserted, places the data outputs $Q_0 - Q_8$ in a low-impedance state.

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential[3]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	V_{CC} + 0.5	V

NOTE:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IH} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at f_C = max		150	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		25	mA

NOTE:

1. I_{CC} and I_{CC2} are dependent upon actual output loading and cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 3

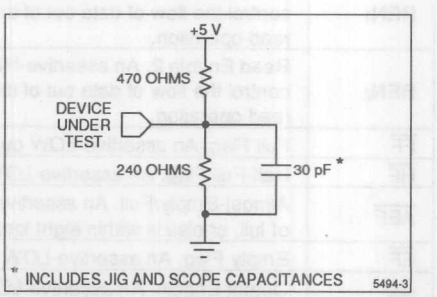


Figure 3. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance	7 pF
C_O (Output Capacitance)	7 pF

NOTES:
1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DESCRIPTION	–25		–30		–35		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f_C	Cycle Frequency	–	40	–	33.3	–	28.5	MHz
t_{WC}	Write Clock Cycle Time	25	–	30	–	35	–	ns
t_{WH}	Write Clock HIGH Time	10	–	12	–	14	–	ns
t_{WL}	Write Clock LOW Time	10	–	12	–	14	–	ns
t_{RC}	Read Clock Cycle Time	25	–	25	–	35	–	ns
t_{RH}	Read Clock HIGH Time	10	–	10	–	14	–	ns
t_{RL}	Read Clock LOW Time	10	–	10	–	14	–	ns
t_{DS}	Data Setup Time to Rising Clock	10	–	10	–	10	–	ns
t_{DH}	Data Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_{ES}	Enable Setup TIme to Rising Clock	10	–	10	–	10	–	ns
t_{EH}	Enable Hold Time from Rising Clock	0	–	0	–	0	–	ns
t_A	Data Output Access Time	–	20	–	22	–	25	ns
t_{SA}	Serial Output Access Time	–	20	—	22	–	25	ns
t_{OH}	Output Hold Time from Rising RCK	5	–	5	–	5	–	ns
t_{OL}	$\overline{OE}$ to Data Outputs Low-Z [2]	1	–	1	–	1	–	ns
t_{OZ}	$\overline{OE}$ to Data Outputs High-Z [2]	–	10	–	11	–	12	ns
t_{OE}	Output Enable to Data Valid	–	10	–	11	–	12	ns
t_{EF}	Clock to Empty Flag Valid	–	20	–	22	–	25	ns
t_{FF}	Clock to Full Flag Valid	–	20	–	22	–	25	ns
t_{HF}	Clock to Half Flag Valid	–	35	–	37	–	40	ns
t_{AEF}	Clock to AEF Flag Valid	–	35	–	37	–	40	ns
t_{RS}	Reset Pulse Width	25	–	30	–	35	–	ns
t_{RSS}	Reset Setup Time [3]	10	–	12	–	15	–	ns
t_{RF}	Reset LOW to Flag Valid	–	30	–	32	–	35	ns
t_{RQ}	Reset to Data Outputs LOW	–	20	–	22	–	25	ns
t_{FRL}	First Read Latency [4]	18	–	19	–	20	–	ns
t_{FWL}	First Write Latency [5]	18	–	19	–	20	–	ns

NOTES:
1. All timing measurements performed at 'AC Test Condition' levels.
2. Value guaranteed by design; not currently production tested.
3. t_{RSS} need not be met *unless* either a rising edge of WCK occurs while WEN is being asserted, or else a rising edge of RCK occurs while REN_1 and REN_2 both are being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-Write delay, following a full condition, which is required to assure successful writing of data.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous Reset input ($\overline{RS}$) is asserted, i.e., taken to a LOW state. A reset operation is required after power up, before the first write operation occurs. The reset operation initializes both the read and write address pointers to the first physical memory location. After the falling edge of $\overline{RS}$, the status flags ($\overline{FF}$, $\overline{HF}$, $\overline{AEF}$, and $\overline{EF}$) are updated to indicate a valid empty condition.

Read, shift, and/or write operations need not be deactivated during a reset operation, but failure to do so requires observance of the Reset Setup Time (t_{RSS}), to assure that the first write and/or first read following a reset operation will occur predictably.

If no read operations have been performed following a reset operation, then the 'previous data' word being held in the output register consists of all zeroes. This data word is seen on the output bus ($Q_0 - Q_8$) whenever the output enable ($\overline{OE}$) is held LOW. Likewise, data in the input shift register is initialized to all zeroes after a reset operation.

Write

A shift operation is initiated on the rising edge of WCK, whenever WEN is HIGH and LD/$\overline{SH}$ is LOW. Data bits are shifted from MSB to LSB, with the data bit on the Serial Input (SI) replacing the contents of bit position D_7 in the input shift register, and the Serial Output (SO) copying the contents of bit position D_0.

A write operation consists of a parallel loading of data from the input shift register (bits $D_7 - D_0$), and the SI pin (bit D_8) to the FIFO memory array. A write operation is initiated on the rising edge of the Write Clock input (WCK), whenever both the edge-sampled Write Enable input (WEN) and the Load/Shift input (LD/$\overline{SH}$) are held HIGH.

When a full condition is reached, shift operations may continue; but write operations should be ceased, in order to prevent overwriting unread data. The state of the status flags has no direct effect on shift or write operations; that is, the execution of write operations is gated only by WEN, and the internal logic of the LH5494 itself has no interlock to prevent overrunning valid data after the internal write pointer 'wraps around' and catches up to the read pointer – and passes it, if writing is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

Following the first read operation from a full FIFO, another memory location is freed up, and the Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency time (t_{FWL}) after the first read operation from a full FIFO, in order to assure that a correct data word is written into the FIFO memory.

Read

A read operation consists of loading parallel data from the FIFO memory array to the output register. A read operation is initiated on the rising edge of the Read Clock input (RCK) whenever both of the edge-sampled Read Enable inputs (REN_1 and REN_2) are held HIGH for the prescribed setup and hold times. Read data becomes valid on the Data Out pins ($Q_0 - Q_8$) by a time t_A after the rising edge of RCK, provided that the Output Enable ($\overline{OE}$) is being held LOW. $\overline{OE}$ is an assertive-LOW asynchronous input. When $\overline{OE}$ is taken LOW, the $Q_0 - Q_8$ outputs are driven (i.e., are in a low-Z state) within a minimum time t_{OL}. When $\overline{OE}$ is taken HIGH, the $Q_0 - Q_8$ outputs are in a high-Z state within a maximum time t_{OZ}. The state of the four status flags has no direct effect on read operations; that is, the execution of read or shift operations is gated only by REN_1 and REN_2 and LD/$\overline{SH}$, and the internal logic of the LH5494 itself has no interlock to prevent underrunning valid data after the internal read pointer catches up to the write pointer – and passes it, if reading is continued. Figure 11 illustrates how such an interlock may be implemented by means of external connections.

When an empty condition is reached, read operations should be ceased, until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the Empty Flag ($\overline{EF}$) is deasserted ($\overline{EF}$ = HIGH). The next read operation should begin no earlier than a First Read Latency time (t_{FRL}) from the first write operation into an empty FIFO, in order to ensure that correct read data is retrieved.

Status Flags

Status Flags are included for Full ($\overline{FF}$), Half-Full ($\overline{HF}$), Almost-Empty/Full ($\overline{AEF}$), and Empty ($\overline{EF}$). These flags are updated at the boundary conditions given in Table 1 (page 5-119). Flag transitions follow the appropriate rising clock edge during an enabled read or write operation. The $\overline{AEF}$ flag is asserted whenever the FIFO either is less than eight locations away from an empty boundary, or else is less than eight locations away from a full boundary.

A separate indicator for Almost-Empty may be generated by a logical NOR of $\overline{AEF}$ with the inversion of $\overline{HF}$. An indicator for Almost-Full may be generated by a NOR of $\overline{AEF}$ with $\overline{HF}$. From an assertive-HIGH perspective, the NOR gate effectively is performing an AND operation in both of these cases.

Reset, Reread

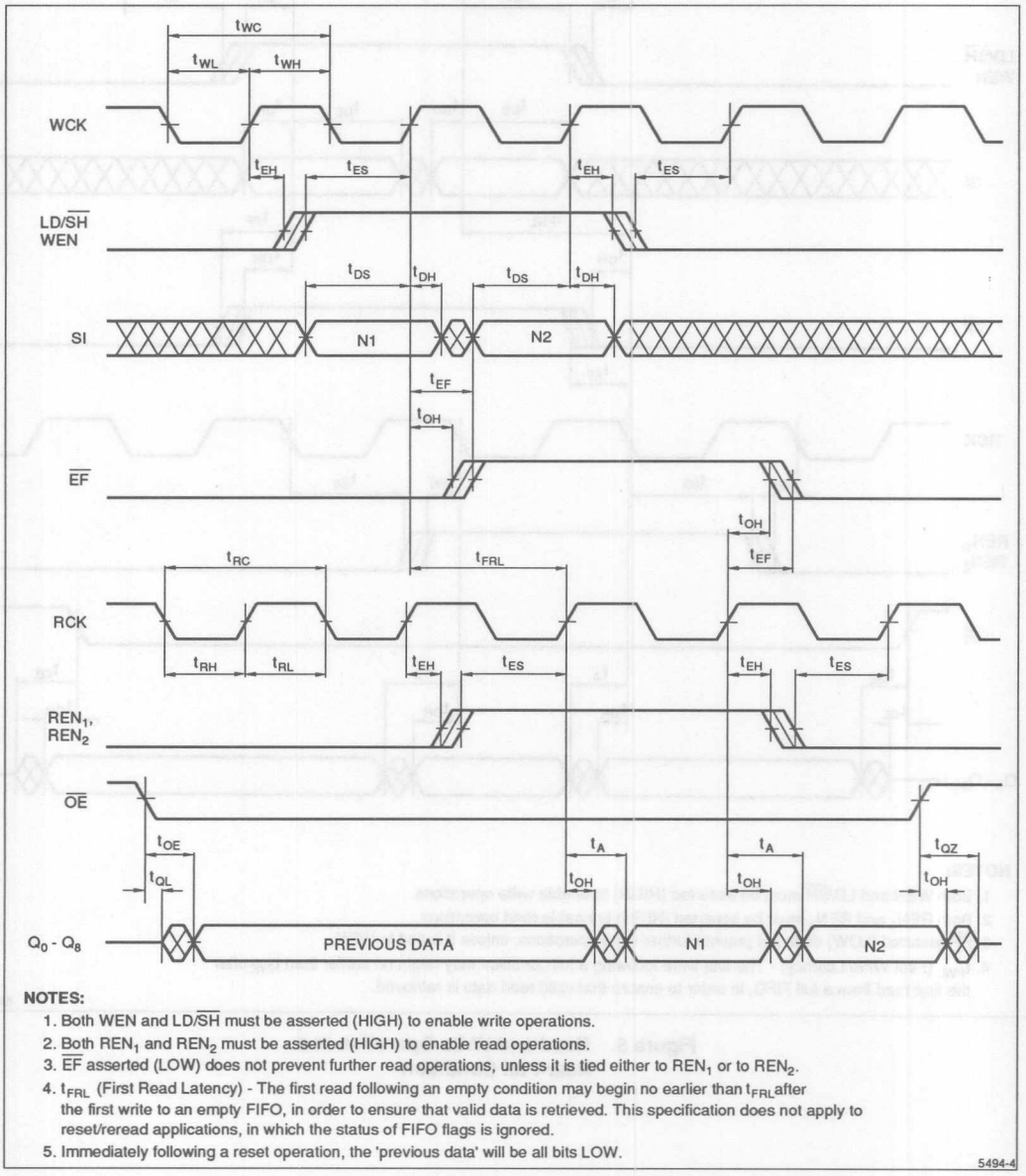
The FIFO can be made to reread previously read data through a reset operation, which initializes the internal read and write address pointers to the first physical location in the FIFO memory (location zero). The status flags are updated to indicate an empty condition; but up to 4096 words of old data, which previously had been written into and/or read from the FIFO, still then remain in

OPERATIONAL DESCRIPTION (cont'd)

the memory array. The status flags may be ignored, and data may be reaccessed by subsequent read operations.

The First Read Latency (t_{FRL}) specification does not apply to reset/reread operations, since no new data are being written to the FIFO following the Reset.

TIMING DIAGRAMS

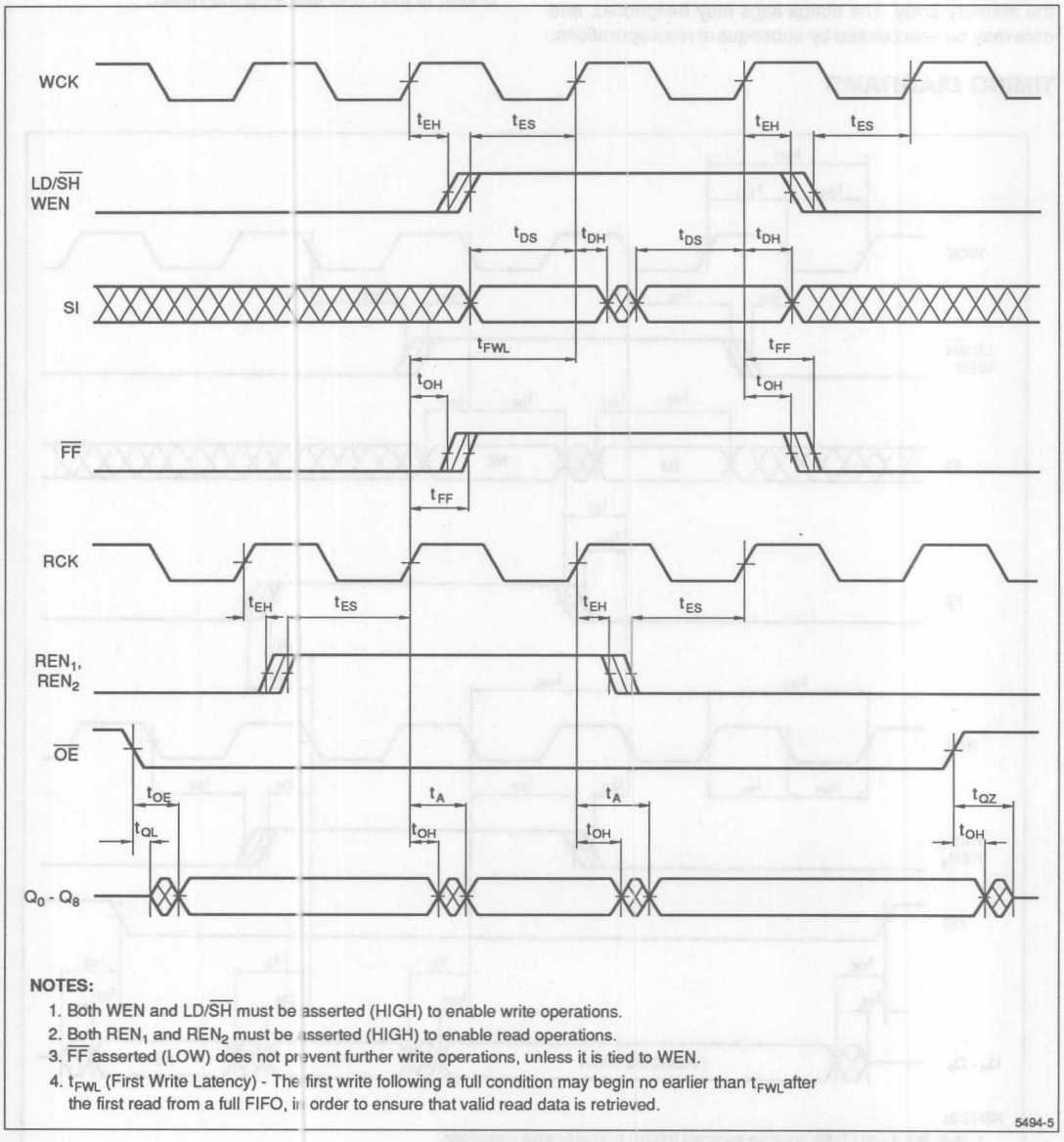


NOTES:

1. Both WEN and LD/$\overline{SH}$ must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{EF}$ asserted (LOW) does not prevent further read operations, unless it is tied either to REN_1 or to REN_2.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, in order to ensure that valid data is retrieved. This specification does not apply to reset/reread applications, in which the status of FIFO flags is ignored.
5. Immediately following a reset operation, the 'previous data' will be all bits LOW.

Figure 4. Write and Read Operations in a Near-Empty Condition

TIMING DIAGRAMS (cont'd)



NOTES:

1. Both WEN and LD/$\overline{SH}$ must be asserted (HIGH) to enable write operations.
2. Both REN_1 and REN_2 must be asserted (HIGH) to enable read operations.
3. $\overline{FF}$ asserted (LOW) does not prevent further write operations, unless it is tied to WEN.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, in order to ensure that valid read data is retrieved.

5494-5

Figure 5. Read and Write Operation in a Near-Full Condition

TIMING DIAGRAMS (cont'd)

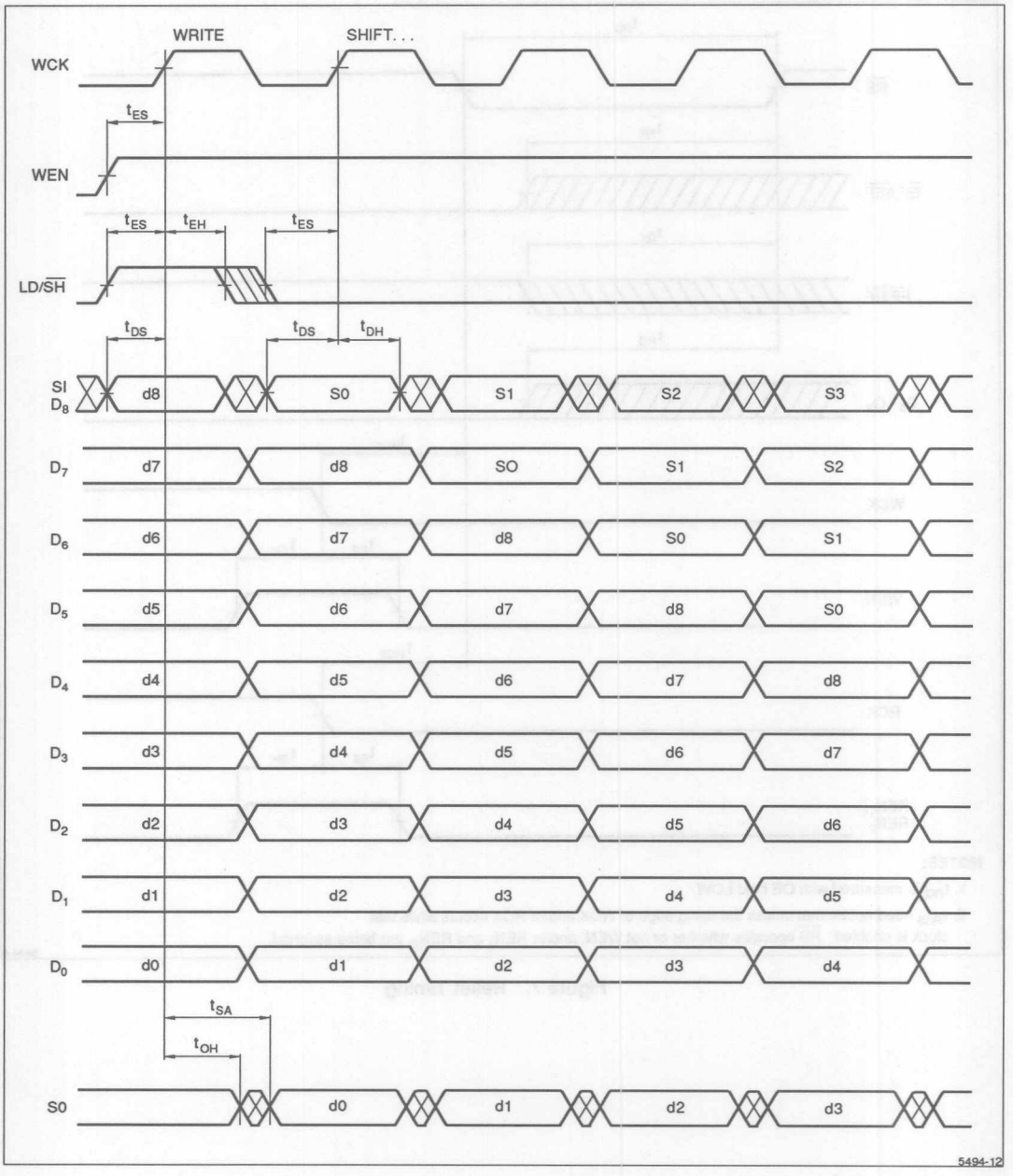
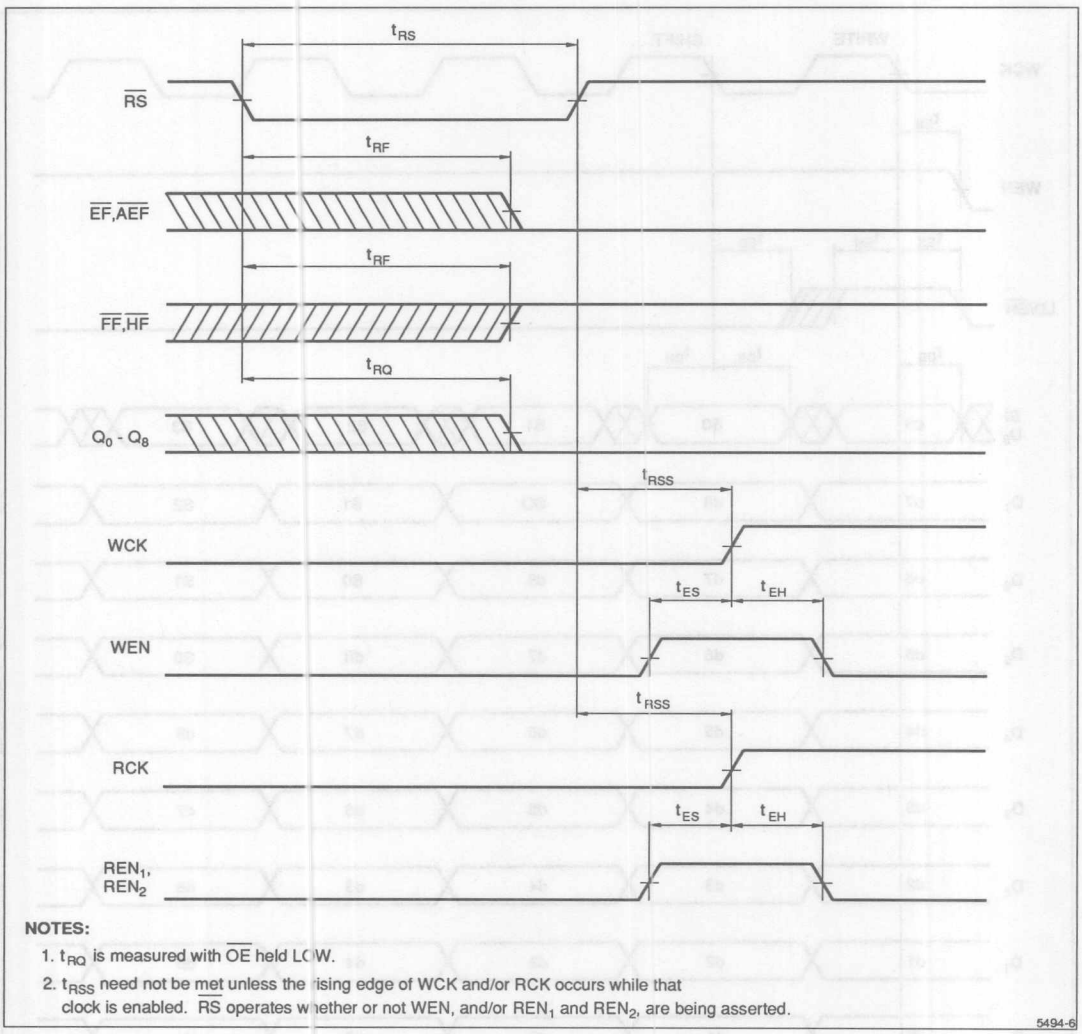


Figure 6. Serial Shift, Write Timing

TIMING DIAGRAMS (cont'd)



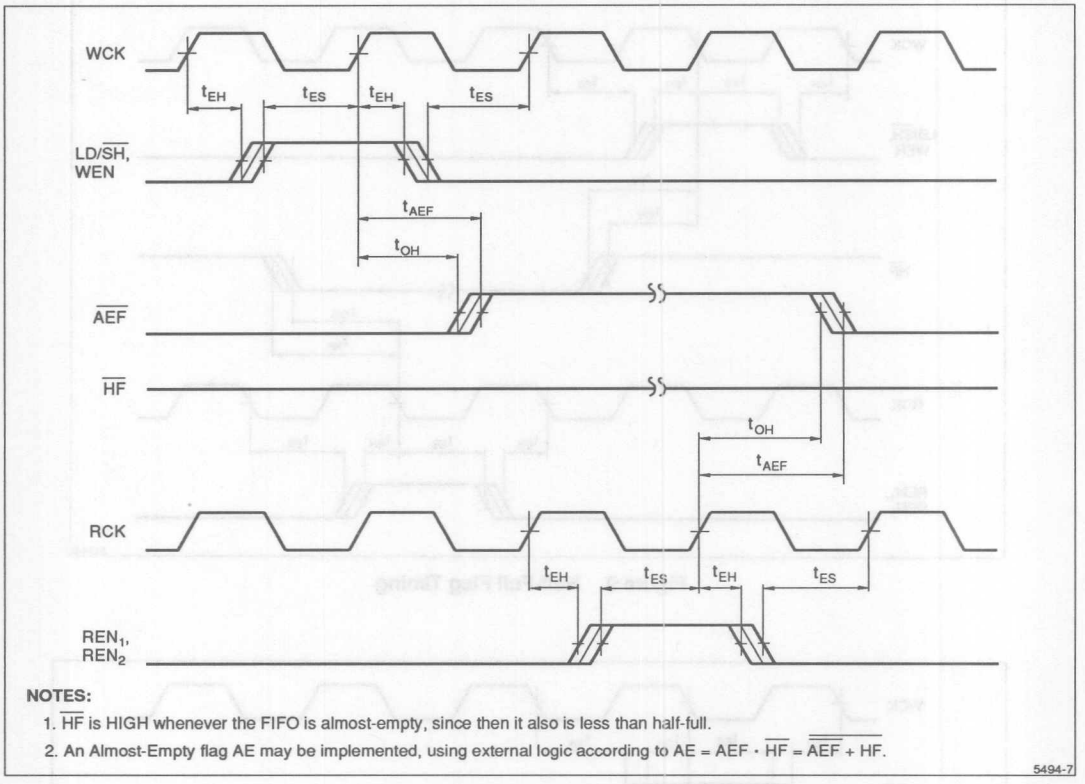
NOTES:

1. t_{RQ} is measured with $\overline{OE}$ held LOW.
2. t_{RSS} need not be met unless the rising edge of WCK and/or RCK occurs while that clock is enabled. $\overline{RS}$ operates whether or not WEN, and/or REN_1 and REN_2, are being asserted.

5494-6

Figure 7. Reset Timing

TIMING DIAGRAMS (cont'd)



NOTES:

1. $\overline{HF}$ is HIGH whenever the FIFO is almost-empty, since then it also is less than half-full.
2. An Almost-Empty flag AE may be implemented, using external logic according to $AE = AEF \cdot \overline{HF} = \overline{\overline{AEF} + HF}$.

5494-7

Figure 8. Almost-Empty Flag Timing

Table 1. Flag Definitions

FLAG STATUS				VALID WRITE CYCLES REMAINING		VALID READ CYCLES REMAINING	
$\overline{EF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{FF}$	min	max	min	max
0	0	1	1	4096	4096	0	0
1	0	1	1	4089	4095	1	7
1	1	1	1	2048	4088	8	2048
1	1	0	1	8	2047	2049	4088
1	0	0	1	1	7	4089	4095
1	0	0	0	0	0	4096	4096

TIMING DIAGRAMS (cont'd)

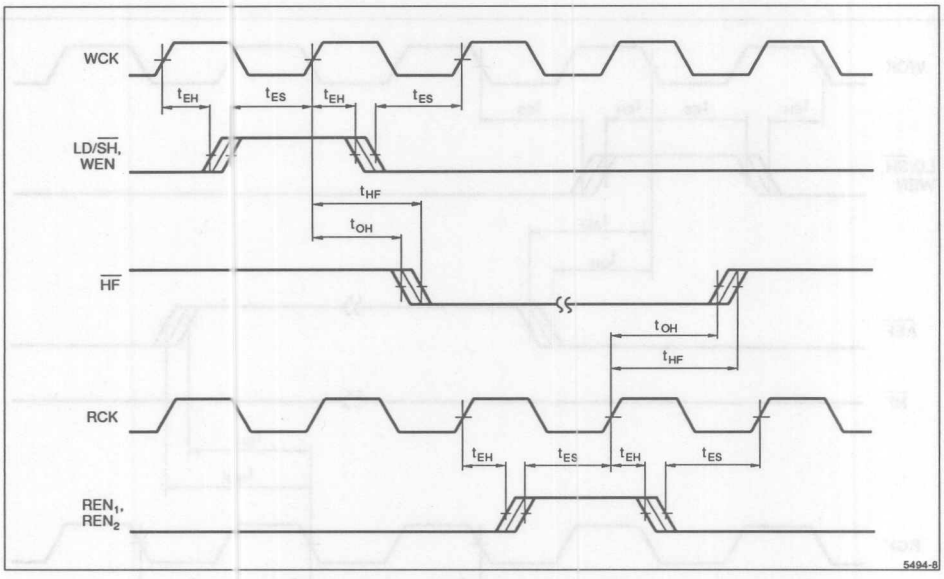
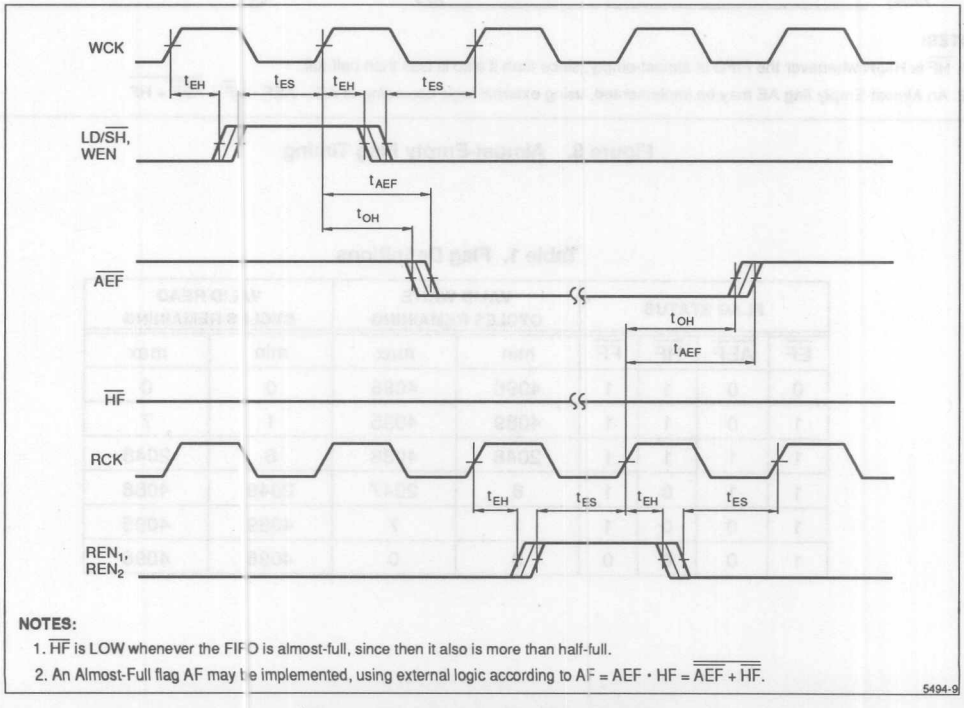


Figure 9. Half-Full Flag Timing



NOTES:

1. $\overline{HF}$ is LOW whenever the FIFO is almost-full, since then it also is more than half-full.
2. An Almost-Full flag AF may be implemented, using external logic according to $AF = AEF \cdot HF = \overline{\overline{AEF} + \overline{HF}}$.

Figure 10. Almost-Full Flag Timing

OPERATIONAL MODES

Synchronous Read and Write Operations

Read and write operations may be performed in synchronism with each other by deriving WCK and RCK from a *common* system clock. As such, the Read Enable (REN_1 and REN_2), Write Enable (WEN), and Load/Shift (LD/$\overline{SH}$) inputs all get sampled at the same clock rising edge.

This type of synchronous read/write operation ensures that flag outputs always satisfy the required setup and hold times for the REN_1, REN_2, and WEN inputs. Thus, the Full Flag output ($\overline{FF}$) may be tied directly to WEN, in order to prevent 'overrun' write operations when the full condition is reached. Likewise, the Empty Flag output ($\overline{EF}$) may be tied directly to REN_1 or REN_2, in order to prevent 'underrun' read operations when the empty condition is reached, while the other Read Enable input remains available for system control.

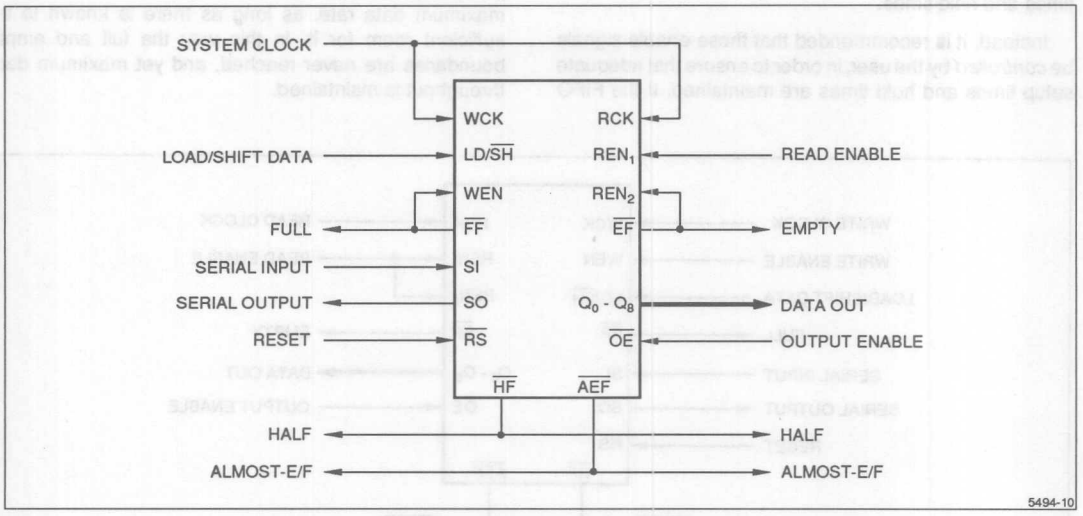


Figure 11. Synchronous Operation

OPERATIONAL MODES (cont'd)

Asynchronous Read and Write Operations

Write operations and read operations may be performed completely asynchronously relative to each other, when the RCK input and the WCK input are derived from clock signals of *different* systems. Under these conditions, status-flag transitions occur relative to two unpredictably-related clock edges. Therefore, these flags should not be used to drive Read Enable or Write Enable inputs directly, since they do not always satisfy valid setup times and hold times.

Instead, it is recommended that these enable signals be *controlled* by the user, in order to ensure that adequate setup times and hold times are maintained. If the FIFO becomes either completely full or completely empty, then some synchronization between read and write operations at the full or empty boundaries becomes necessary to prevent timing violations.

When the FIFO is operating in this manner, the Almost-Empty/Full flag and the Half-Full flag should be used to provide some advance warning, to avoid overrunning or underrunning a FIFO internal boundary. Typically, these flags are used as system interrupts. When an interrupt is received by the faster of the two systems, a predefined block of data then may be transferred at the maximum data rate, as long as there is known to be sufficient room for it. In this way the full and empty boundaries are never reached, and yet maximum data throughput is maintained.

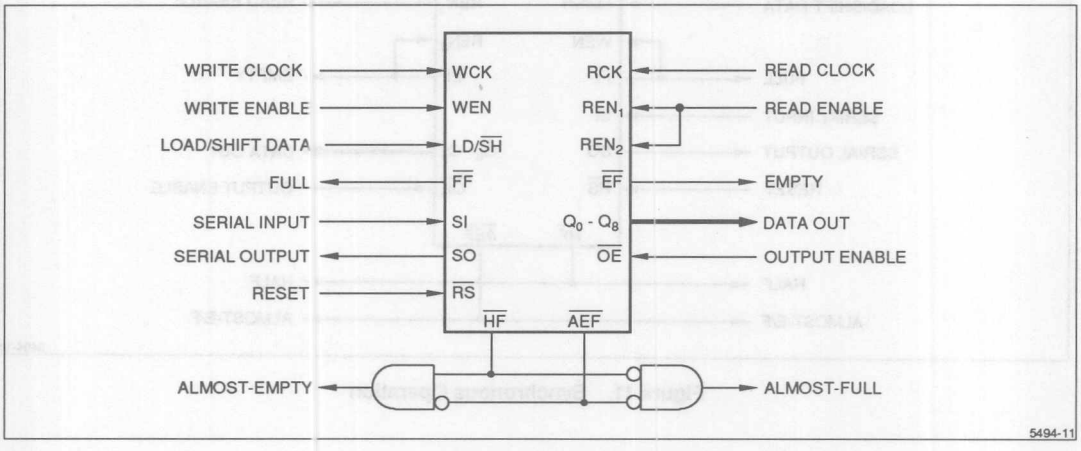


Figure 12. Asychronous Operation

OPERATIONAL MODES (cont'd)

Cascaded Operation

Cascaded operation allows LH5494 input shift registers to be extended in wordwidth, by interconnecting multiple LH5494 devices in a serial chain. The Serial Input (SI) of the first device in the chain serves as the 'effective-FIFO' serial input. The SI pin of any subsequent device is connected to the Serial Out (SO) pin of the preceding device in the chain. The final 'effective FIFO' serial output data (if needed) is taken from the SO pin of the last device in the chain.

In cascaded operation, the output port may be configured either for an increase in FIFO depth, or for an increase in FIFO wordwidth. When the output port is expanded in width, the Read Enable inputs (REN_1 and REN_2) and Output Enable ($\overline{OE}$) are common for all devices.

When the output port is expanded in depth, the common Data Out pins of multiple devices may be tied together. One Read Enable may then be used for system control, while the other Read Enable and $\overline{OE}$ are driven by decode logic to direct the flow of data. This decode logic should alternate read accesses from one device to the next in a sequential manner.

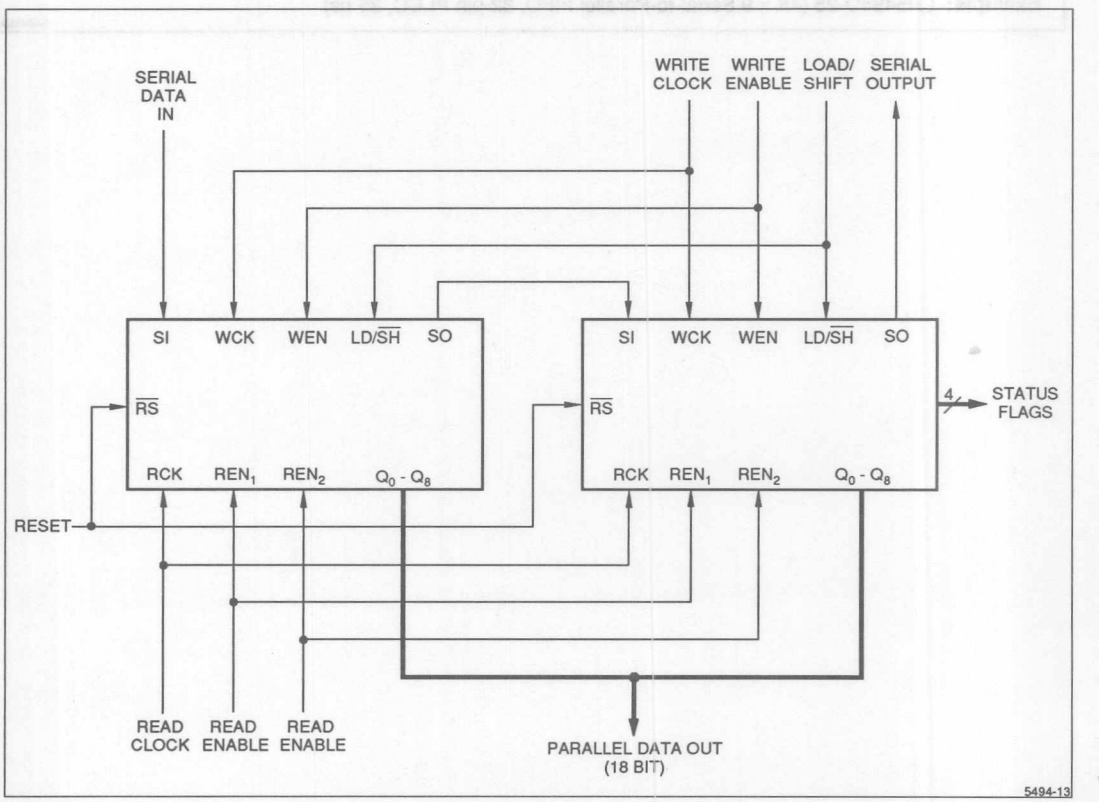
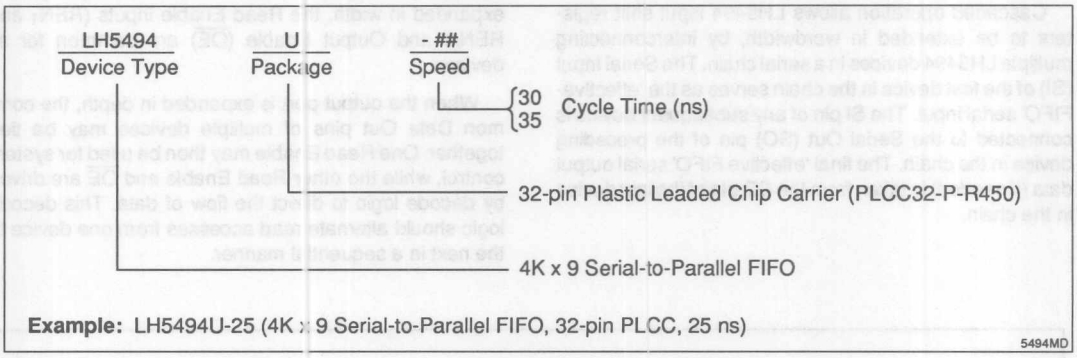


Figure 13. Cascaded Serial Operation (4096 × 18 Bit)

ORDERING INFORMATION



Example: LH5494U-25 (4K x 9 Serial-to-Parallel FIFO, 32-pin PLCC, 25 ns)

5494MD

LH5420

256 × 36 × 2 Bidirectional FIFO

FEATURES

- Fast Cycle Times: 25/30/35 ns
- Two 256 × 36-bit FIFO Buffers
- Full 36-bit Word Width
- Selectable 36/18/9-bit Word Width on Port B
- Fully Asynchronous Port-to-Port Communications
- 'Synchronous' Enable-Plus-Clock Control at Both Ports
- R/$\overline{W}$, Enable, Request, and Address Control Inputs Sampled on the Rising Clock Edge
- Synchronous Request/Acknowledge 'Handshake' Capability; Use is Optional
- Device Comes Up Into Known Default State at Reset; Programming is Allowed, but is not Required
- Asynchronous Output Enables
- 5 Status Flags per Port: Full, Almost-Full, Half-Full, Almost-Empty, and Empty
- Almost-Full Flag and Almost-Empty Flag are Programmable
- Mailbox Registers with Synchronized Flags
- Data Bypass Function
- Data Retransmit Function
- Automatic Byte Parity Checking
- TTL/CMOS-Compatible I/O
- Space-Saving PQFP and PGA Packages
- Mosel MS76542-SSFC and National Semiconductor NMF256X36X2 are Pin-Compatible and Functionally Equivalent

FUNCTIONAL DESCRIPTION

The LH5420 contains two FIFO buffers, FIFO #1 and FIFO #2. These operate in parallel, but in opposite directions, for bidirectional data buffering. FIFO #1 and FIFO #2 each are organized as 256 words by 36 bits. The LH5420 is ideal either for wide unidirectional applications or for bidirectional data applications; component count and board area are reduced.

The LH5420 has two 36-bit ports, Port A and Port B. Each port has its own port-synchronous clock, but the two ports may operate asynchronously relative to each other. Data flow is initiated at a port by the rising edge of the appropriate clock; it is gated by the corresponding edge-sampled enable, request, and read/write control signals. At the maximum operating frequency, the clock duty cycle may vary from 40% to 60%. At lower frequencies, the clock waveform may be quite asymmetric, as long as the minimum pulse-width conditions for clock-HIGH and clock-LOW remain satisfied; the LH5420 is a fully-static part.

Conceptually, the port clocks CK_A and CK_B are free-running, periodic 'clock' waveforms, used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that these 'clock' waveforms *must* be periodic. An 'asynchronous' mode of operation is possible, in one or both directions, independently, if the appropriate enable and request inputs are continuously asserted, and aperiodic 'clock' pulses of suitable duration are generated by external logic.

A synchronous request/acknowledge handshake facility is provided at each port for FIFO data access. This request/ acknowledge handshake resolves FIFO full and empty boundary conditions, when the two ports are operated asynchronously relative to each other.

FIFO status flags monitor the extent to which each FIFO buffer has been filled. Full, Almost-Full, Half-Full, Almost-Empty, and Empty flags are included for *each* FIFO. The Almost-Full and Almost-Empty flags are programmable over the entire FIFO depth, but are automatically initialized to eight locations from the respective FIFO boundaries at reset. A data block of 256 or fewer words may be retransmitted any desired number of times.

Two mailbox registers provide a separate path for passing control words or status words between ports. Each mailbox has a New-Mail-Alert Flag, which is synchronized to the reading port's clock. This mailbox function facilitates the synchronization of data transfers between asynchronous systems.

FUNCTIONAL DESCRIPTION (cont'd)

Data-bypass mode allows Port A to directly transfer data to or from Port B at reset. In this mode, the device acts as a registered transceiver under the control of Port A. For instance, a master processor on Port A can use the data bypass feature to send or receive initialization or configuration information directly, to or from a peripheral device on Port B, during system startup.

A word-width-select option is provided on Port B for 36-bit, 18-bit, or 9-bit data access. This feature allows word-width matching between Port A and Port B, with no additional logic needed. It also ensures maximum utilization of bus bandwidths.

A Byte Parity Check Flag at each port monitors data integrity. These flags are initialized for odd data parity at reset, but may be reprogrammed for even parity.

PIN CONNECTIONS

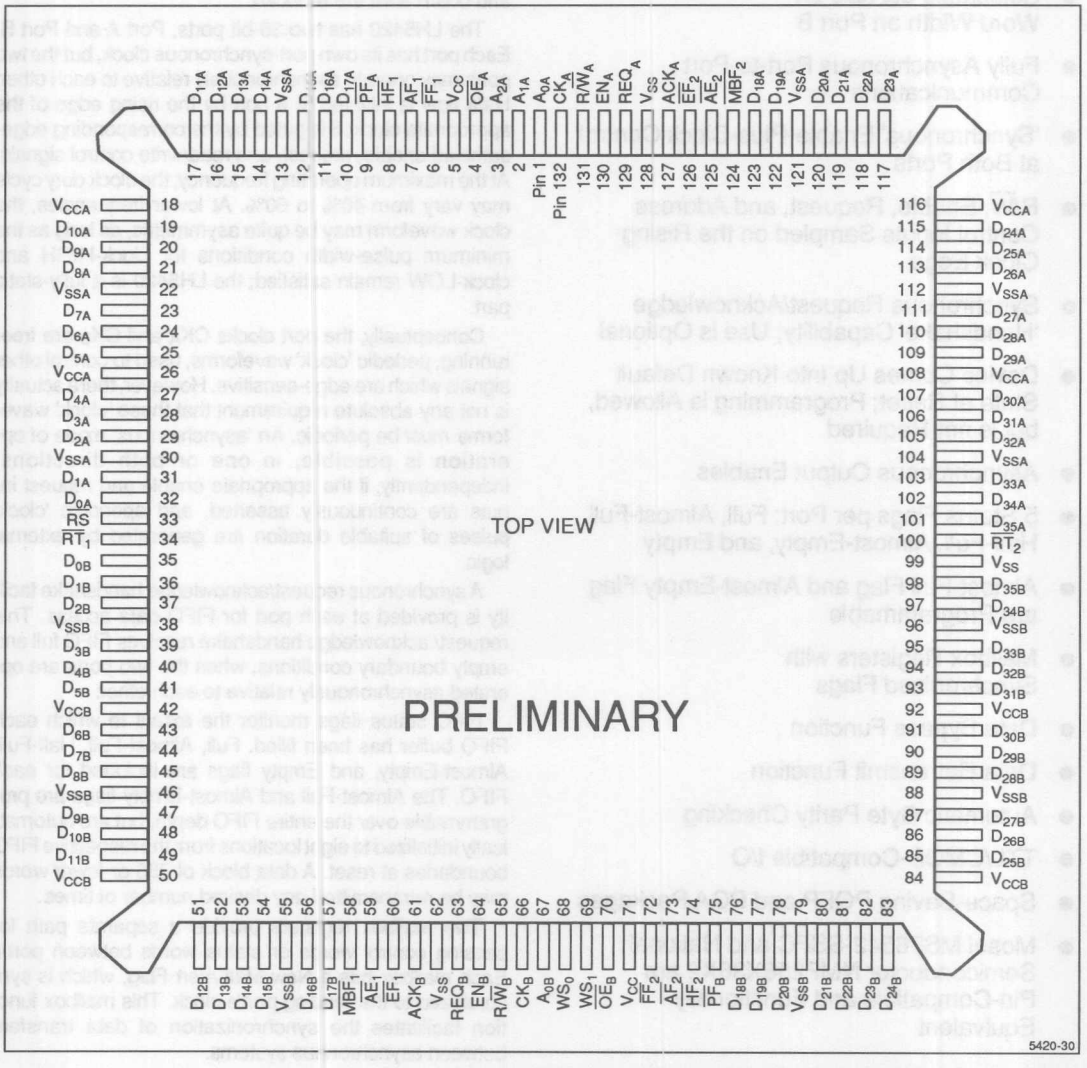


Figure 1. Pin Connections for 132-Pin Quad Flat Package (TOP VIEW)

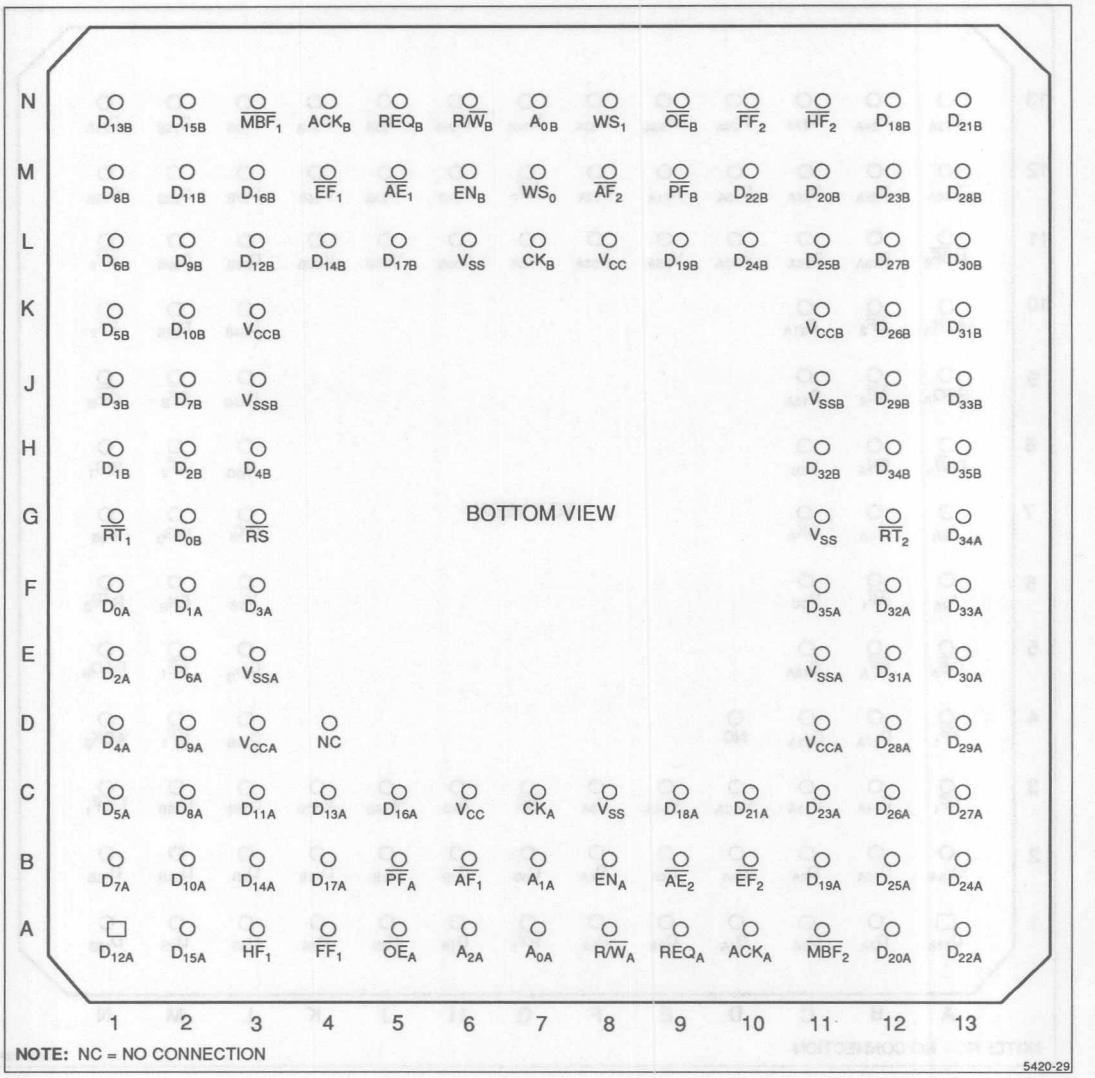


Figure 2. Pin Connections for 120-Pin PGA Package (BOTTOM VIEW)

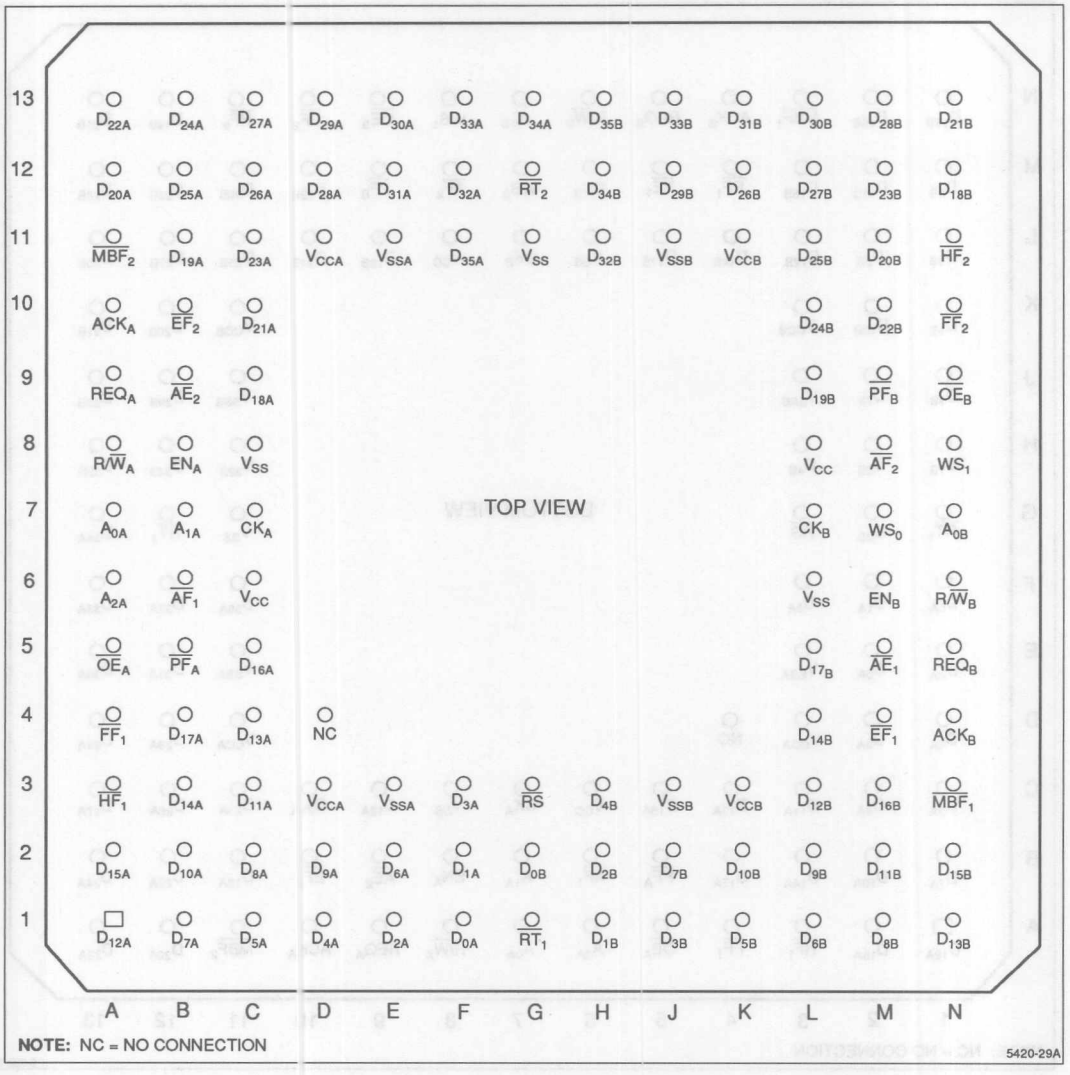


Figure 3. Pin Connections for 120-Pin PGA Package (Top View)

PIN LIST

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
A_{0A}	1	A7
A_{1A}	2	B7
A_{2A}	3	A6
$\overline{OE}_A$	4	A5
$\overline{FF}_1$	6	A4
$\overline{AF}_1$	7	B6
$\overline{HF}_1$	8	A3
$\overline{PF}_A$	9	B5
D_{17A}	10	B4
D_{16A}	11	C5
D_{15A}	12	A2
D_{14A}	14	B3
D_{13A}	15	C4
D_{12A}	16	A1
D_{11A}	17	C3
D_{10A}	19	B2
D_{9A}	20	D2
D_{8A}	21	C2
D_{7A}	23	B1
D_{6A}	24	E2
D_{5A}	25	C1
D_{4A}	27	D1
D_{3A}	28	F3
D_{2A}	29	E1
D_{1A}	31	F2
D_{0A}	32	F1
$\overline{RS}$	33	G3
$\overline{RT}_1$	34	G1
D_{0B}	35	G2
D_{1B}	36	H1
D_{2B}	37	H2
D_{3B}	39	J1
D_{4B}	40	H3
D_{5B}	41	K1
D_{6B}	43	L1
D_{7B}	44	J2
D_{8B}	45	M1
D_{9B}	47	L2
D_{10B}	48	K2
D_{11B}	49	M2
D_{12B}	51	L3
D_{13B}	52	N1
D_{14B}	53	L4
D_{15B}	54	N2

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
D_{16B}	56	M3
D_{17B}	57	L5
$\overline{MBF}_1$	58	N3
$\overline{AE}_1$	59	M5
$\overline{EF}_1$	60	M4
ACK_B	61	N4
REQ_B	63	N5
EN_B	64	M6
$R/\overline{W}_B$	65	N6
CK_B	66	L7
A_{0B}	67	N7
WS_0	68	M7
WS_1	69	N8
$\overline{OE}_B$	70	N9
$\overline{FF}_2$	72	N10
$\overline{AF}_2$	73	M8
$\overline{HF}_2$	74	N11
$\overline{PF}_B$	75	M9
D_{18B}	76	N12
D_{19B}	77	L9
D_{20B}	78	M11
D_{21B}	80	N13
D_{22B}	81	M10
D_{23B}	82	M12
D_{24B}	83	L10
D_{25B}	85	L11
D_{26B}	86	K12
D_{27B}	87	L12
D_{28B}	89	M13
D_{29B}	90	J12
D_{30B}	91	L13
D_{31B}	93	K13
D_{32B}	94	H11
D_{33B}	95	J13
D_{34B}	97	H12
D_{35B}	98	H13
$\overline{RT}_2$	100	G12
D_{35A}	101	F11
D_{34A}	102	G13
D_{33A}	103	F13
D_{32A}	105	F12
D_{31A}	106	E12
D_{30A}	107	E13
D_{29A}	109	D13

SIGNAL NAME	PQFP PIN NO.	PGA PIN NO.
D_{28A}	110	D12
D_{27A}	111	C13
D_{26A}	113	C12
D_{25A}	114	B12
D_{24A}	115	B13
D_{23A}	117	C11
D_{22A}	118	A13
D_{21A}	119	C10
D_{20A}	120	A12
D_{19A}	122	B11
D_{18A}	123	C9
$\overline{MBF}_2$	124	A11
$\overline{AE}_2$	125	B9
$\overline{EF}_2$	126	B10
ACK_A	127	A10
REQ_A	129	A9
EN_A	130	B8
$R/\overline{W}_A$	131	A8
CK_A	132	C7
V_{CC}	5	C6
V_{SSA}	13	E3
V_{CCA}	18	D3
V_{SSA}	22	E3
V_{CCA}	26	D3
V_{SSA}	30	E3
V_{SSB}	38	J3
V_{CCB}	42	K3
V_{SSB}	46	J3
V_{CCB}	50	K3
V_{SSB}	55	J3
V_{SS}	62	L6
V_{CC}	71	L8
V_{SSB}	79	J11
V_{CCB}	84	K11
V_{SSB}	88	J11
V_{CCB}	92	K11
V_{SSB}	96	J11
V_{SS}	99	G11
V_{SSA}	104	E11
V_{CCA}	108	D11
V_{SSA}	112	E11
V_{CCA}	116	D11
V_{SSA}	121	E11
V_{SS}	128	C8

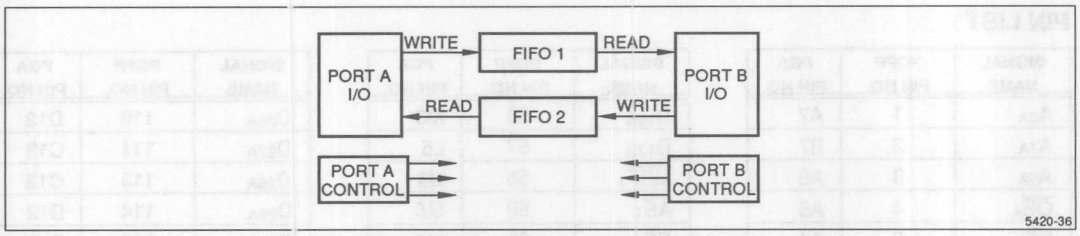


Figure 4a. Simplified LH5420 Block Diagram

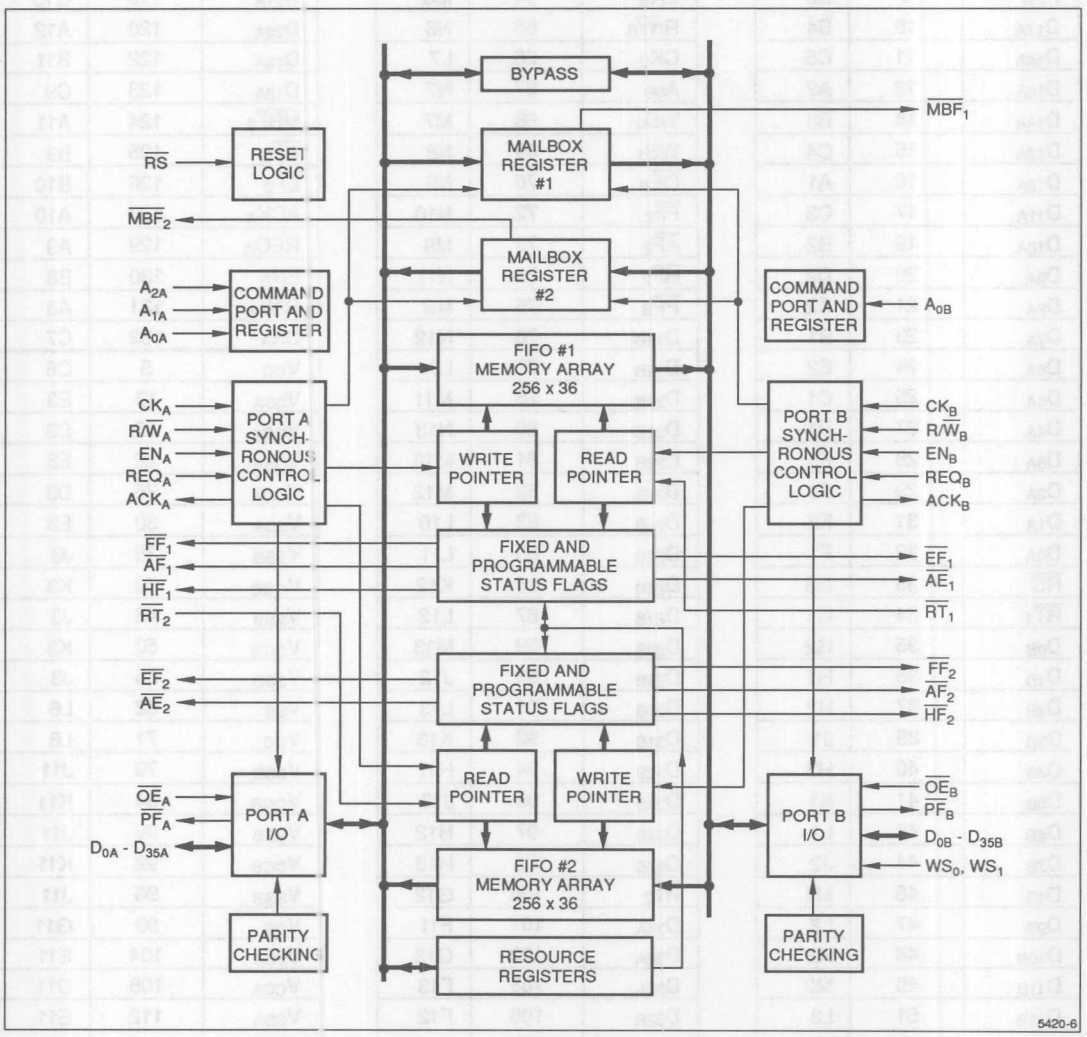


Figure 4b. Detailed LH5420 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
		GENERAL
V_{CC}, V_{SS}	V	Power, Ground
$\overline{RS}$	I	Reset
		PORT A
CK_A	I	Port A Free-Running Clock
$R/\overline{W}_A$	I	Port A Edge-Sampled Read/Write Control
EN_A	I	Port A Edge-Sampled Enable
A_{0A}, A_{1A}, A_{2A}	I	Port A Edge-Sampled Address Pins
$\overline{OE}_A$	I	Port A Level-Sensitive Output Enable
REQ_A	I	Port A Request/Enable
$\overline{RT}_2$	I	FIFO #2 Retransmit
$D_{0A} - D_{35A}$	I/O/Z	Port A Bidirectional Data Bus
$\overline{FF}_1$	O	FIFO #1 Full Flag (Write Boundary)
$\overline{AF}_1$	O	FIFO #1 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}_1$	O	FIFO #1 Half-Full Flag
$\overline{AE}_2$	O	FIFO #2 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}_2$	O	FIFO #2 Empty Flag (Read Boundary)
$\overline{MBF}_A$	O	Port A Mailbox New-Mail-Alert Flag for Mailbox #2
$\overline{PF}_A$	O	Port A Parity Flag
ACK_A	O	Port A Acknowledge
		PORT B
CK_B	I	Port B Free-Running Clock
$R/\overline{W}_B$	I	Port B Edge-Sampled Read/Write Control
EN_B	I	Port B Edge-Sampled Enable
A_{0B}	I	Port B Edge-Sampled Address Pin
$\overline{OE}_B$	I	Port B Level-Sensitive Output Enable
WS_0, WS_1	I	Port B Word-Width Select
REQ_B	I	Port B Request/Enable
$\overline{RT}_1$	I	FIFO #1 Retransmit
$D_{0B} - D_{35B}$	I/O/Z	Port B Bidirectional Data Bus
$\overline{FF}_2$	O	FIFO #2 Full Flag (Write Boundary)
$\overline{AF}_2$	O	FIFO #2 Programmable Almost-Full Flag (Write Boundary)
$\overline{HF}_2$	O	FIFO #2 Half-Full Flag
$\overline{AE}_1$	O	FIFO #1 Programmable Almost-Empty Flag (Read Boundary)
$\overline{EF}_1$	O	FIFO #1 Empty Flag (Read Boundary)
$\overline{MBF}_B$	O	Port B Mailbox New-Mail-Alert Flag for Mailbox #1
$\overline{PF}_B$	O	Port B Parity Flag
ACK_B	O	Port B Acknowledge

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [3]	−0.5 V to V_{CC} + 0.5 V
DC Output Current [2]	± 40 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	2 Watts (Quad Flat Pack)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.
3. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.2	V_{CC} + 0.5	V

NOTE:

1. Negative undershoot of 1.5 V in amplitude is permitted for up to 10 ns, once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V To V_{CC}	−10	10	µA
I_{LO}	I/O Leakage Current	$\overline{OE} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−10	10	µA
V_{OL}	Logic LOW Output Voltage	I_{OL} = 8.0 mA		0.4	V
V_{OH}	Logic HIGH Output Voltage	I_{OH} = −2.0 mA	2.4		V
I_{CC}	Average Supply Current [1]	Measured at f_C = max		280	mA
I_{CC2}	Average Standby Supply Current [1]	All Inputs = V_{IHMIN} (Clock idle)			mA
I_{CC3}	Power-Down Supply Current [1]	All Inputs = V_{CC} − 0.2 V (Clock idle)			mA

NOTE:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading, and I_{CC} is also dependent on cycle rates. Specified values are with outputs open; and, for I_{CC}, operating at minimum cycle times.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Output Reference Levels	1.5 V
Input Timing Reference Levels	1.5 V
Output Load, Timing Tests	Figure 5

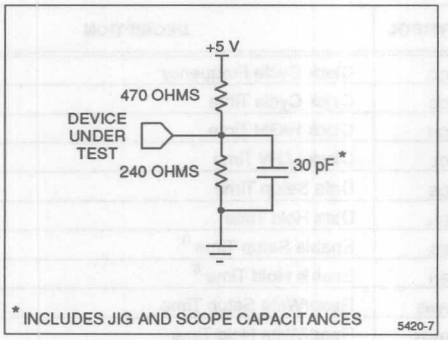


Figure 5. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} (Input Capacitance)	8 pF
C_O (Output Capacitance)	8 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz, with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS [1] (V_{CC} = 5 V ± 10%, T_A = 0°C to 70°C)

SYMBOL	DESCRIPTION	–25		–30		–35		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
f_{CC}	Clock Cycle Frequency	—	40	—	33	—	28.5	MHz
t_{CC}	Clock Cycle Time	25	—	30	—	35	—	ns
t_{CH}	Clock HIGH Time	10	—	12	—	15	—	ns
t_{CL}	Clock LOW Time	10	—	12	—	15	—	ns
t_{DS}	Data Setup Time	12	—	13	—	15	—	ns
t_{DH}	Data Hold Time	0	—	0	—	0	—	ns
t_{ES}	Enable Setup Time [6]	13	—	15	—	15	—	ns
t_{EH}	Enable Hold Time [6]	0	—	0	—	0	—	ns
t_{RWS}	Read/Write Setup Time	13	—	15	—	18	—	ns
t_{RWH}	Read/Write Hold Time	0	—	0	—	0	—	ns
t_{RQS}	Request Setup Time [6]	15	—	18	—	21	—	ns
t_{RQH}	Request Hold Time [6]	0	—	0	—	0	—	ns
t_{AS}	Address Setup Time [6]	15	—	18	—	21	—	ns
t_{AH}	Address Hold Time [6]	0	—	0	—	0	—	ns
t_A	Data Output Access Time	—	16	—	20	—	25	ns
t_{ACK}	Acknowledge Access Time	—	—[8]	—	20	—	25	ns
t_{OH}	Output Hold Time	5	—	5	—	5	—	ns
t_{ZX}	Output Enable Time, $\overline{OE}$ LOW to $D_0 – D_{35}$ Low-Z [3]	5	—	5	—	5	—	ns
t_{XZ}	Output Disable Time, $\overline{OE}$ HIGH to $D_0 – D_{35}$ High-Z [3]	—	15	—	20	—	25	ns
t_{EF}	Clock to $\overline{EF}$ Flag Valid (Empty Flag)	—	22	—	25	—	30	ns
t_{FF}	Clock to $\overline{FF}$ Flag Valid (Full Flag)	—	22	—	25	—	30	ns
t_{HF}	Clock to $\overline{HF}$ Flag Valid (Half-Full)	—	22	—	25	—	30	ns
t_{AE}	Clock to $\overline{AE}$ Flag Valid (Almost-Empty)	—	20	—	25	—	30	ns
t_{AF}	Clock to $\overline{AF}$ Flag Valid (Almost-Full)	—	20	—	25	—	30	ns
t_{MBF}	Clock to $\overline{MBF}$ Flag Valid (Mailbox Flag)	—	15	—	20	—	25	ns
t_{PF}	Data to Parity Flag Valid	—	17	—	20	—	25	ns
t_{RS}	Reset/Retransmit Pulse Width [7]	40/25	—	52/30	—	65/35	—	ns
t_{RSS}	Reset/Retransmit Setup Time [3]	20	—	25	—	30	—	ns
t_{RSH}	Reset/Retransmit Hold Time [3]	10	—	15	—	20	—	ns
t_{RF}	Reset LOW to Flag Valid	—	35	—	40	—	45	ns
t_{FRL}	First Read Latency [4]	25	—	30	—	35	—	ns
t_{FWL}	First Write Latency [5]	25	—	30	—	35	—	ns
t_{BS}	Bypass Data Setup	15	—	18	—	21	—	ns
t_{BH}	Bypass Data Hold	5	—	5	—	5	—	ns
t_{BA}	Bypass Data Access	—	20	—	25	—	30	ns

NOTES:

1. Timing measurements performed at 'AC Test Condition' levels.
2. Values are guaranteed by design; not currently production tested.
3. t_{RSS} and/or t_{RSH} need not be met unless a rising edge of CK_A occurs while EN_A is being asserted, or else a rising edge of CK_B occurs while EN_B is being asserted.
4. t_{FRL} is the minimum first-write-to-first-read delay, following an empty condition, which is required to assure valid read data.
5. t_{FWL} is the minimum first-read-to-first-write delay, following a full condtion, which is required to assure successful writing of data.
6. t_{AS}, t_{AH} address setup times and hold times need only be satisfied at clock edges which occur while the corresponding enables are being asserted.
7. First number used only when CK_A or CK_B is enabled; $t_{RS} = t_{RSS} + t_{CH} + t_{RSH}$.
8. The REQ/ACK facility is not available at cycle times less than 30 ns.

OPERATIONAL DESCRIPTION

Reset

The device is reset whenever the asynchronous Reset ($\overline{RS}$) input is taken LOW. A reset operation is required after power-up, before the first write operation may occur. The LH5420 is fully ready for operation after being reset. No device programming is required if the default states described below are acceptable.

A reset operation initializes the read-address and write-address pointers for FIFO #1 and FIFO #2 to those FIFO's first physical memory locations. FIFO and mailbox status flags are updated to indicate an empty condition. In addition, the programmable-status-flag offset values are initialized to eight. Thus, the $\overline{AE}_1/\overline{AE}_2$ flag gets asserted within eight locations of an empty condition, and the $\overline{AF}_1/\overline{AF}_2$ flag likewise gets asserted within eight locations of a full condition, for FIFO #1/FIFO #2 respectively.

Bypass Operation

During reset (whenever $\overline{RS}$ is LOW) the device acts as a registered transceiver, bypassing the internal FIFO memories. Port A acts as the master port. A write or read operation on Port A during reset transfers data directly to or from Port B. Port B is considered to be the slave, and does not permit write or read operations during reset. The direction of the bypass data transmission is determined by th $R/\overline{W}_A$ control input, which does not get overridden by the $\overline{RS}$ input. The bypass capability may be used to pass initialization or configuration data directly between a master processor and a peripheral device during reset.

Address Modes

Address pins select the device resource to be accessed by each port. Port A has three resource-register-select inputs, A_{0A}, A_{1A}, and A_{2A}, which select between FIFO access, mailbox-register access, and flag-offset-value-programming operating mode. Port B has a single address input, A_{0B}, to select between FIFO access or mailbox-register access. The status of the resource-register-select inputs is sampled at the rising edge of an enabled clock (CK_A or CK_B). Select-input definitions are summarized in Table 1.

FIFO Write

Port A writes to FIFO #1, and Port B writes to FIFO #2. A write operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the appropriate request (REQ_A or REQ_B) is held HIGH; the appropriate Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held LOW; the FIFO address is selected for the address inputs ($A_{2A} - A_{0A}$ or A_{0B}); and the prescribed setup times and hold times are observed for all of these signals. Setup times and hold times must also be observed on the data-bus pins ($D_{0A} - D_{35A}$ or $D_{0B} - D_{35B}$).

When a FIFO full condition is reached, write operations are locked out. Following the first read operation from a full FIFO, another memory location is freed up, and the corresponding Full Flag is deasserted ($\overline{FF}$ = HIGH). The first write operation should begin no earlier than a First Write Latency (t_{FWL}) after the first read operation from a full FIFO, to ensure that correct read data are retrieved.

FIFO Read

Port A reads from FIFO #2, and Port B reads from FIFO #1. A read operation is initiated on the rising edge of a clock (CK_A or CK_B) whenever: the appropriate enable (EN_A or EN_B) is held HIGH; the appropriate request (REQ_A or REQ_B) is held HIGH; the appropriate Read/Write control ($R/\overline{W}_A$ or $R/\overline{W}_B$) is held HIGH; and the FIFO address is selected for the address inputs ($A_{2A} - A_{0A}$ or A_{0B}); and the prescribed setup times and hold times are observed for all of these signals. Read data becomes valid on the data-bus pins ($D_{0A} - D_{35A}$ or $D_{0B} - D_{35B}$) by a time t_A after the rising clock (CK_A or CK_B) edge, provided that the data outputs are enabled.

$\overline{OE}_A$ and $\overline{OE}_B$ are assertive-LOW, asynchronous output enables. Their effect is only to enable or disable the output drivers of the respective Port. Disabling the outputs does *not* disable a read operation; data transmitted to the corresponding output register will remain available later, when the outputs again are enabled, unless it subsequently is overwritten.

When an empty condition is reached, read operations are locked out until a valid write operation(s) has loaded additional data into the FIFO. Following the first write to an empty FIFO, the corresponding empty flag ($\overline{EF}$) will be deasserted (HIGH). The first read operation should begin no earlier than a First Read Latency (t_{FRL}) after the first write to an empty FIFO, to ensure that correct read data is retrieved.

Table 1. Resource-Register Addresses

A_{2A}	A_{1A}	A_{0A}	RESOURCE
PORT A			
H	H	H	FIFO
H	H	L	Mailbox
H	L	H	$\overline{AF}_2$, $\overline{AE}_2$, $\overline{AF}_1$, $\overline{AE}_1$ Flag Offset Registers
H	L	L	Parity Mode Bit
L	H	H	$\overline{AE}_1$ Flag Offset Register
L	H	L	$\overline{AF}_1$ Flag Offset Register
L	L	H	$\overline{AE}_2$ Flag Offset Register
L	L	L	$\overline{AF}_2$ Flag Offset Register
A_{0B}			RESOURCE
PORT B			
H			FIFO
L			Mailbox

OPERATIONAL DESCRIPTION (cont'd)

Dedicated FIFO Status Flags

Six dedicated FIFO status flags are included for Full ($\overline{FF_1}$ and $\overline{FF_2}$), Half-Full ($\overline{HF_1}$ and $\overline{HF_2}$), and Empty ($\overline{EF_1}$ and $\overline{EF_2}$). $\overline{FF_1}$, $\overline{HF_1}$, and $\overline{EF_1}$ indicate the status of FIFO #1; and $\overline{FF_2}$, $\overline{HF_2}$, and $\overline{EF_2}$ indicate the status of FIFO #2.

A Full Flag is asserted following the rising clock edge for a write operation that fills the FIFO. A Full Flag is deasserted following the falling clock edge for a read operation to a full FIFO. A Half-Full Flag is updated following the rising clock edge of a read or write operation to a FIFO. An Empty Flag is asserted following the rising clock edge for a read operation that empties the FIFO. An Empty Flag is deasserted following the falling clock edge for a write operation to an empty FIFO.

Programmable Status Flags

Four programmable FIFO status flags are provided, two for Almost-Full ($\overline{AF_1}$ and $\overline{AF_2}$), and two for Almost-Empty ($\overline{AE_1}$ and $\overline{AE_2}$). Thus, each port has two programmable flags to monitor the status of the two internal FIFO buffer memories. The offset values for these flags are initialized to eight locations from the respective FIFO boundaries during reset, but can be reprogrammed over the entire FIFO depth.

Flag offsets may be written or read through the Port A data bus. All four programmable FIFO status flag offsets can be set simultaneously through a single 36-bit status word; or, each programmable flag offset can be set individually, through one of four eight-bit status words. Table 3 illustrates the data format for flag-programming words.

Mailbox Operation

Two mailbox registers are provided for passing control/status words between ports. Each port can read its own mailbox and write to the other port's mailbox. Mailbox access is performed on the rising edge of the controlling FIFO's clock, with the mailbox address selected and the enable (EN_A or EN_B) HIGH. That is, writing to Mailbox Register #1, or reading from Mailbox Register #2, is synchronized to CK_A; and writing to Mailbox Register #2, or reading from Mailbox Register #1, is synchronized to CK_B.

The $R/\overline{W}_{A/B}$ and $\overline{OE}_{A/B}$ pins control the direction and availability of mailbox-register access. Each mailbox register has its own New-Mail-Alert Flag, which is synchronized to the reading port's clock. These New-Mail-Alert Flags are status indicators only, and cannot inhibit mailbox-register read or write operations.

Request Acknowledge Handshake

An optional, synchronous, request-acknowledge handshake feature is provided for each port, to perform boundary synchronization between asynchronously-operated ports. The Request input ($REQ_{A/B}$) is sampled at a rising clock edge. With $REQ_{A/B}$ HIGH, $R/\overline{W}_{A/B}$ determines whether a FIFO read operation or a FIFO write operation is being requested. The Acknowledge output ($ACK_{A/B}$) is updated during the following clock cycle(s). $ACK_{A/B}$ meets the setup and hold time requirements of the Enable input (EN_A or EN_B). Therefore, $ACK_{A/B}$ may be tied back to the enable input to directly gate FIFO accesses, at a slight decrease in maximum operating frequency.

The assertion of $ACK_{A/B}$ signifies that $REQ_{A/B}$ was asserted. However, $ACK_{A/B}$ does not depend logically on $EN_{A/B}$; and thus the assertion of $ACK_{A/B}$ does *not* prove that a FIFO write access or a FIFO read access actually did occur. While $REQ_{A/B}$ and $EN_{A/B}$ are being held HIGH, $ACK_{A/B}$ may be considered as a synchronous, predictive boundary flag. That is, $ACK_{A/B}$ acts as a synchronized predictor of the Almost-Full Flag $\overline{AF}$ for write operations, or as a synchronized predictor of the Almost-Empty Flag $\overline{AE}$ for read operations.

Outside the 'almost-full' region and the 'almost-empty' region, $ACK_{A/B}$ remains continuously HIGH whenever $REQ_{A/B}$ is held continuously HIGH. Within the 'almost-full' region or the 'almost-empty' region, $ACK_{A/B}$ occurs only on every *third* cycle, to prevent an overrun of the FIFO's actual full or empty boundaries and to ensure that the t_{FWL} (first write latency) and t_{FRL} (first read latency) specifications are satisfied before $ACK_{A/B}$ is received.

The 'almost-full region' is defined as 'that region, where the Almost-Full Flag is being asserted'; and the 'almost-empty region' as 'that region, where the Almost-Empty Flag is being asserted.' Thus, the extent of these 'almost' regions depends on how the system has programmed the offset values for the Almost-Full Flags and the Almost-Empty Flags. If the system has *not* programmed them, these offset values remain at their default values, eight in each case.

If a write attempt is unsuccessful because the corresponding FIFO is full, or if a read attempt is unsuccessful because the corresponding FIFO is empty, $ACK_{A/B}$ is *not* asserted in response to $REQ_{A/B}$.

If the REQ/ACK handshake is not used, then the $REQ_{A/B}$ input may be used as a second enable input, at a possible minor loss in maximum operating speed. In this case, the $ACK_{A/B}$ output may be ignored.

WARNING: Whether or not the REQ/ACK handshake is being used, the $REQ_{A/B}$ input for a port *must* be asserted for the corresponding FIFO to operate.

Data Retransmit

A retransmit operation resets the read-address pointer of the corresponding FIFO (#1 or #2) back to the first FIFO physical memory location, so that data may be reread. The write pointer is not affected. The status flags are updated; and a block of up to 256 data words, which previously had been written and read from a FIFO, can be retrieved. The block to be retransmitted is bounded by the first FIFO memory location, and the FIFO memory

OPERATIONAL DESCRIPTION (cont'd)

location addressed by the write pointer. FIFO #1 retransmit is initiated by strobing the $\overline{RT}_1$ pin LOW. FIFO #2 retransmit is initiated by strobing the $\overline{RT}_2$ pin LOW. Read and write operations to a FIFO should be stopped while the corresponding Retransmit signal is being asserted.

Parity Check

The Parity Check Flags, $\overline{PF}_A$ and $\overline{PF}_B$, are asserted (LOW) whenever there is a parity error in the data word present on the Port A data bus or the Port B data bus respectively. The inputs to the parity-evalution logic come directly from the data bus bonding *pads*, in each case.

The four bytes of a 36-bit data word are grouped as $D_0 - D_8$, $D_9 - D_{17}$, $D_{18} - D_{25}$, and $D_{26} - D_{35}$. The parity of each nine-bit byte is individually checked, and the four single-bit parity indications are logically inclusive-ORed to produce the Parity-Flag output. Parity checking is initialized for odd parity at reset, but can be reprogrammed for even or odd parity during operation.

Word-Width Selection on Port B

The word width of data access on Port B is selected by the WS_0 and WS_1 control inputs. WS_1 is tied HIGH for 36-bit access. WS_0 and WS_1 both are tied LOW for single-byte access. For double-byte access, WS_0 is tied HIGH and WS_1 is tied LOW.

In the single-byte-access or double-byte-access modes, FIFO write operations on Port B pack the data to form 36-bit words when viewed from Port A. Similarly, single-byte or double-byte FIFO read operations on Port B essentially unpack 36-bit words through a series of shift operations. FIFO status flags are updated following the last access which forms a complete 36-bit transfer.

Note that the word-width programming feature is *only* supported for FIFO accesses. Mailbox and Data Bypass operations do *not* support word-width matching between Port A and Port B. Table 2, Figure 3 and Figure 4 summarize word-width selection for Port B.

Table 2. Port B Word-Width Selection

WS_1	WS_0	PORT B DATA WIDTH
H	H	36-Bit
H	L	36-Bit
L	H	18-Bit
L	L	9-Bit

Table 3. Flag Programming Words

RESOURCE-REGISTER ADDRESS			RESOURCE-REGISTER CONTENTS									
A_2	A_1	A_0										
			(NORMAL FIFO OPERATION)									
H	H	H	X...									
			MAILBOX									
H	H	L	X...									
			36-BIT MODE (A_{2A}, A_{1A}, A_{0A}) = 1, 0, 1									
			D_{34A} . . . D_{27A}			D_{25A} . . . D_{18A}			D_{16A} . . . D_{9A}			D_{7A} . . . D_{0A}	
H	L	H	X	$\overline{AF_2}$ Offset [1]		X	$\overline{AE_2}$ Offset [1]		X	$\overline{AF_1}$ Offset [1]		X	$\overline{AE_1}$ Offset [1]
			PARITY MODE (A_2, A_1, A_0) = 1, 0, 0 (WRITE ONLY)									
												D_{0A}
H	L	L	X...									X	Parity Mode [2]
			8-BIT $\overline{AE_1}$ FLAG (A_{2A}, A_{1A}, A_{0A}) = 0, 1, 1									
												D_{7A} . . . D_{0A}
L	H	H	X...									X	$\overline{AE_1}$ Offset [1]
			8-BIT $\overline{AF_1}$ FLAG (A_{2A}, A_{1A}, A_{0A}) = 0, 1, 0									
												D_{7A} . . . D_{0A}
L	H	L	X...									X	$\overline{AF_1}$ Offset [1]
			8-BIT $\overline{AE_2}$ FLAG (A_{2A}, A_{1A}, A_{0A}) = 0, 0, 1									
												D_{7A} . . . D_{0A}
L	L	H	X...									X	$\overline{AE_2}$ Offset [1]
			8-BIT $\overline{AF_2}$ FLAG (A_{2A}, A_{1A}, A_{0A}) = 0, 0, 0									
												D_{7A} . . . D_{0A}
L	L	L	X...									X	$\overline{AF_2}$ Offset [1]

NOTES:

1. All four programmable-flag-offset values are initialized to eight (8) during a reset operation.
2. Odd parity = HIGH; even parity = LOW. The parity mode is initialized to odd during a reset operation.

Table 4. Flag Definition Table [1]

FLAG	VALID READ CYCLES REMAINING				VALID WRITE CYCLES REMAINING			
	FLAG = LOW		FLAG = HIGH		FLAG = LOW		FLAG = HIGH	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
$\overline{FF}$	256	256	0	255	0	0	1	256
$\overline{AF}$	256-p	256	0	255-p	0	p	p + 1	256
$\overline{HF}$	129	256	0	128	0	127	128	256
$\overline{AE}$	0	q	q + 1	256	256-q	256	0	255-q
$\overline{EF}$	0	0	1	256	256	256	0	255

NOTE:

1. p is the number in the Almost-Full-Flag-Offset-Value register for that port. q is the number in the Almost-Empty-Flag-Offset-Value register for that port.

PORT B WORD-WIDTH SELECTION

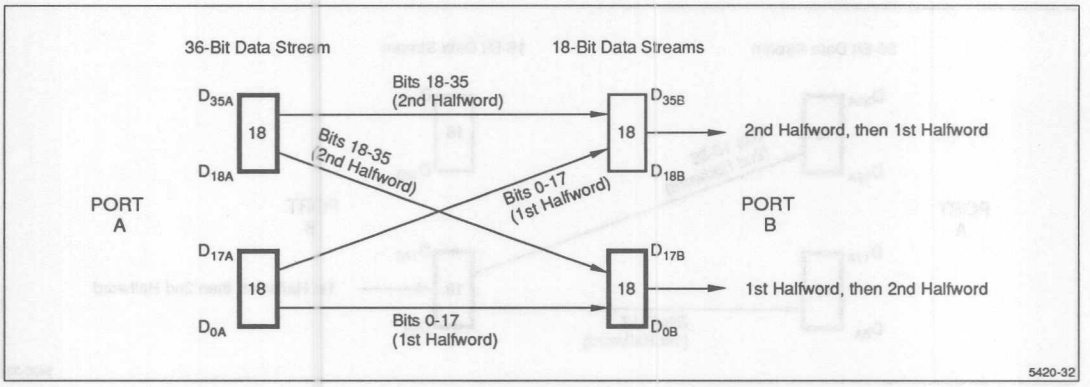


Figure 6a. 36-to-18 Funneling Through FIFO #1

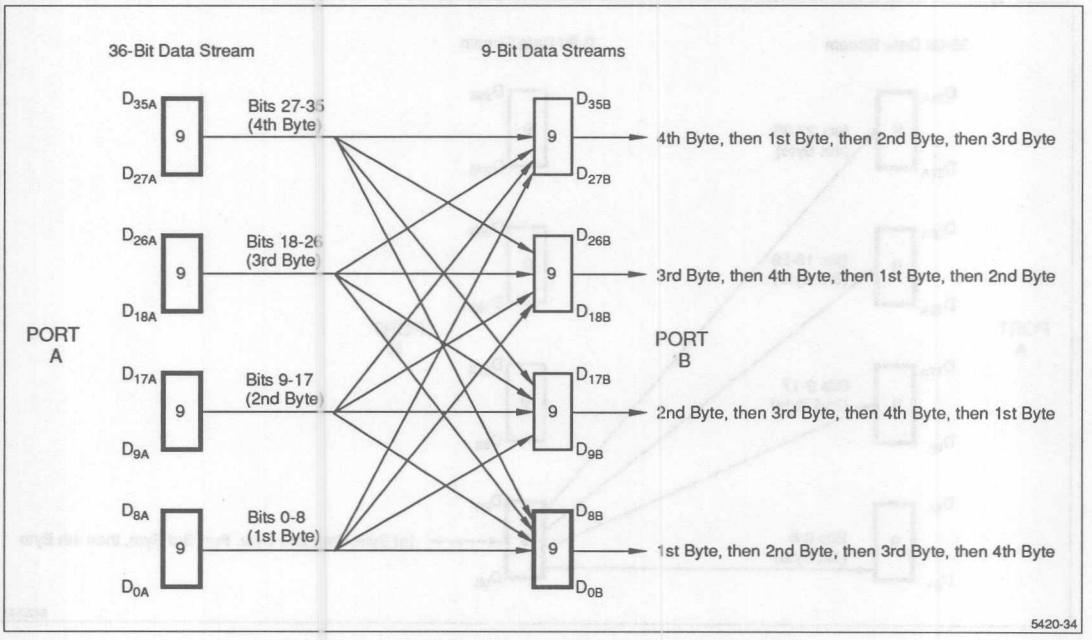


Figure 6b. 36-to-9 Funneling Through FIFO #1

NOTES:

1. The heavy black borders on register segments indicate the main data path, suitable for most applications. Alternate paths feature a different ordering of bytes within a word, at Port B.
2. The funneling process does not change the ordering of bits within a byte. Halfwords (Figure 6a) or bytes (Figure 6b) are transferred in parallel form from Port A to Port B.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attempting to read $D_{0B} - D_{35B}$. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO.

PORT B WORD-WIDTH SELECTION

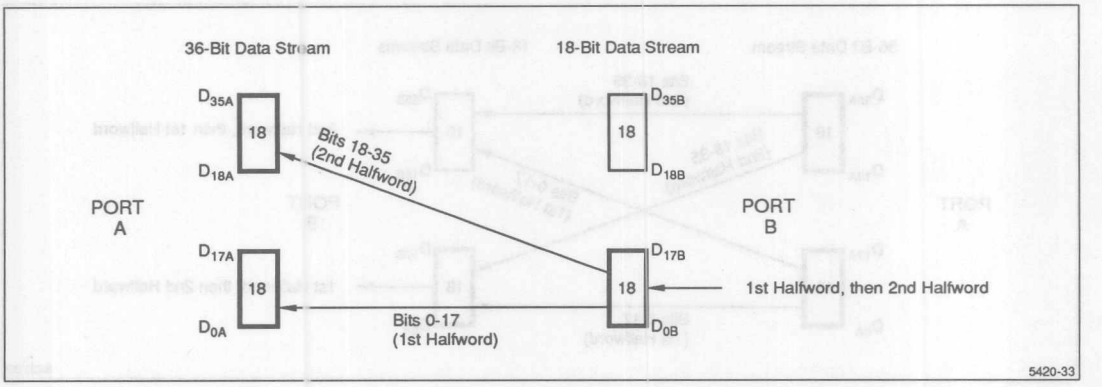


Figure 7a. 18-to-36 Defunneling Through FIFO #2

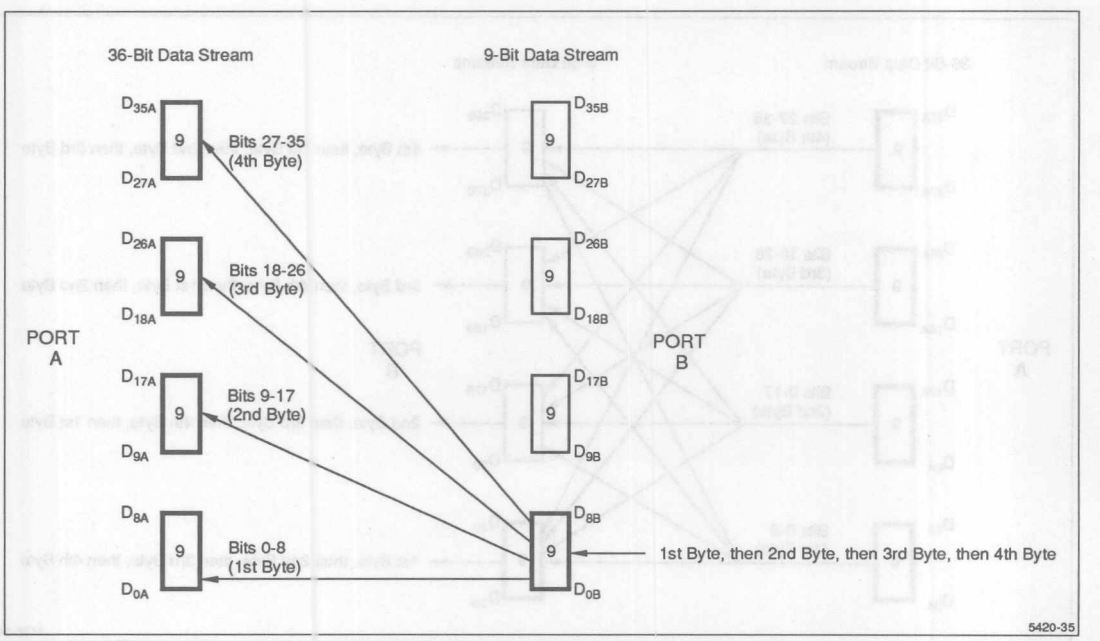
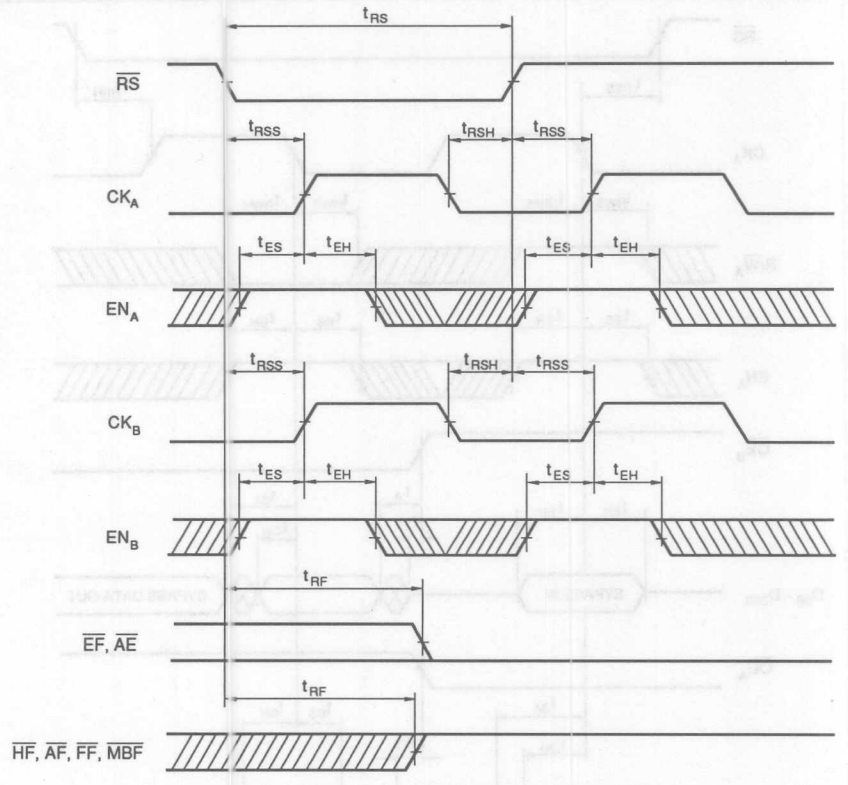


Figure 7b. 9-to-36 Defunneling Through FIFO #2

NOTES:

1. The heavy black borders on register segments indicate the only data paths used. The other byte segments of Port B do not participate in the data path during defunneling.
2. The defunneling process does not change the ordering of bits within a byte. Halfwords (Figure 7a) or bytes (Figure 7b) are transferred in parallel form from Port B to Port A.
3. The word-width setting may be changed during system operation; however, two clock intervals should be allowed for these signals to settle, before again attempting to send data. Also, incomplete data words may occur when the word width is changed from shorter to longer, at an inappropriate point in the data block passing through the FIFO.

TIMING DIAGRAMS



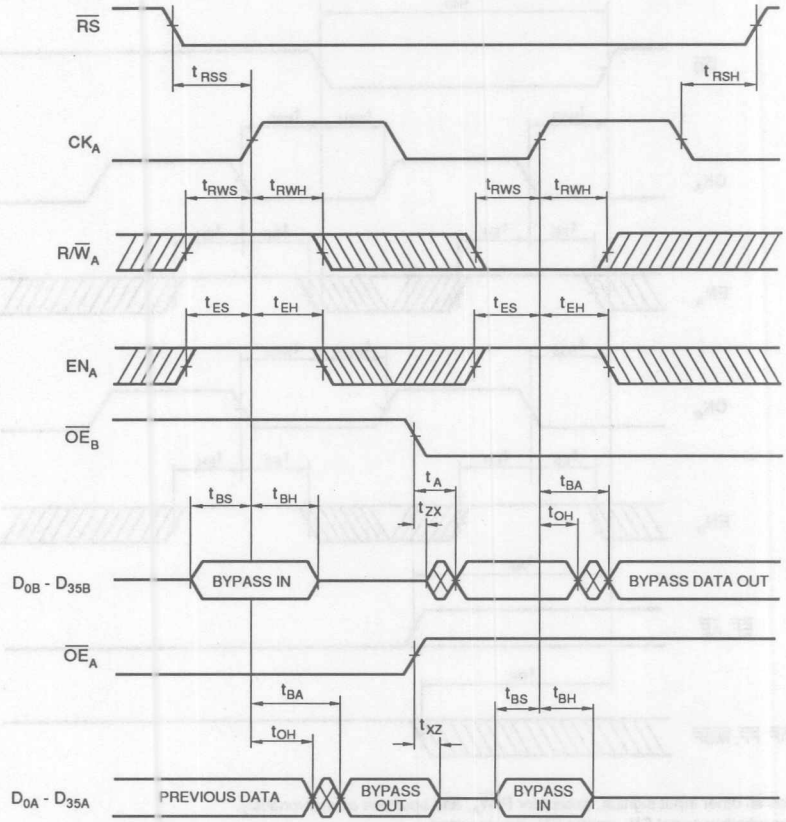
NOTES:

1. $\overline{RS}$ overrides all other input signals, except for $R/\overline{W}_A$, and operates asynchronously. $\overline{RS}$ operates whether or not EN_A and/or EN_B are asserted.
2. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A and/or CK_B occurs while that clock is enabled.
3. The parity check is initialized to odd byte parity at reset.
4. The $\overline{AE}$ and $\overline{AF}$ flag offsets are initialized to eight locations from the boundary at reset.

5420-26

Figure 8. Reset Timing

TIMING DIAGRAMS (cont'd)



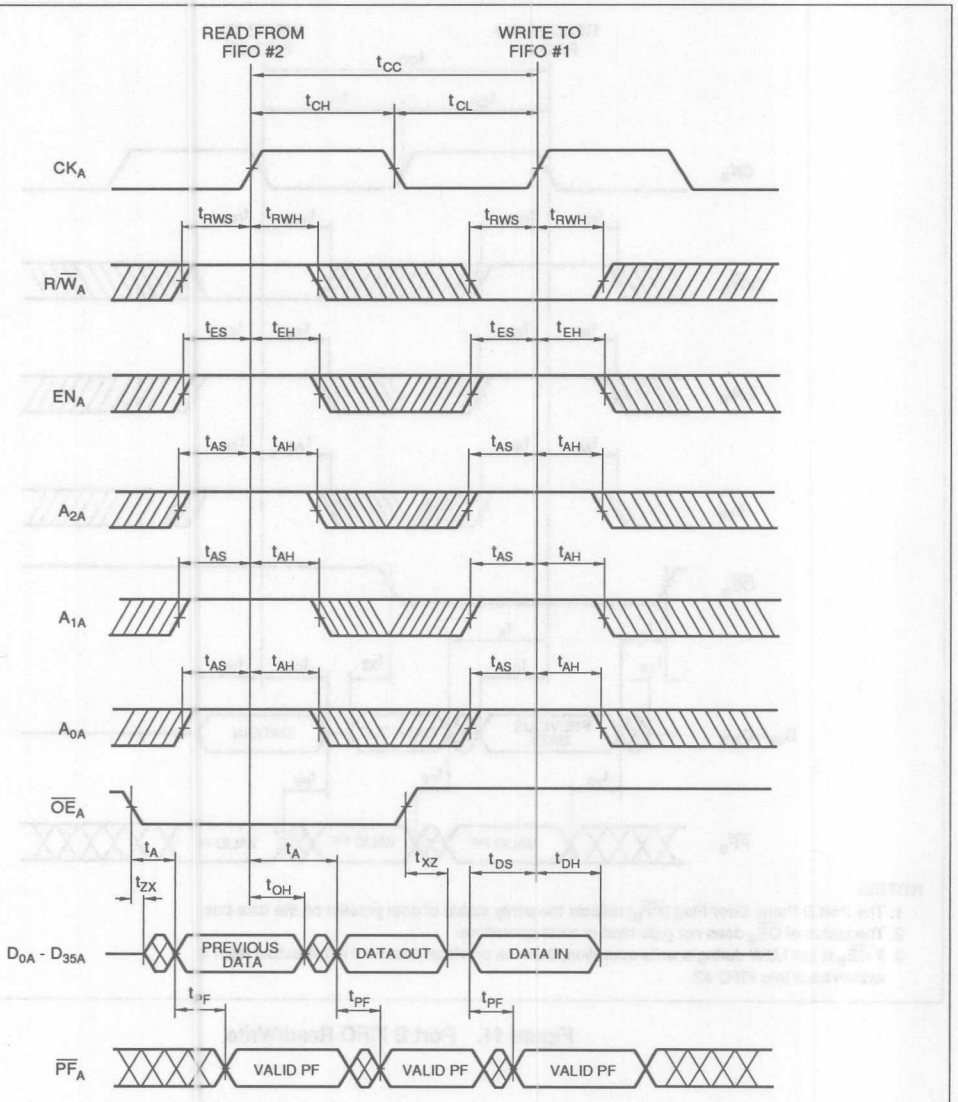
NOTES:

1. t_{RSS}, t_{RSH} need not be met unless the rising edge of CK_A or CK_B occurs while that clock is enabled.
2. Port A is considered the master port for bypass operation. Thus, CK_A, $R/\overline{W}_A$, and EN_A control the transmission of data between ports at reset.

5420-27

Figure 9. Data Bypass Timing

TIMING DIAGRAMS (cont'd)



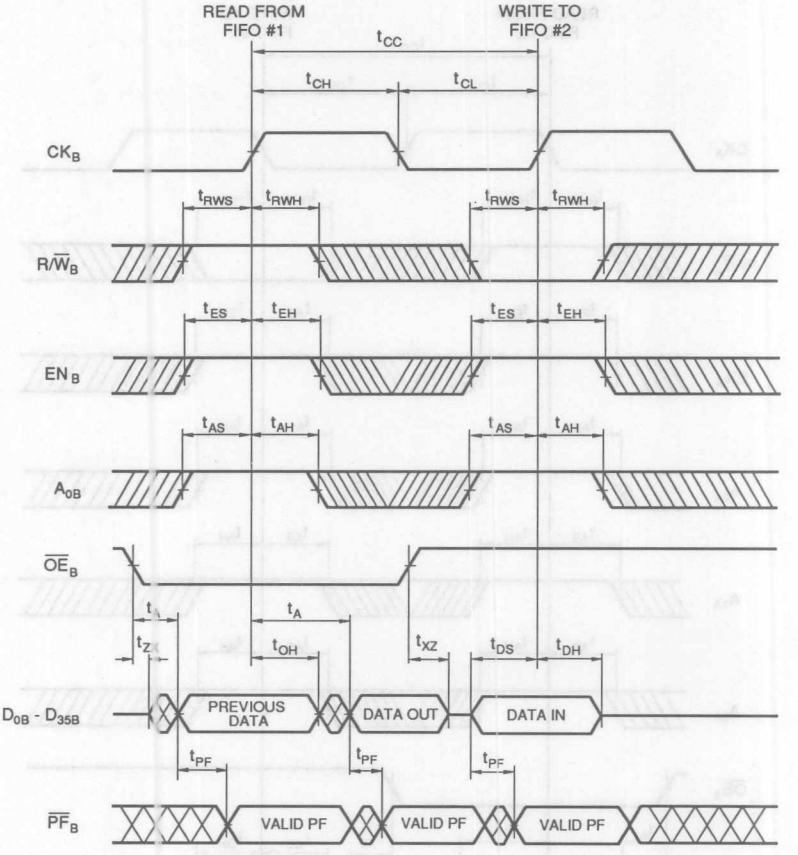
NOTES:

1. The Port A Parity Error Flag ($\overline{PF}_A$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_A$ does not gate read or write operations.
3. If $\overline{OE}_A$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #1.

5420-24

Figure 10. Port A FIFO Read/Write

TIMING DIAGRAMS (cont'd)



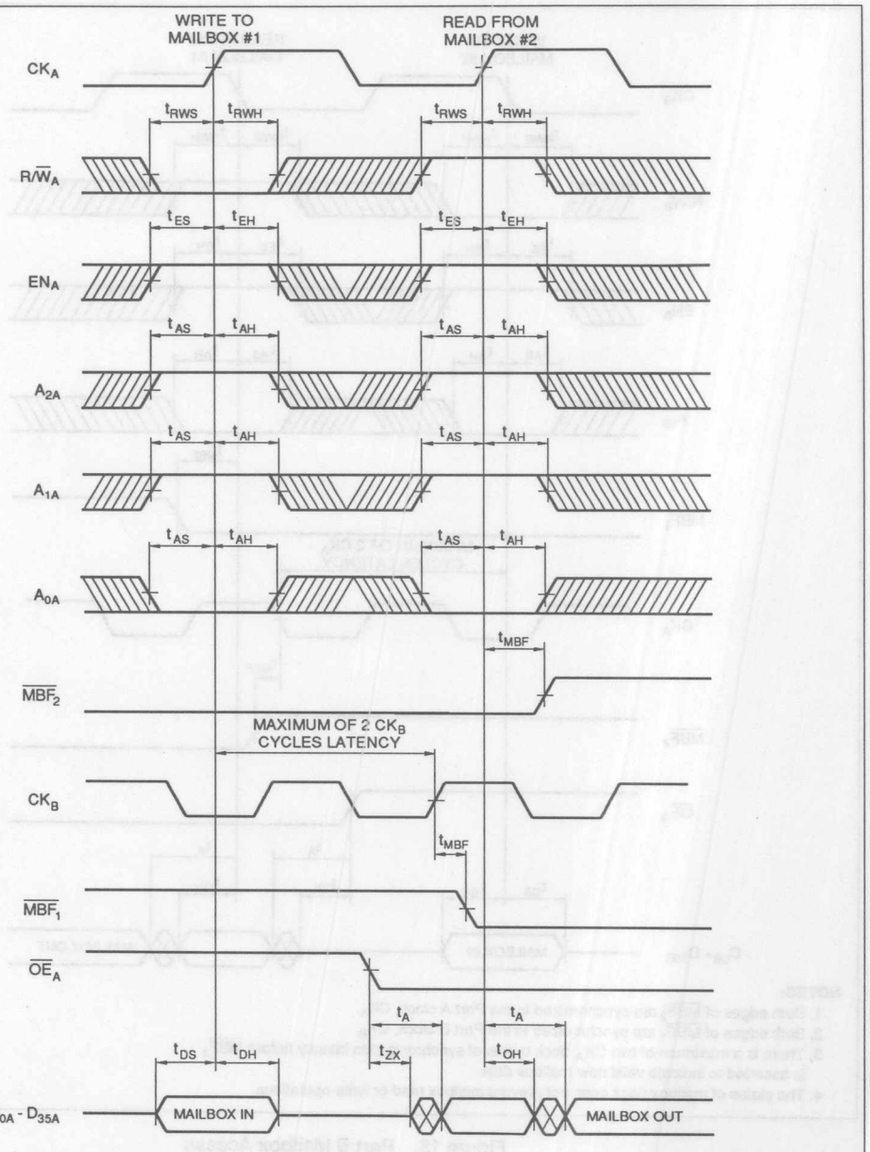
NOTES:

1. The Port B Parity Error Flag ($\overline{PF}_B$) reflects the parity status of data present on the data bus.
2. The status of $\overline{OE}_B$ does not gate read or write operations.
3. If $\overline{OE}_B$ is left LOW during a write operation, then the previous data held in the output latch is written back into FIFO #2.

5420-25

Figure 11. Port B FIFO Read/Write

TIMING DIAGRAMS (cont'd)



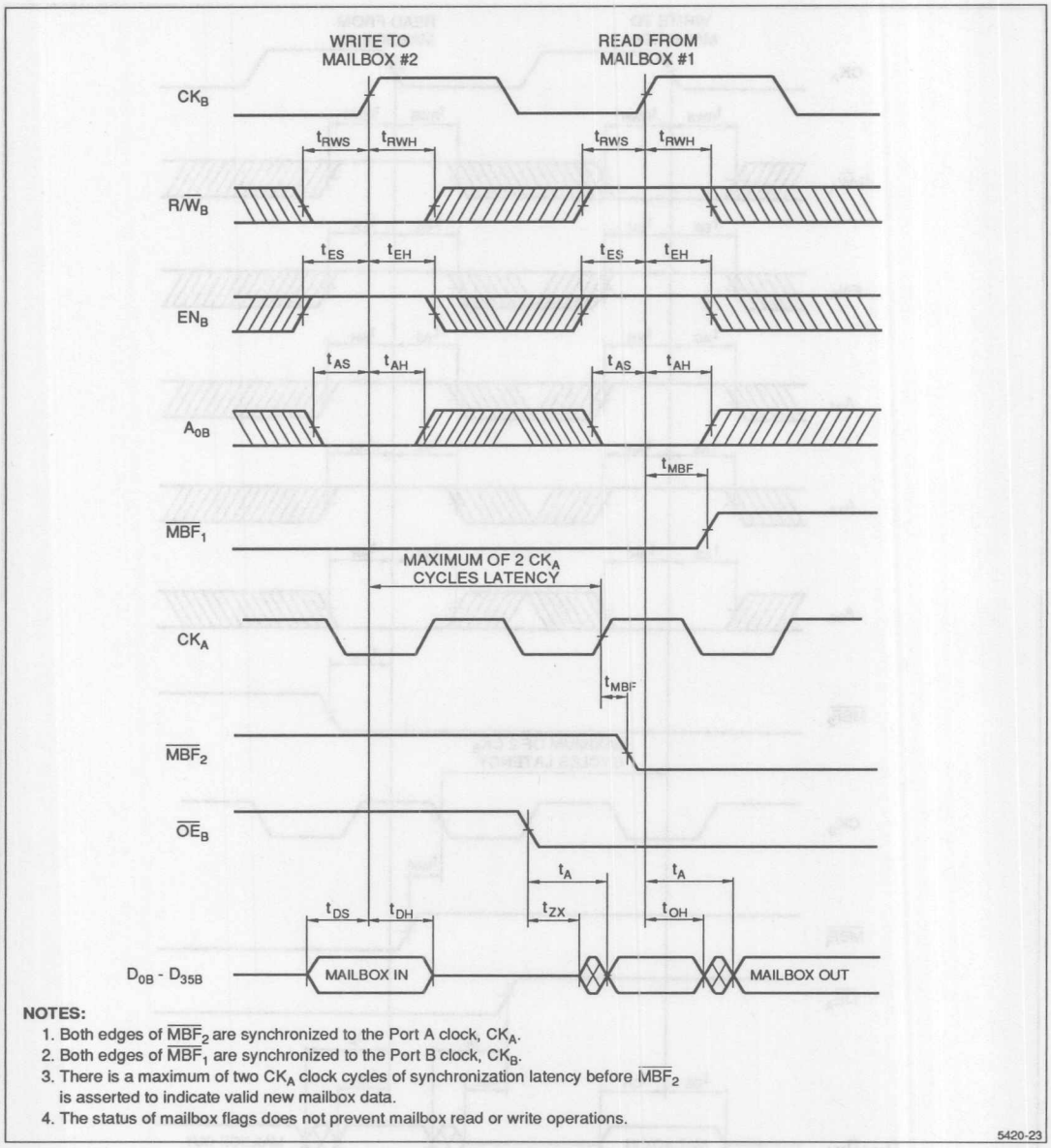
NOTES:

1. Both edges of $\overline{MBF_2}$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF_1}$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of two CK_B clock cycles of synchronization latency before $\overline{MBF_1}$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.

5420-22

Figure 12. Port A Mailbox Access

TIMING DIAGRAMS (cont'd)



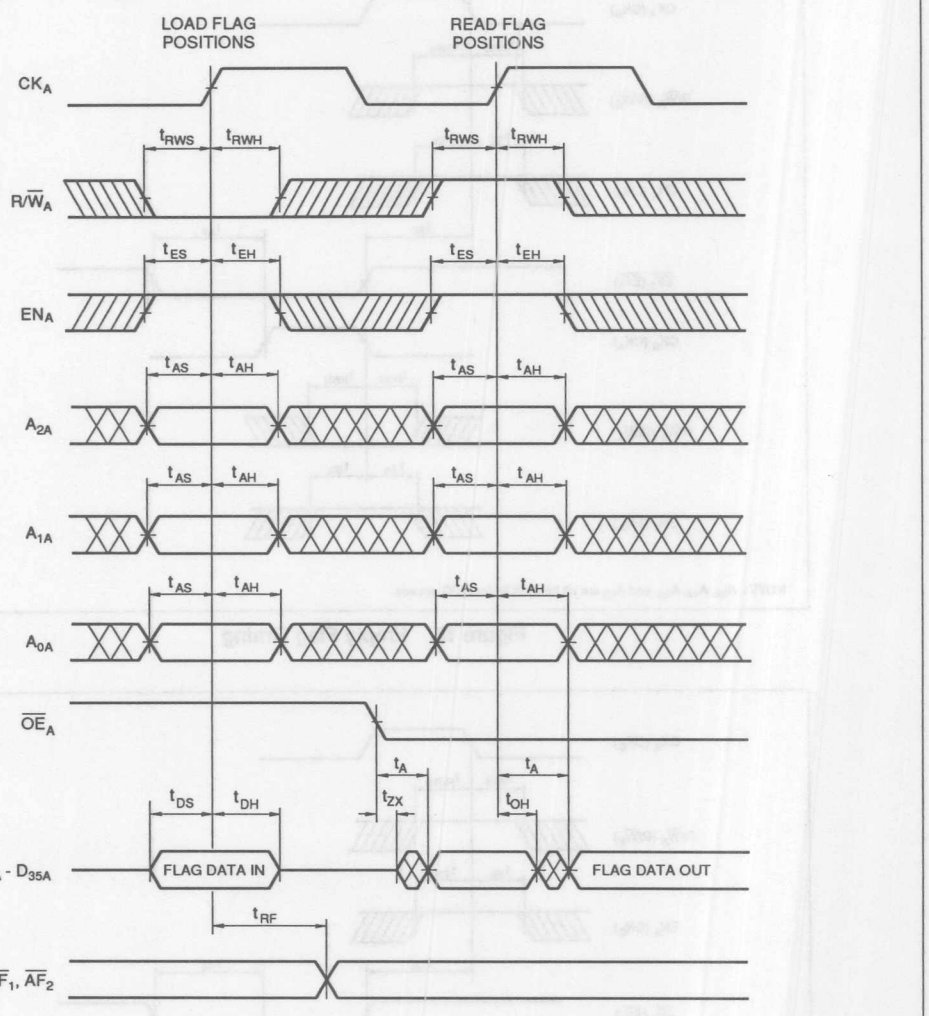
NOTES:

1. Both edges of $\overline{MBF}_2$ are synchronized to the Port A clock, CK_A.
2. Both edges of $\overline{MBF}_1$ are synchronized to the Port B clock, CK_B.
3. There is a maximum of two CK_A clock cycles of synchronization latency before $\overline{MBF}_2$ is asserted to indicate valid new mailbox data.
4. The status of mailbox flags does not prevent mailbox read or write operations.

5420-23

Figure 13. Port B Mailbox Access

TIMING DIAGRAMS (cont'd)



NOTES:

1. For valid flag address codes and data formats, see Table 3.
2. If flag status is altered by flag programming, the updated flags will be valid within a time t_{RF}.

5420-18

Figure 14. Flag Programming

TIMING DIAGRAMS (cont'd)

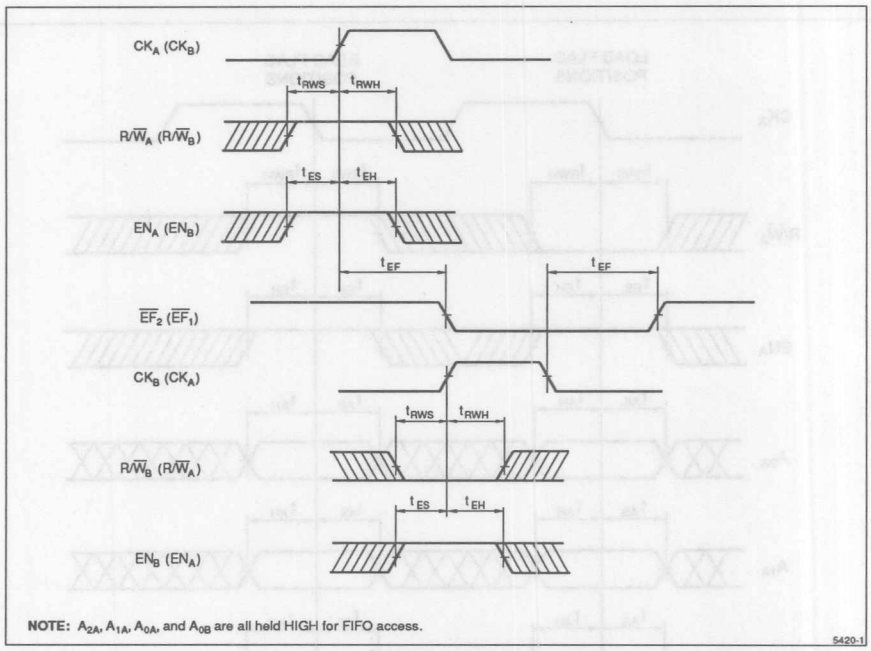


Figure 15. Empty Flag Timing

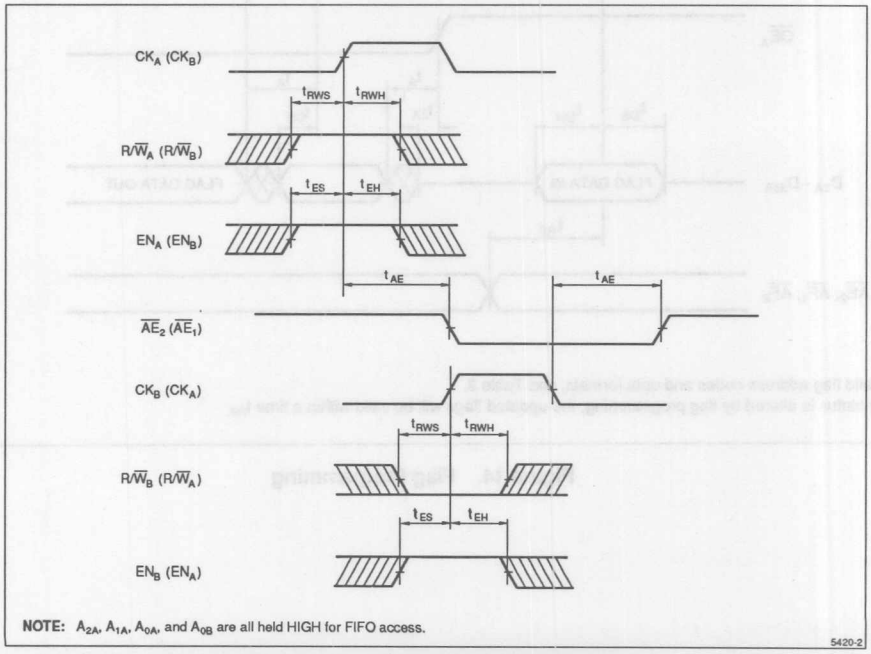


Figure 16. Almost-Empty Flag Timing

TIMING DIAGRAMS (cont'd)

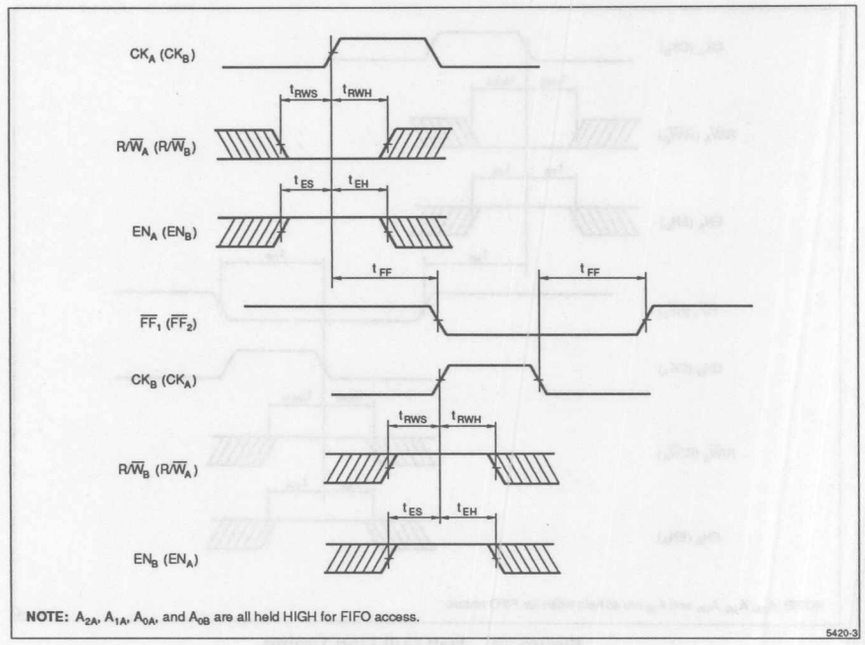


Figure 17. Full Flag Timing

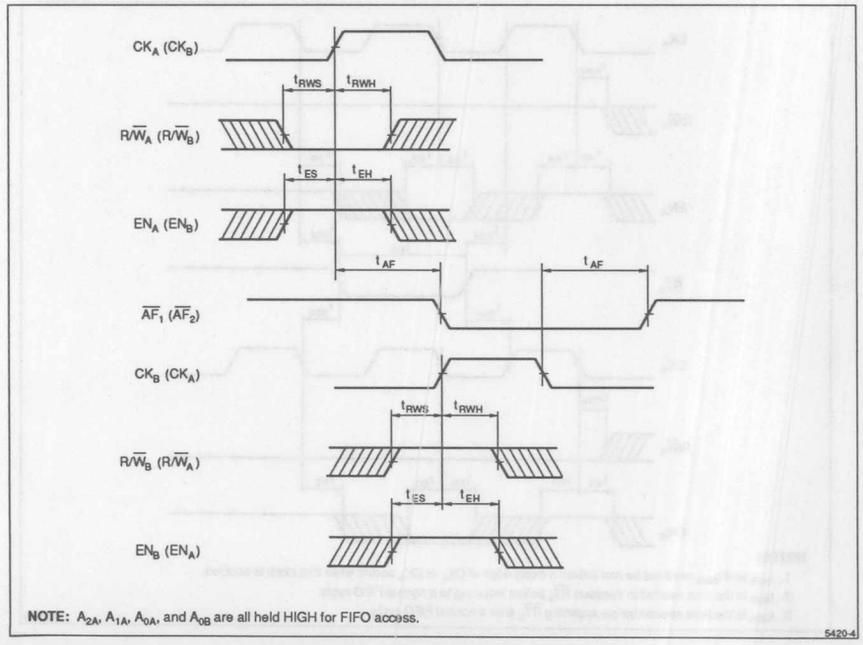
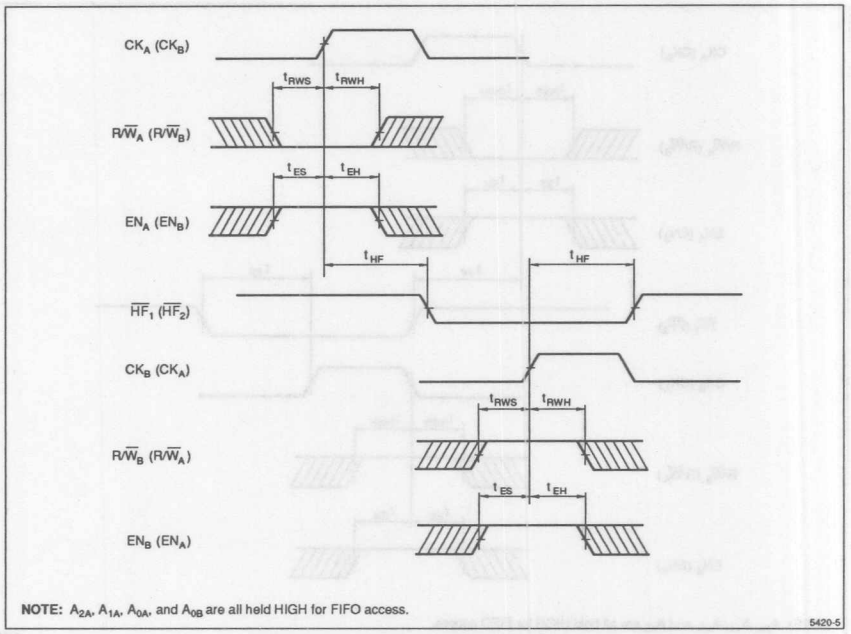


Figure 18. Almost-Full Flag Timing

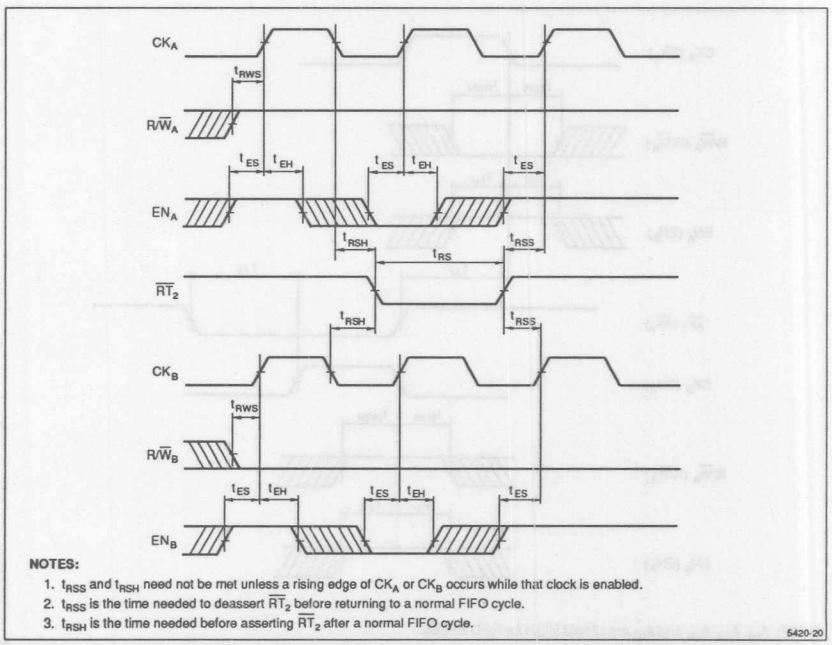
TIMING DIAGRAMS (cont'd)



NOTE: A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.

5420-5

Figure 19. Half-Full Flag Timing



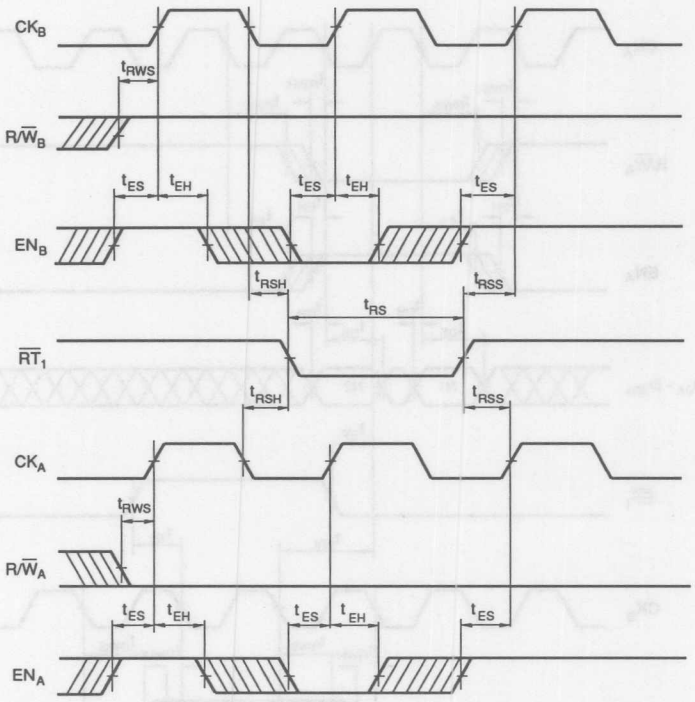
NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_2$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_2$ after a normal FIFO cycle.

5420-20

Figure 20. FIFO #2 Retransmit

TIMING DIAGRAMS (cont'd)



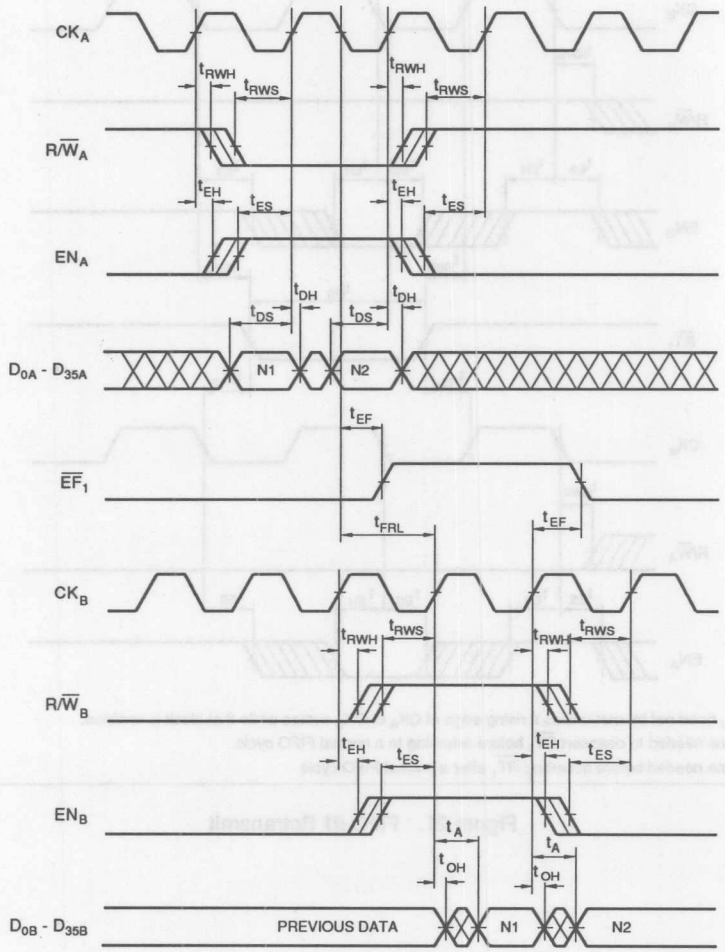
NOTES:

1. t_{RSS} and t_{RSH} need not be met unless a rising edge of CK_A or CK_B occurs while that clock is enabled.
2. t_{RSS} is the time needed to deassert $\overline{RT}_1$ before returning to a normal FIFO cycle.
3. t_{RSH} is the time needed before asserting $\overline{RT}_1$ after a normal FIFO cycle.

5420-21

Figure 21. FIFO #1 Retransmit

TIMING DIAGRAMS (cont'd)



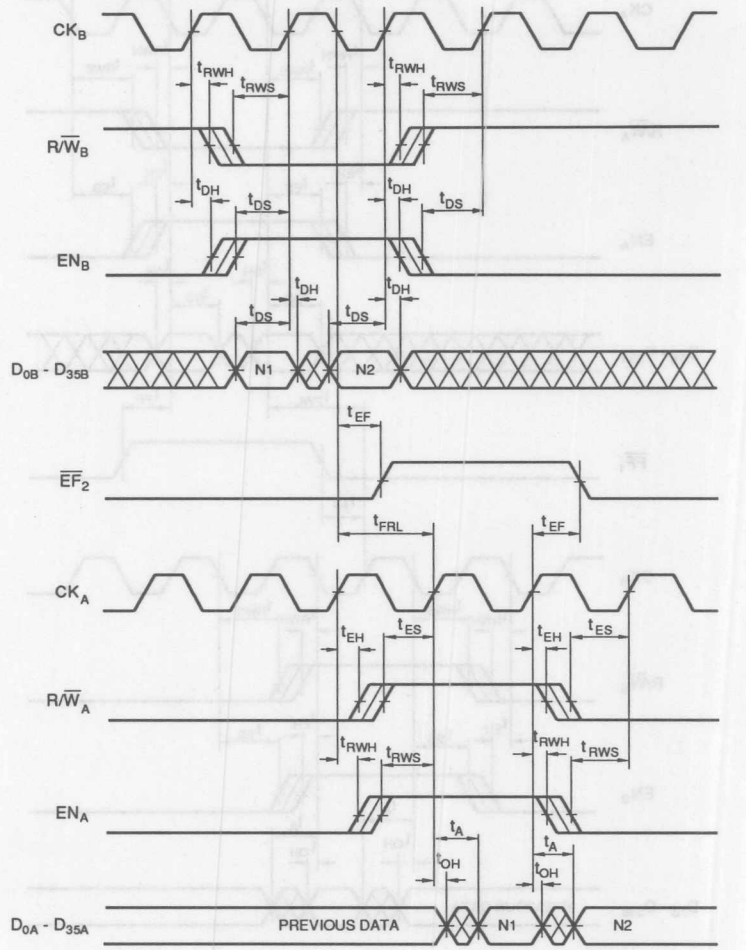
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

5420-16

Figure 22. FIFO #1 Write and Read Operation in Near-Empty Region

TIMING DIAGRAMS (cont'd)



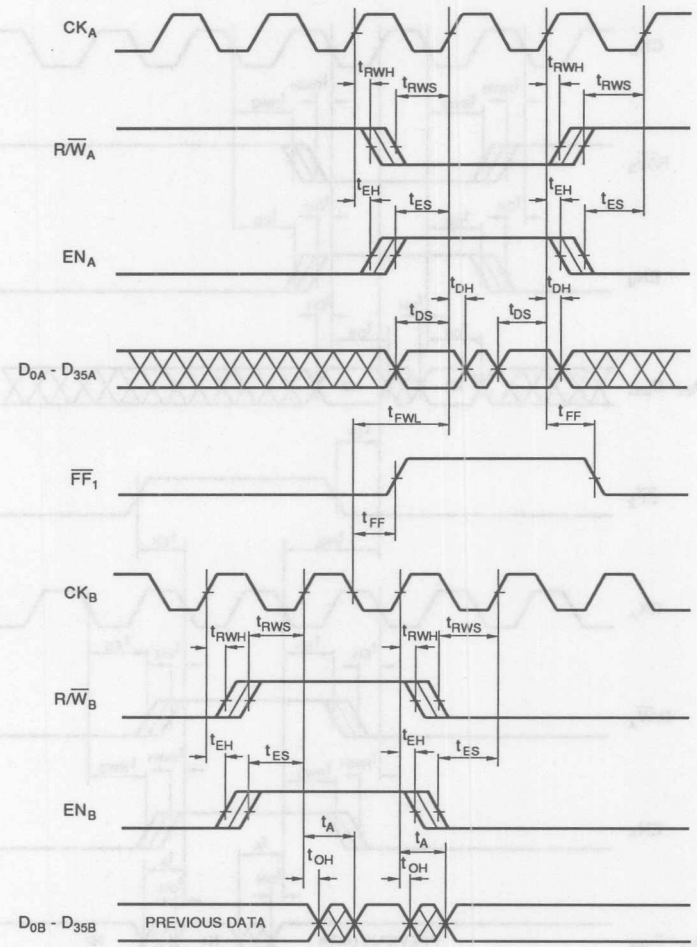
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FRL} (First Read Latency) - The first read following an empty condition may begin no earlier than t_{FRL} after the first write to an empty FIFO, to ensure that valid read data is retrieved.

5420-17

Figure 23. FIFO #2 Write and Read Operation in Near-Empty Region

TIMING DIAGRAMS (cont'd)



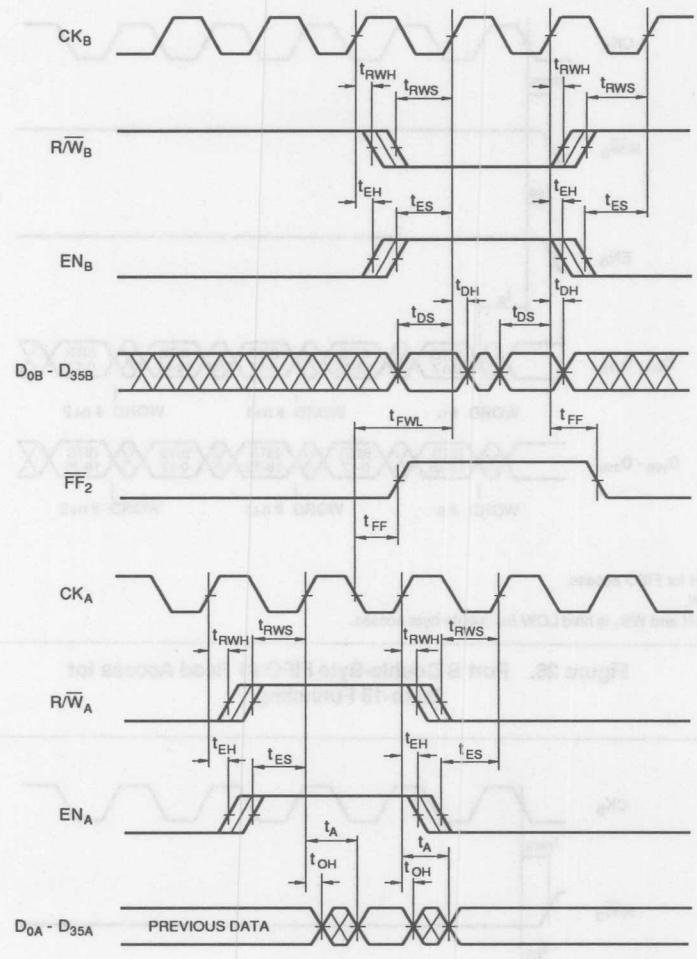
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held HIGH.
3. $\overline{OE}_B$ is held LOW.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

5420-14

Figure 24. FIFO #1 Read and Write Operation in Near-Full Region

TIMING DIAGRAMS (cont'd)



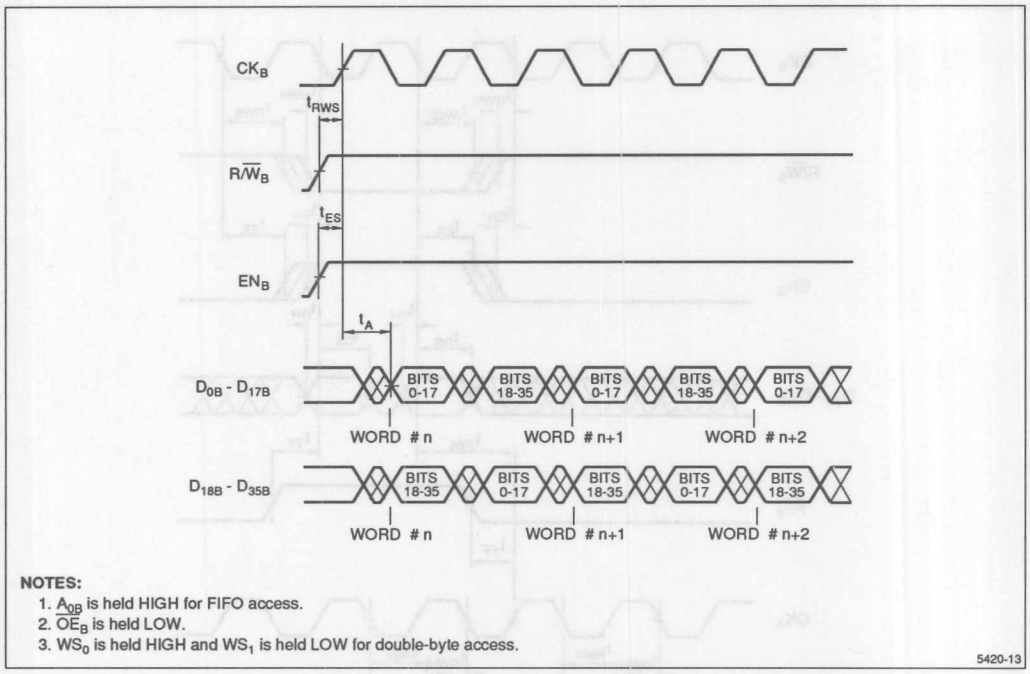
NOTES:

1. A_{2A}, A_{1A}, A_{0A}, and A_{0B} are all held HIGH for FIFO access.
2. $\overline{OE}_A$ is held LOW.
3. $\overline{OE}_B$ is held HIGH.
4. t_{FWL} (First Write Latency) - The first write following a full condition may begin no earlier than t_{FWL} after the first read from a full FIFO, to ensure that valid write data is written.

5420-15

Figure 25. FIFO #2 Read and Write Operation in Near-Full Region

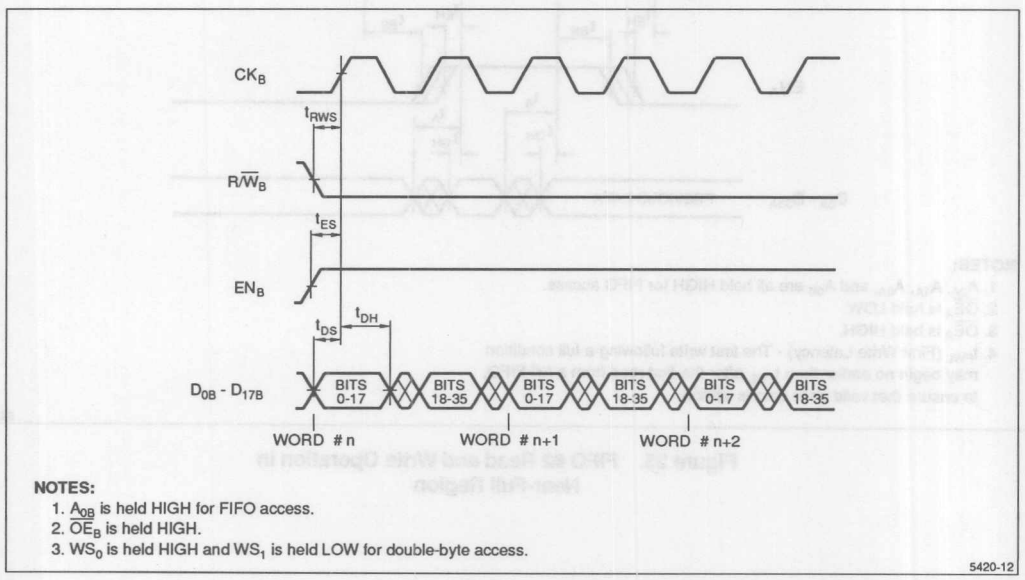
TIMING DIAGRAMS (cont'd)



NOTES:
1. $\overline{A_{0B}}$ is held HIGH for FIFO access.
2. $\overline{OE_B}$ is held LOW.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.

5420-13

Figure 26. Port B Double-Byte FIFO #1 Read Access for 36-to-18 Funneling

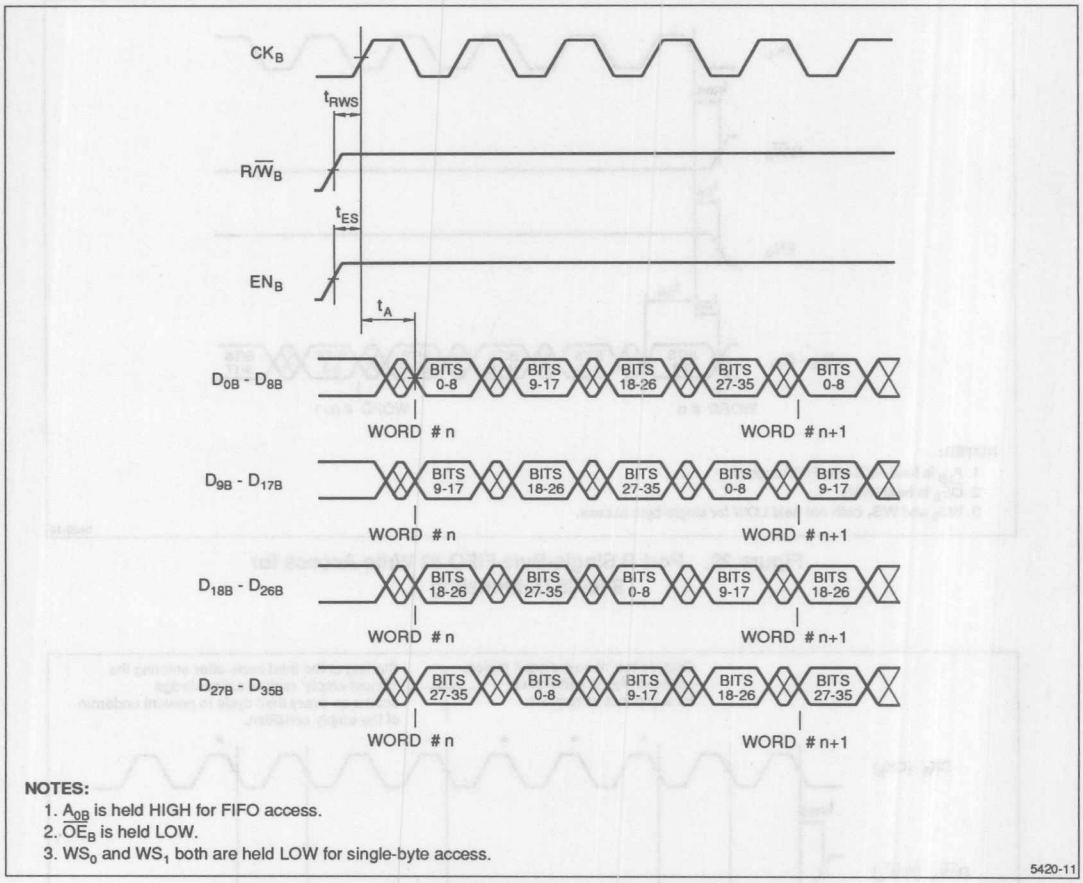


NOTES:
1. $\overline{A_{0B}}$ is held HIGH for FIFO access.
2. $\overline{OE_B}$ is held HIGH.
3. WS_0 is held HIGH and WS_1 is held LOW for double-byte access.

5420-12

Figure 27. Port B Double-Byte FIFO #2 Write Access for 18-to-36 Defunneling

TIMING DIAGRAMS (cont'd)

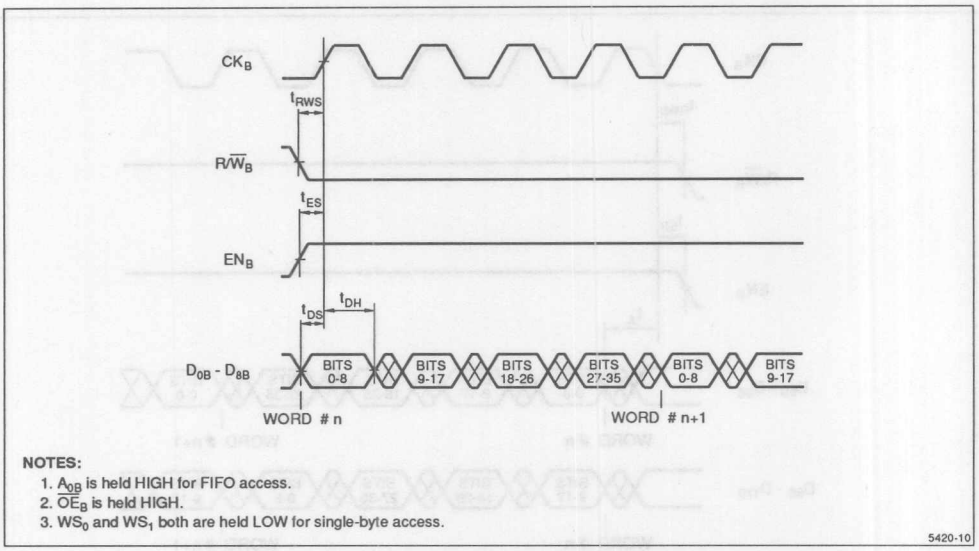


NOTES:
1. $\overline{A_{0B}}$ is held HIGH for FIFO access.
2. $\overline{OE_B}$ is held LOW.
3. WS_0 and WS_1 both are held LOW for single-byte access.

5420-11

Figure 28. Port B Single-Byte FIFO #1 Read Access for 36-to-9 Funneling

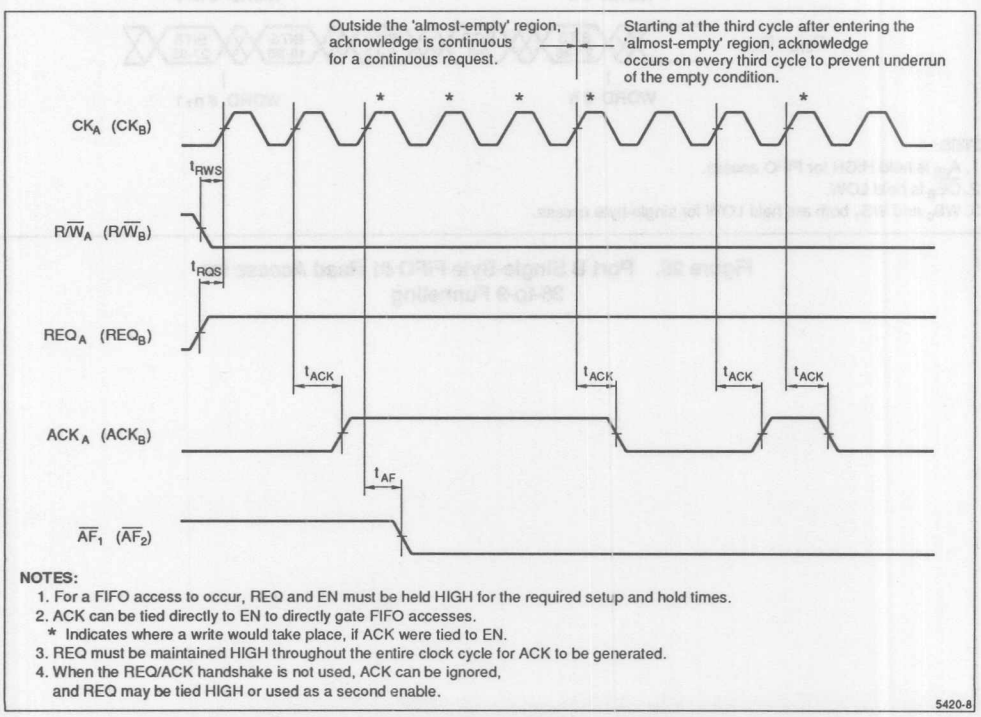
TIMING DIAGRAMS (cont'd)



NOTES:
1. A_{0B} is held HIGH for FIFO access.
2. $\overline{OE}_B$ is held HIGH.
3. WS_0 and WS_1 both are held LOW for single-byte access.

5420-10

Figure 29. Port B Single-Byte FIFO #2 Write Access for 9-to-36 Defunneling

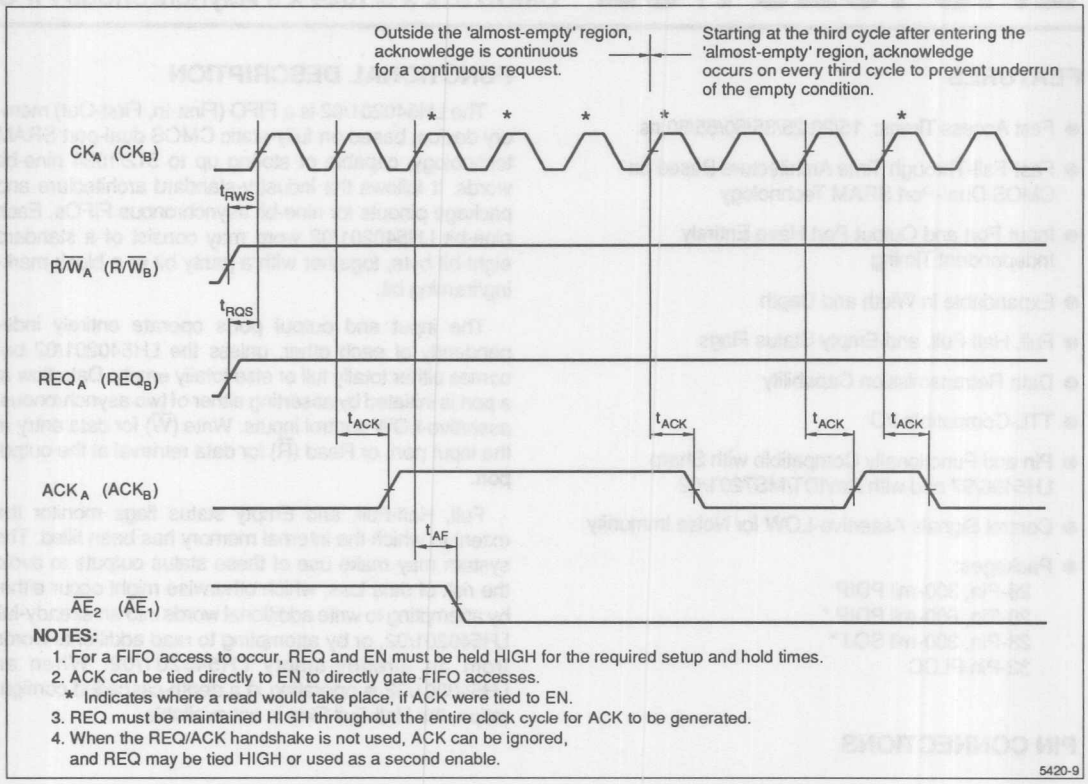


NOTES:
1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a write would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.

5420-8

Figure 30. Write Request/Acknowledge Handshake

TIMING DIAGRAMS (cont'd)



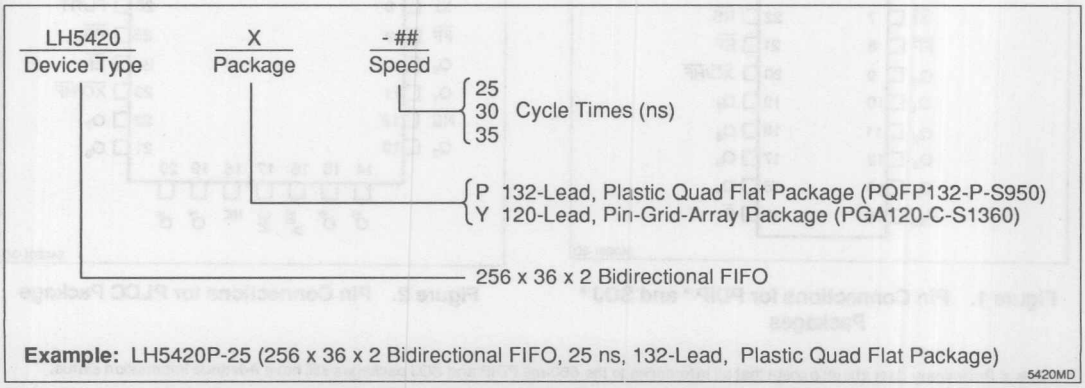
NOTES:

1. For a FIFO access to occur, REQ and EN must be held HIGH for the required setup and hold times.
2. ACK can be tied directly to EN to directly gate FIFO accesses.
   * Indicates where a read would take place, if ACK were tied to EN.
3. REQ must be maintained HIGH throughout the entire clock cycle for ACK to be generated.
4. When the REQ/ACK handshake is not used, ACK can be ignored, and REQ may be tied HIGH or used as a second enable.

5420-9

Figure 31. Read Request/Acknowledge Handshake

ORDERING INFORMATION



Example: LH5420P-25 (256 x 36 x 2 Bidirectional FIFO, 25 ns, 132-Lead, Plastic Quad Flat Package)

5420MD

LH540201/02

PRELIMINARY

CMOS 512 × 9/1024 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 15/20/25/35/50/65/80 ns
- Fast-Fall-Through Time Architecture Based on CMOS Dual-Port SRAM Technology
- Input Port and Output Port Have Entirely Independent Timing
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Data Retransmission Capability
- TTL-Compatible I/O
- Pin and Functionally Compatible with Sharp LH5496/97 and with Am/IDT/MS7201/02
- Control Signals Assertive-LOW for Noise Immunity
- Packages:
  - 28-Pin, 300-mil PDIP
  - 28-Pin, 600-mil PDIP *
  - 28-Pin, 300-mil SOJ *
  - 32-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH540201/02 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 512/1024 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit LH540201/02 word may consist of a standard eight-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the LH540201/02 becomes either totally full or else totally empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full LH540201/02, or by attempting to read additional words from an already-empty LH540201/02. When an LH540201/02 is operating in a depth-cascaded configuration, the Half-Full Flag is not available.

PIN CONNECTIONS

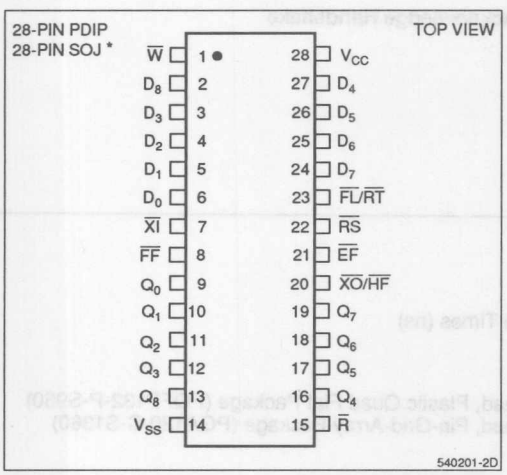


Figure 1. Pin Connections for PDIP * and SOJ * Packages

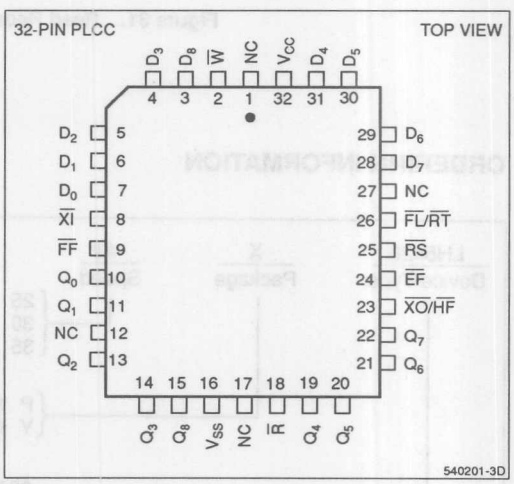


Figure 2. Pin Connections for PLCC Package

* This is a Preliminary data sheet; except that all references to the 600-mil PDIP and SOJ packages still have Advance Information status.

FUNCTIONAL DESCRIPTION (cont'd)

Data words are read out from the LH540201/02's output port in precisely the same order that they were written in at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the LH540201/02 device.

Drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO-memory-array read-address pointer to be set back to zero, to point to the LH540201/02's first physical memory location, without affecting the internal FIFO-memory-array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address-pointer value, may be read out *repeatedly* an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an LH540201/02 is operating in a depth-expanded configuration.

The Reset ($\overline{RS}$) control signal returns the LH540201/02 to an initial state, empty and ready to be filled. An LH540201/02 should be reset during every system power-up sequence. A reset operation causes the internal FIFO-memory-array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the LH540201/02's first physical memory location. Any information which previously had been stored within the LH540201/02 is not recoverable after a reset operation.

A cascading (depth-expansion) scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}/\overline{HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual LH540201/02 devices, without incurring additional latency ('fallthrough' or 'bubble-through') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one LH540201/02 device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL}/\overline{RT}$) control input; the remaining LH540201/02 devices are designated as 'slaves,' by tying their $\overline{FL}/\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' LH540201/02 devices operating in cascaded mode.

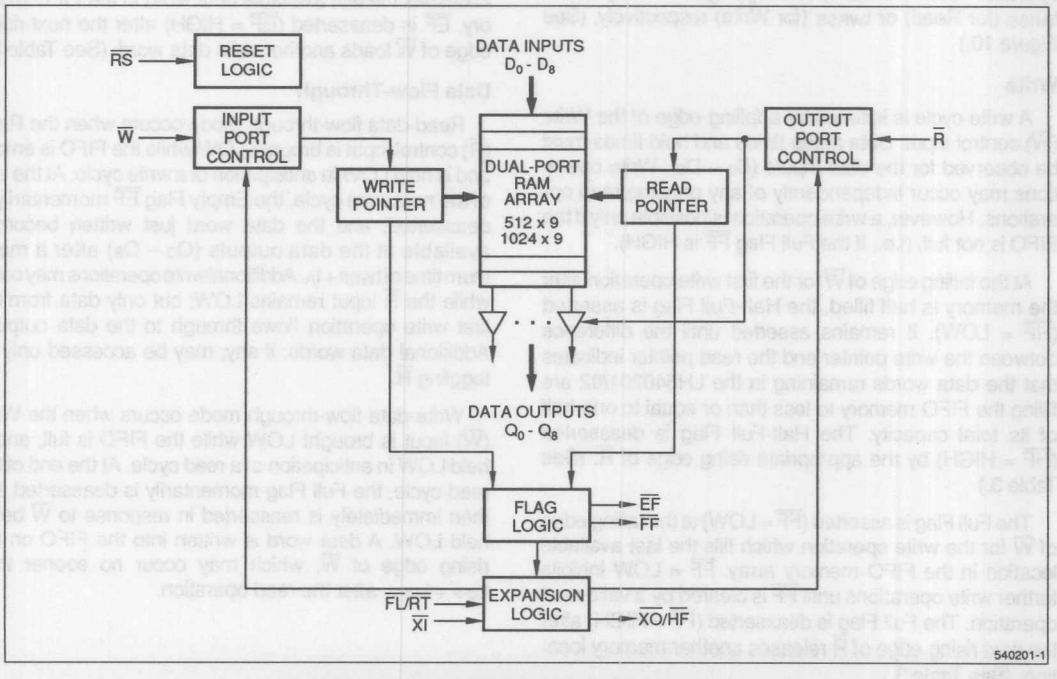


Figure 3. LH540201/02 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

OPERATIONAL DESCRIPTION

Reset

The LH540201/02 is reset whenever the Reset input ($\overline{RS}$) is taken LOW. A reset operation initializes both the read-address pointer and the write-address pointer to point to location zero, the first physical memory location. During a reset operation, the state of the $\overline{XI}$ and $\overline{FL}/\overline{RT}$ inputs determines whether the device is in standalone mode or in depth-cascaded mode. (See Tables 1 and 2.)

A reset operation is required whenever the LH540201/02 first is powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) inputs may be in any state when the reset operation is initiated; but they must be HIGH, before the reset operation is terminated by a rising edge of $\overline{RS}$, by a time t_{RRSS} (for Read) or t_{WRSS} (for Write) respectively. (See Figure 10.)

Write

A write cycle is initiated by a falling edge of the Write ($\overline{W}$) control input. Data setup times and hold times must be observed for the data inputs ($D_0 - D_8$). Write operations may occur independently of any ongoing read operations. However, a write operation is possible only if the FIFO is not full, (i.e., if the Full Flag $\overline{FF}$ is HIGH).

At the falling edge of $\overline{W}$ for the first write operation after the memory is half filled, the Half-Full Flag is asserted ($\overline{HF}$ = LOW). It remains asserted until the difference between the write pointer and the read pointer indicates that the data words remaining in the LH540201/02 are filling the FIFO memory to less than or equal to one-half of its total capacity. The Half-Full Flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$. (See Table 3.)

The Full Flag is asserted ($\overline{FF}$ = LOW) at the falling edge of $\overline{W}$ for the write operation which fills the last available location in the FIFO memory array. $\overline{FF}$ = LOW inhibits further write operations until $\overline{FF}$ is cleared by a valid read operation. The Full Flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location. (See Table 3.)

Read

A read cycle is initiated by a falling edge of the Read ($\overline{R}$) control input. Read data becomes valid at the data outputs ($Q_0 - Q_8$) after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data outputs return to a high-impedance state. Read operations may occur independently of any ongoing write operations. However, a read operation is possible only if the FIFO is not empty (i.e., if the Empty Flag $\overline{EF}$ is HIGH).

The LH540201/02's internal read-address and write-address pointers operate in such a way that consecutive read operations always access data words in the same order that they were written. The Empty Flag is asserted ($\overline{EF}$ = LOW) after that falling edge of $\overline{R}$ which accesses the last available data word in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another valid data word. (See Table 3.)

Data Flow-Through

Read-data flow-through mode occurs when the Read ($\overline{R}$) control input is brought LOW while the FIFO is empty, and is held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty Flag $\overline{EF}$ momentarily is deasserted, and the data word just written becomes available at the data outputs ($Q_0 - Q_8$) after a maximum time of $t_{WEF} + t_A$. Additional write operations may occur while the $\overline{R}$ input remains LOW; but only data from the first write operation flows through to the data outputs. Additional data words, if any, may be accessed only by toggling $\overline{R}$.

Write-data flow-through mode occurs when the Write ($\overline{W}$) input is brought LOW while the FIFO is full, and is held LOW in anticipation of a read cycle. At the end of the read cycle, the Full Flag momentarily is deasserted, but then immediately is reasserted in response to $\overline{W}$ being held LOW. A data word is written into the FIFO on the rising edge of $\overline{W}$, which may occur no sooner than $t_{RFF} + t_{WPW}$ after the read operation.

OPERATIONAL DESCRIPTION (cont'd)

Retransmit

The FIFO can be made to reread previously-read data by means of the Retransmit function. A retransmit operation is initiated by pulsing the $\overline{RT}$ input LOW. Both $\overline{R}$ and $\overline{W}$ must be deasserted (HIGH) for the duration of the retransmit pulse. The FIFO's internal read-address pointer is reset to point to location zero, the first physical memory location, while the internal write-address pointer remains unchanged.

After a retransmit operation, those data words in the region in between the read-address pointer and the write-address pointer may be reaccessed by subsequent read operations. A retransmit operation may affect the state of the status flags $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$, depending on the relocation of the read-address pointer. There is no restriction on the number of times that a block of data within an LH540201/02 may be read out, by repeating the retransmit operation and the subsequent read operations.

The maximum length of a data block which may be retransmitted is 512/1024 words. Note that if the write-address pointer ever 'wraps around' (i.e., passes location zero more than once) during a sequence of retransmit operations, some data words will be lost.

The Retransmit function is not available when the LH540201/02 is operating in depth-cascaded mode, because the $\overline{FL}/\overline{RT}$ control pin must be used for first-load selection rather than for retransmission control.

Table 1. Grouping-Mode Determination During a Reset Operation

$\overline{XI}$	$\overline{FL}/\overline{RT}$	MODE	$\overline{XO}/\overline{HF}$ USAGE	$\overline{XI}$ USAGE	$\overline{FL}/\overline{RT}$ USAGE
H [1]	H	Cascaded Slave [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
H [1]	L	Cascaded Master [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
L	X	Standalone	$\overline{HF}$	(none)	$\overline{RT}$

NOTES:
1. A reset operation forces $\overline{XO}$ HIGH for the nth FIFO, thus forcing $\overline{XI}$ HIGH for the n+1st FIFO.
2. The terms 'master' and 'slave' refer to operation in depth-cascaded grouping mode.
3. H = HIGH; L = LOW; X = Don't Care.

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	STANDALONE	CASCADED MASTER	CASCADED SLAVE
I	$\overline{XI}$	Grounded	From $\overline{XO}$ (n-1st FIFO)	From $\overline{XO}$ (n-1st FIFO)
O	$\overline{XO}/\overline{HF}$	Becomes $\overline{HF}$	To $\overline{XI}$ (n+1st FIFO)	To $\overline{XI}$ (n+1st FIFO)
I	$\overline{FL}/\overline{RT}$	Becomes $\overline{RT}$	Grounded (Logic LOW)	Logic HIGH

Table 3. Status Flags

LH540201				LH540202			
NUMBER OF UNREAD DATA WORDS PRESENT WITHIN 512 × 9 FIFO	$\overline{FF}$	$\overline{HF}$	$\overline{EF}$	NUMBER OF UNREAD DATA WORDS PRESENT WITHIN 1024 × 9 FIFO	$\overline{FF}$	$\overline{HF}$	$\overline{EF}$
0	H	H	L	0	H	H	L
1 to 256	H	H	H	1 to 512	H	H	H
257 to 511	H	L	H	513 to 1023	H	L	H
512	L	L	H	1024	L	L	H

OPERATIONAL MODES

Standalone Configuration

When depth cascading is not required for a given application, the LH540201/02 is placed in standalone mode by tying the Expansion In input ($\overline{XI}$) to ground. This input is internally sampled during a reset operation. (See Table 1.)

Width Expansion

Word-width expansion is implemented by placing multiple LH540201/02 devices in parallel. Each LH540201/02 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 4, 5, and 6.)

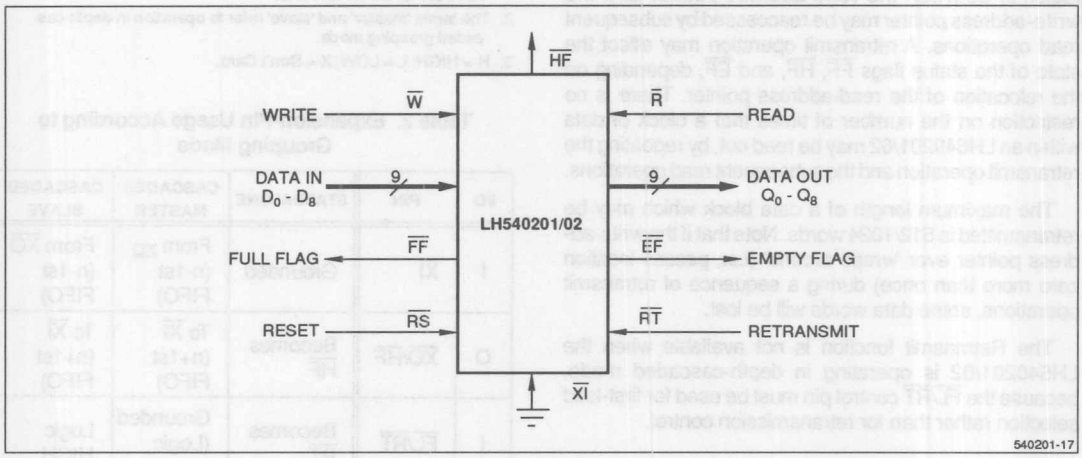


Figure 4. Standalone FIFO (512 × 9/1024 × 9)

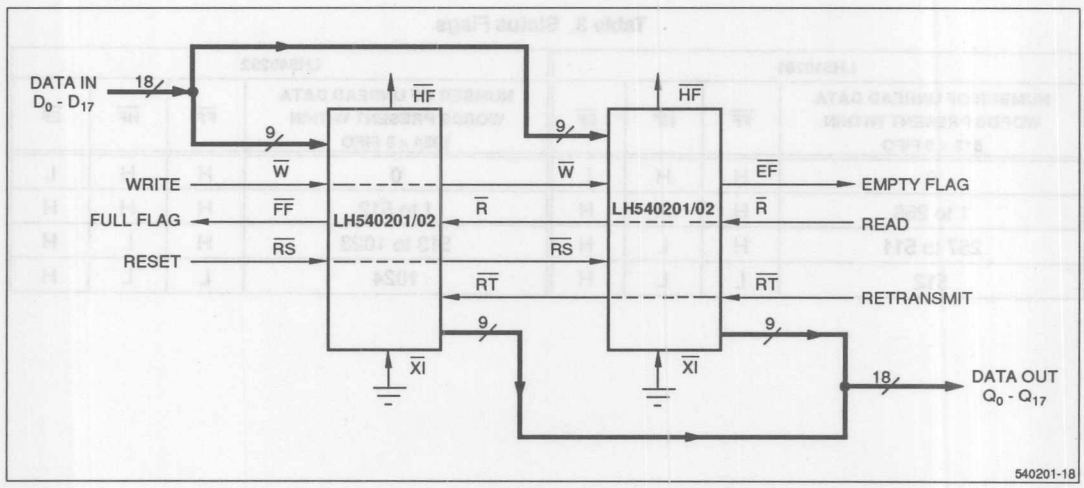


Figure 5. FIFO Word-Width Expansion (512 × 18/1024 × 18)

OPERATIONAL MODES (cont'd)

Depth Cascading

Depth cascading is implemented by configuring the required number of LH540201/02s in depth-cascaded mode. In this arrangement, the FIFOs are connected in a circular fashion, with the Expansion Out output ($\overline{XO}$) of each device tied to the Expansion In input ($\overline{XI}$) of the next device. One FIFO in the cascade must be designated as the 'first-load' device, by tying its First Load input ($\overline{FL}/\overline{RT}$) to ground. All other devices must have their $\overline{FL}/\overline{RT}$ inputs tied HIGH. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while logic within each LH540201/02 controls the steering of data. Only one LH540201/02 is enabled during any given write cycle; thus, the common Data In inputs of all devices are tied together. Likewise, only one LH540201/02 is enabled during any given read cycle; thus, the common Data Out outputs of all devices are wire-ORed together

In depth-cascaded mode, external logic should be used to generate a composite Full Flag and a composite Empty Flag, by ANDing the $\overline{FF}$ outputs of all LH540201/02 devices together and ANDing the $\overline{EF}$ outputs of all devices together. Since $\overline{FF}$ and $\overline{EF}$ are assertive-LOW signals, this 'ANDing' actually is implemented using an assertive-HIGH physical OR gate. The Half-Full Flag and the Retransmit function are not available in depth-cascaded mode.

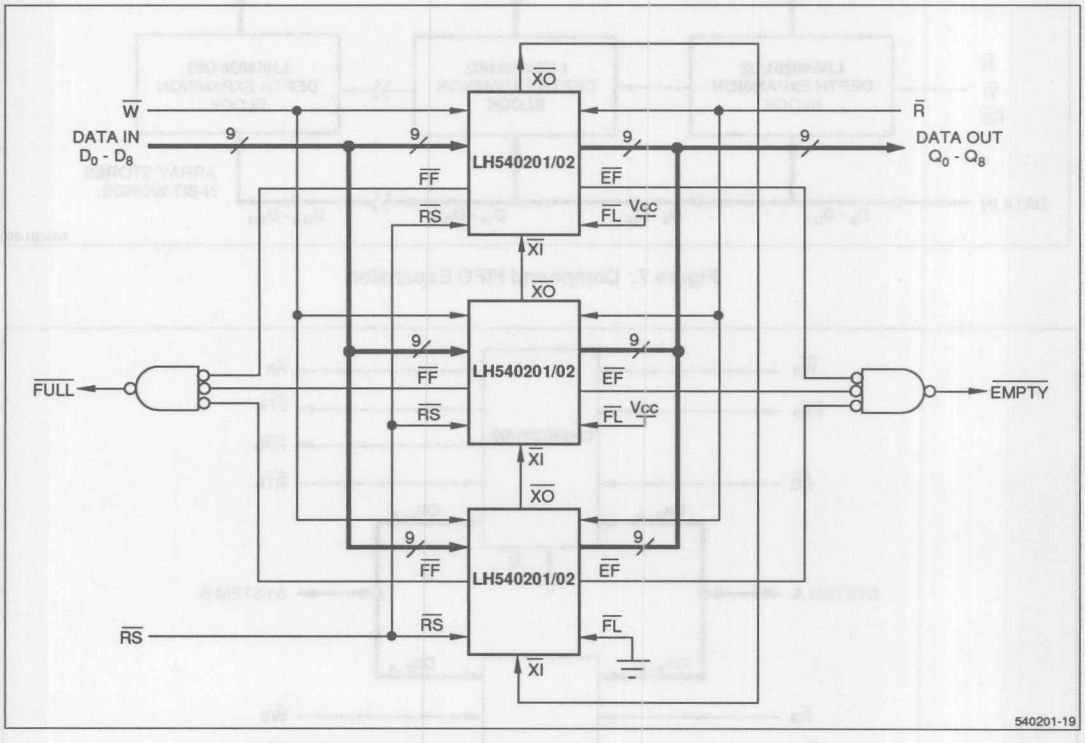


Figure 6. FIFO Depth Cascading (1536 × 9/3072 × 9)

OPERATIONAL MODES (cont'd)

Compound FIFO Expansion

A combination of word-width expansion and depth cascading may be implemented easily by operating groups of depth-cascaded FIFOs in parallel.

Bidirectional FIFO Operation

Bidirectional data buffering between two systems may be implemented by operating LH540201/02 devices in parallel, but in opposite directions. The Data In inputs of each LH540201/02 are tied to the corresponding Data Out outputs of another LH540201/02, which is operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both word-width expansion and depth cascading may be used in bidirectional applications.

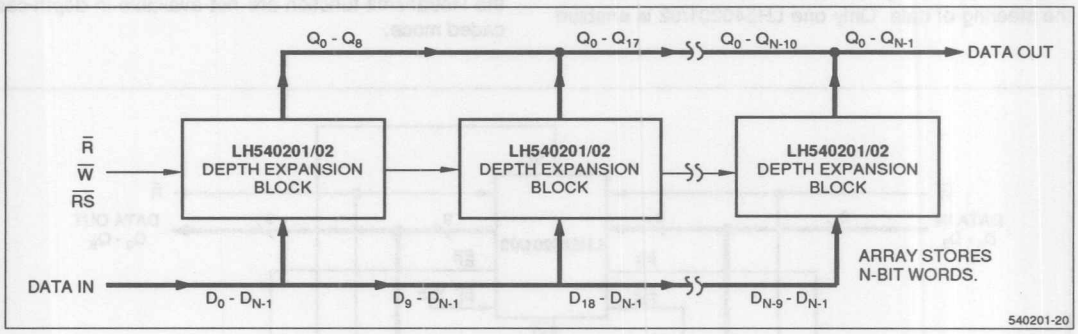


Figure 7. Compound FIFO Expansion

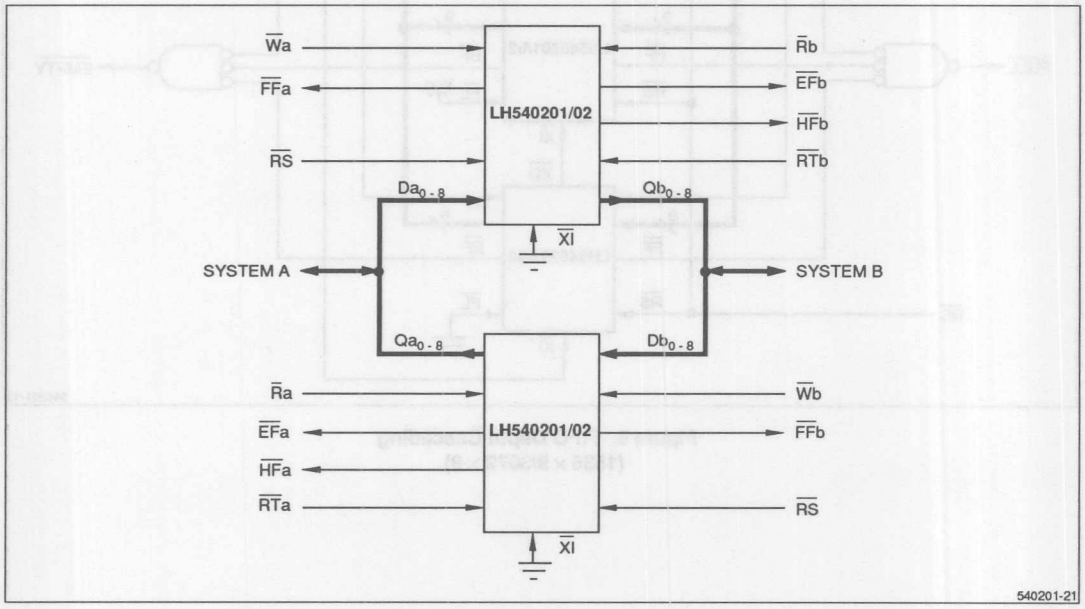


Figure 8. Bidirectional FIFO Operation (512 × 9 × 2/1024 × 9 × 2)

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [2]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside of those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

NOTES:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		5	mA

NOTES:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 9

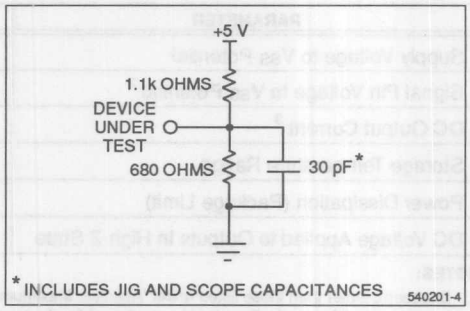


Figure 9. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
C_O MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz, with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS) [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [4,5]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
RETRANSMIT TIMING [5]																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65		80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65		80	–	ns
FLAG TIMING																
t_{EFL}	Reset LOW to Empty Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset HIGH to Half-Full and Full Flags HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out LOW	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements are performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values are guaranteed by design; not currently tested.
4. Only applies to read-data flow-through mode.
5. See also Note 2, Figure 19.

TIMING DIAGRAMS

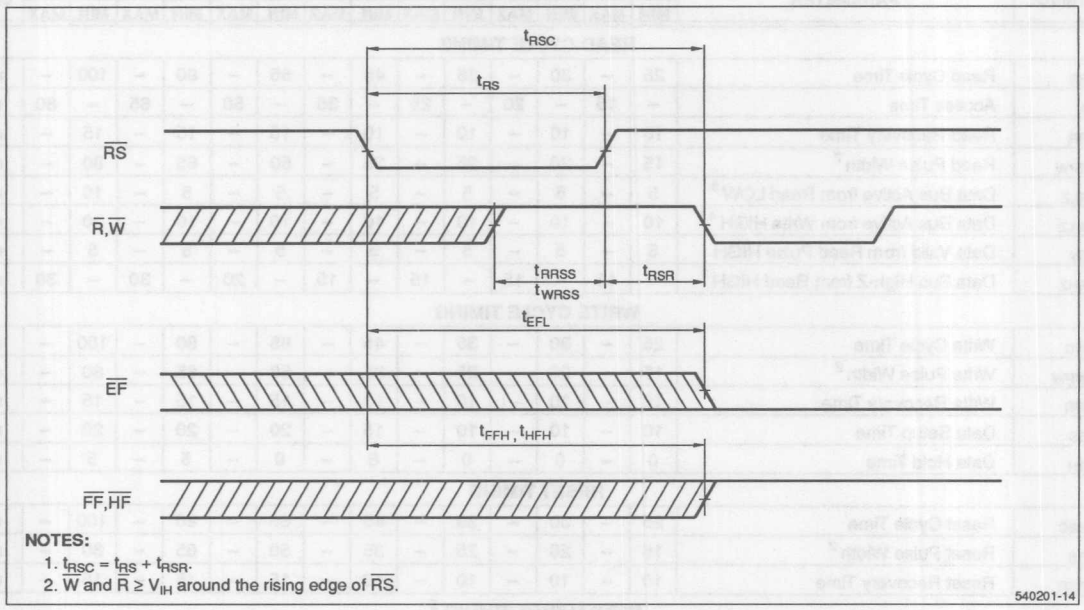


Figure 10. Reset Timing

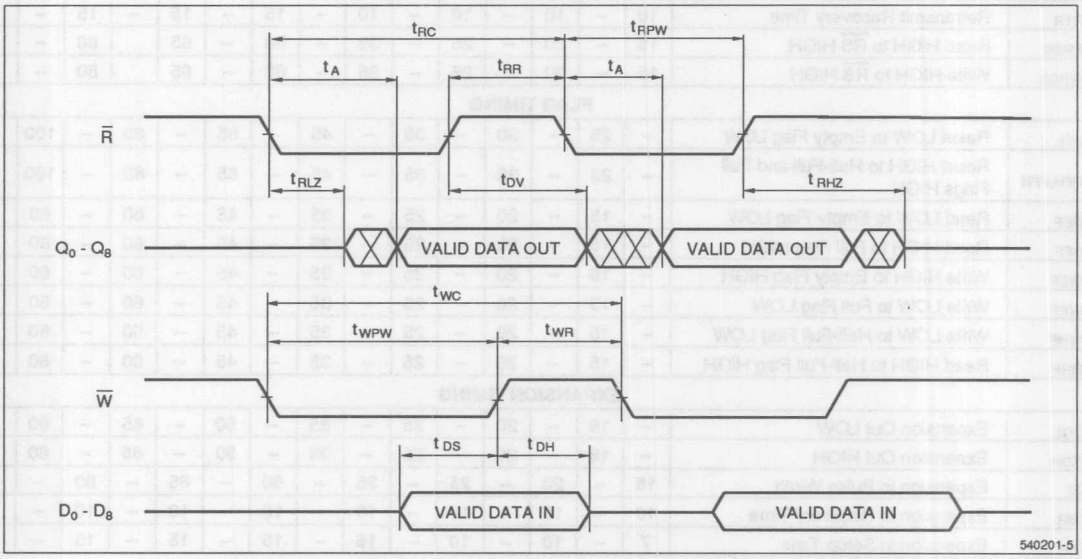


Figure 11. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

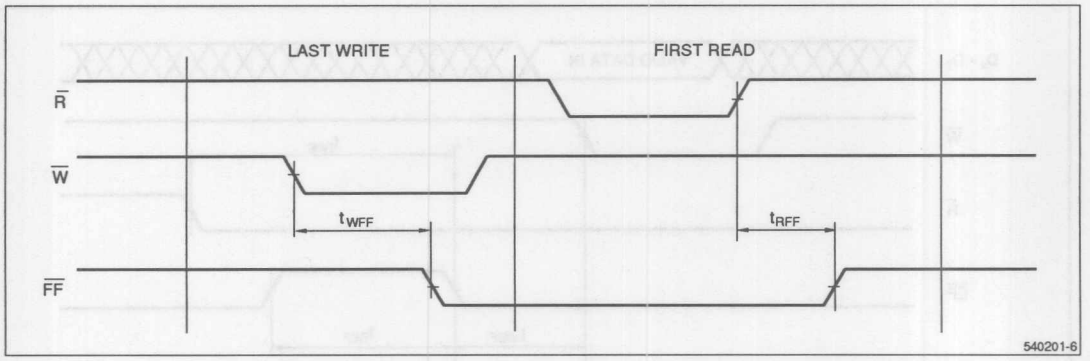


Figure 12. Full Flag From Last Write to First Read

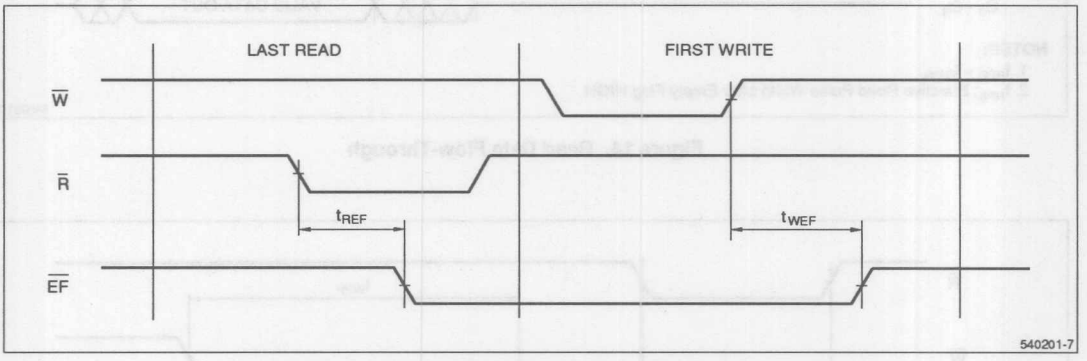
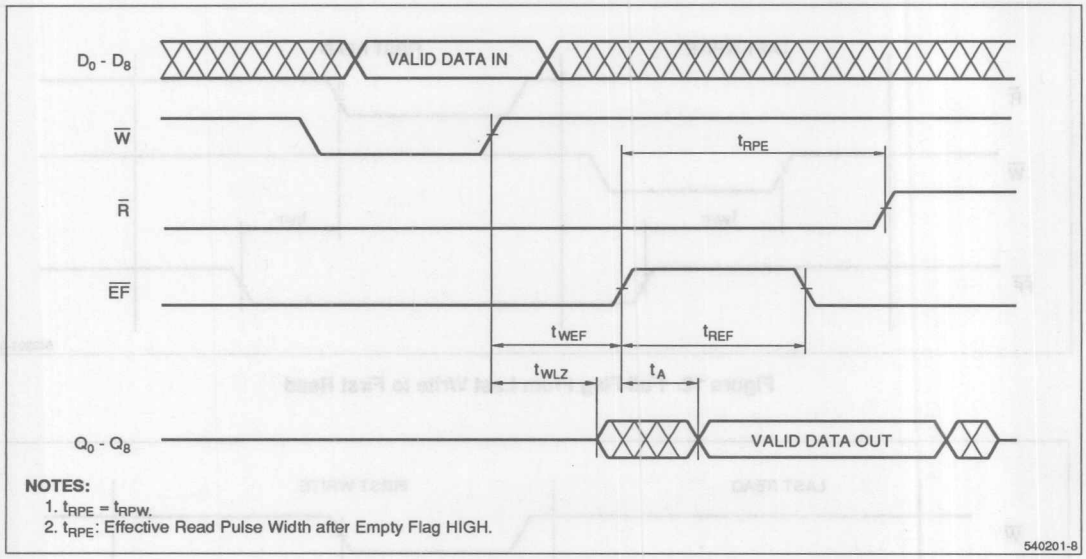


Figure 13. Empty Flag From Last Read to First Write

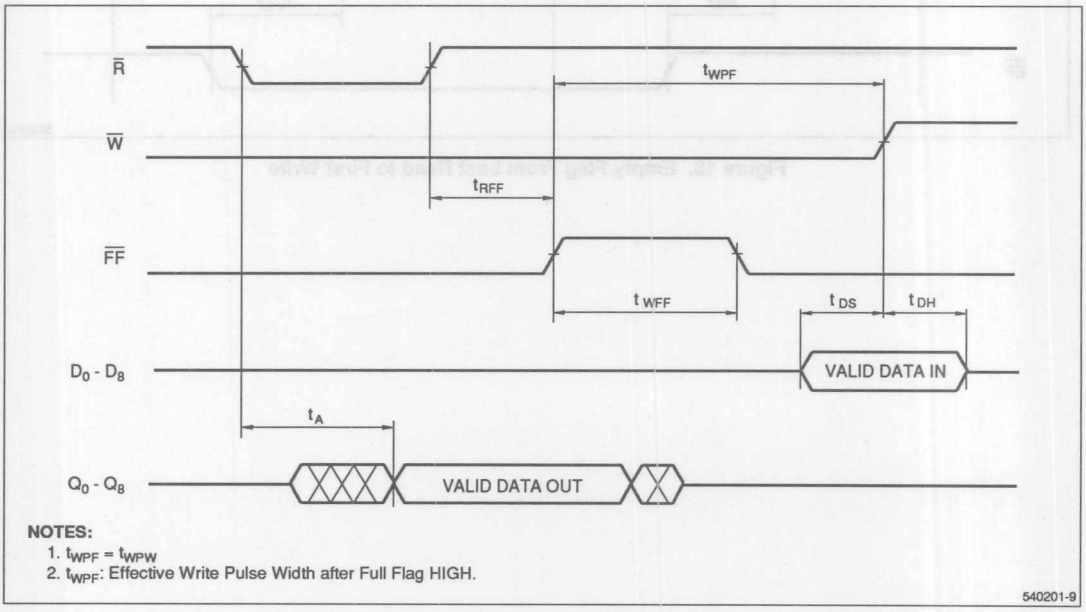
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540201-8

Figure 14. Read Data Flow-Through

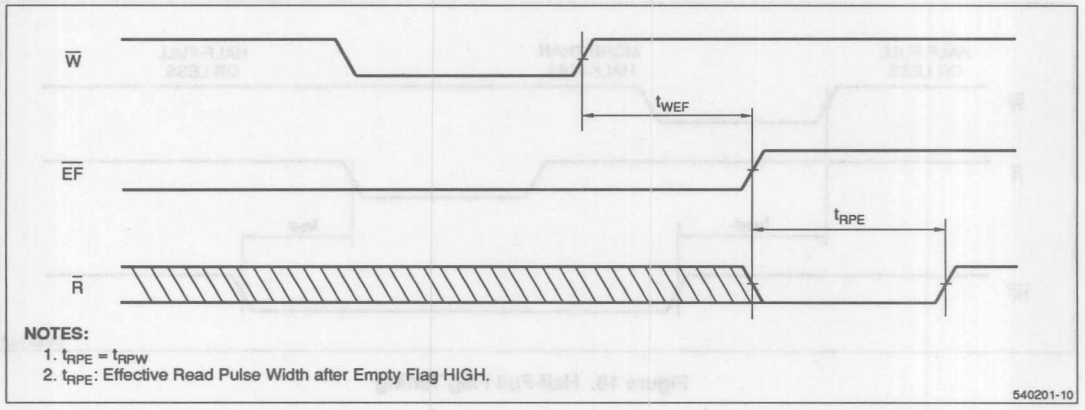


NOTES:
1. $t_{WPF} = t_{WPW}$
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540201-9

Figure 15. Write Data Flow-Through

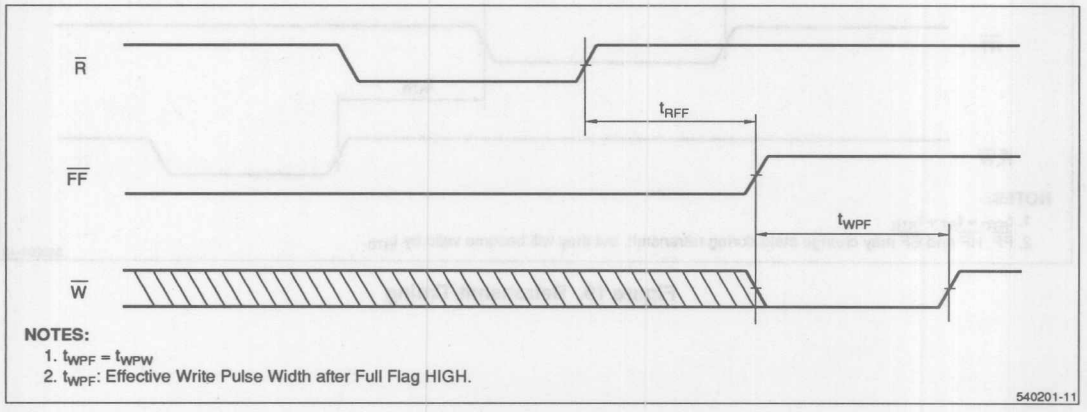
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540201-10

Figure 16. Empty Flag Timing



NOTES:
1. $t_{WPF} = t_{WPW}$
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540201-11

Figure 17. Full Flag Timing

TIMING DIAGRAMS (cont'd)

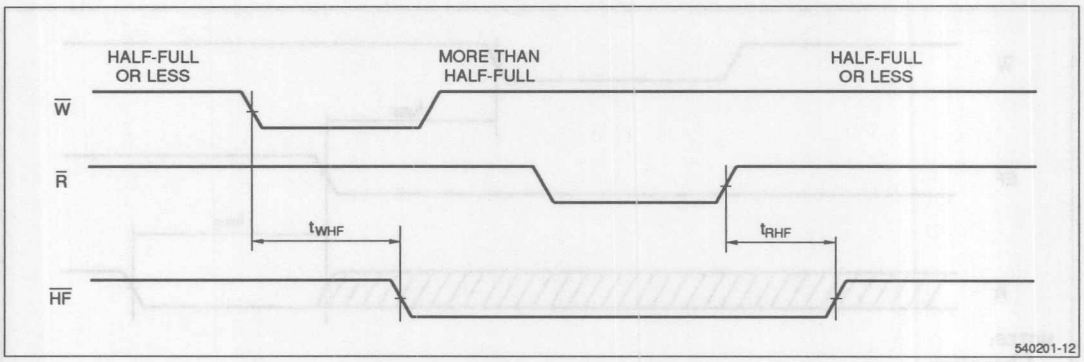


Figure 18. Half-Full Flag Timing

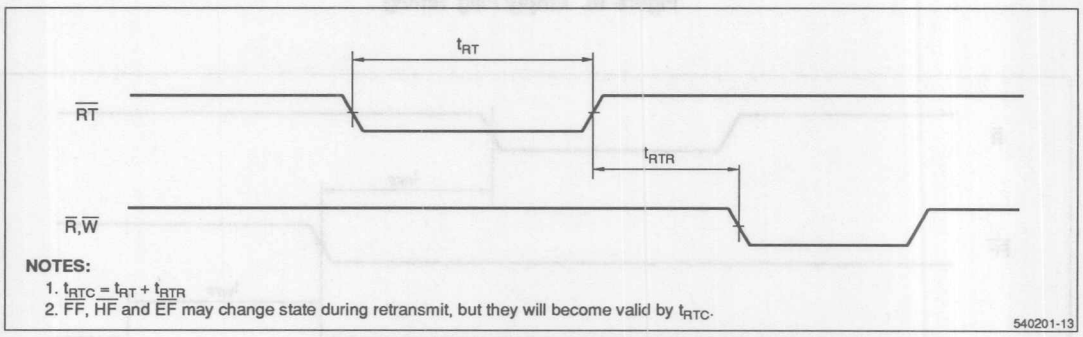


Figure 19. Retransmit Timing

TIMING DIAGRAMS (cont'd)

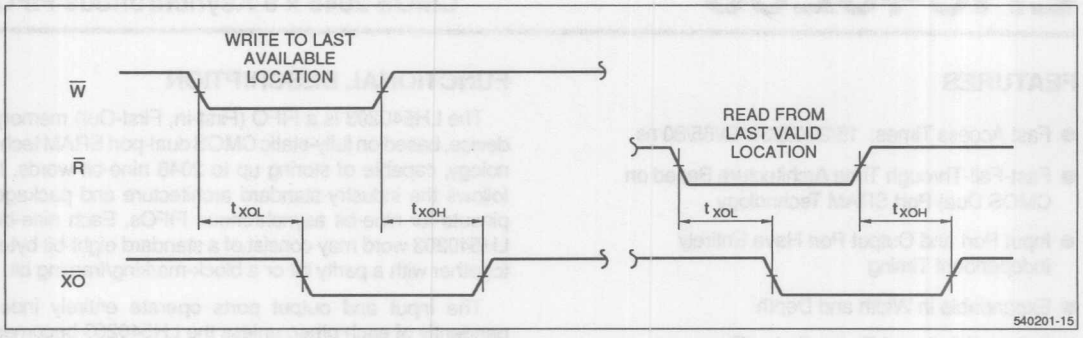


Figure 20. Expansion-Out Timing

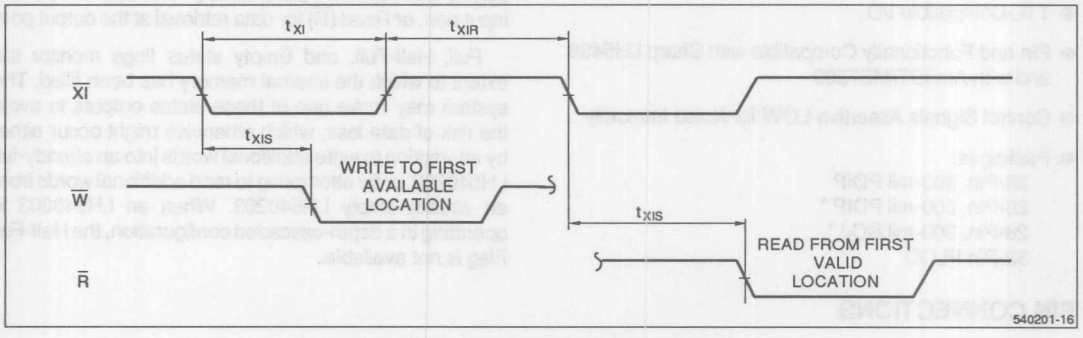
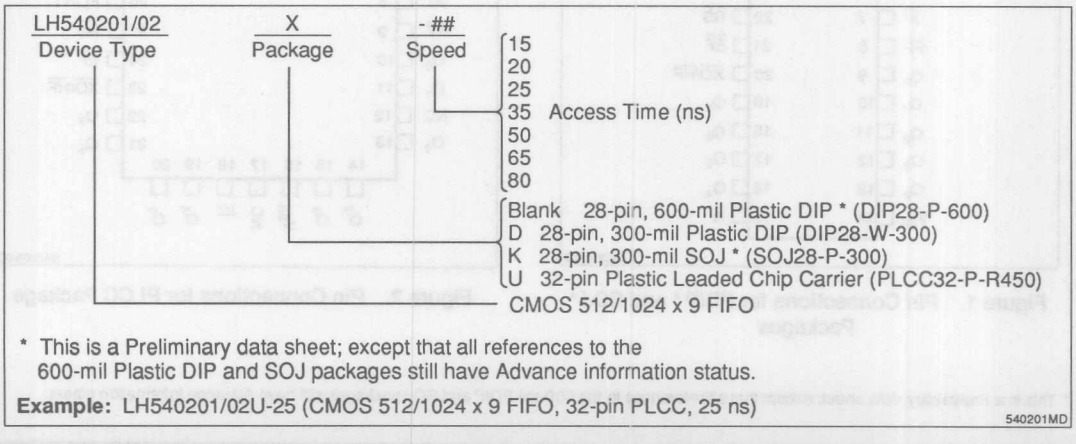


Figure 21. Expansion-In Timing

ORDERING INFORMATION



LH540203

PRELIMINARY

CMOS 2048 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 15/20/25/35/50/65/80 ns
- Fast-Fall-Through Time Architecture Based on CMOS Dual-Port SRAM Technology
- Input Port and Output Port Have Entirely Independent Timing
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Data Retransmission Capability
- TTL-Compatible I/O
- Pin and Functionally Compatible with Sharp LH5498 and with Am/IDT/MS7203
- Control Signals Assertive-LOW for Noise Immunity
- Packages:
  - 28-Pin, 300-mil PDIP
  - 28-Pin, 600-mil PDIP *
  - 28-Pin, 300-mil SOJ *
  - 32-Pin PLCC

FUNCTIONAL DESCRIPTION

The LH540203 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 2048 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit LH540203 word may consist of a standard eight-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the LH540203 becomes either totally full or else totally empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full LH540203, or by attempting to read additional words from an already-empty LH540203. When an LH540203 is operating in a depth-cascaded configuration, the Half-Full Flag is not available.

PIN CONNECTIONS

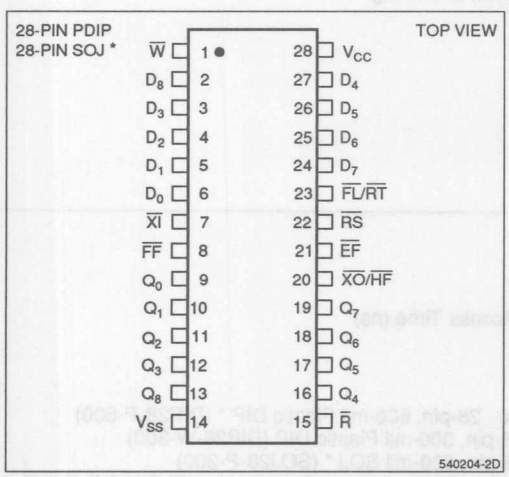


Figure 1. Pin Connections for PDIP * and SOJ * Packages

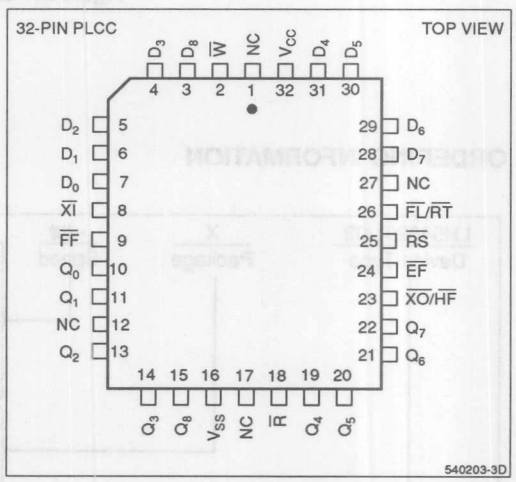


Figure 2. Pin Connections for PLCC Package

* This is a Preliminary data sheet; except that all references to the 600-mil PDIP and SOJ packages still have Advance Information status.

FUNCTIONAL DESCRIPTION (cont'd)

Data words are read out from the LH540203's output port in precisely the same order that they were written in at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the LH540203 device.

Drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO-memory-array read-address pointer to be set back to zero, to point to the LH540203's first physical memory location, without affecting the internal FIFO-memory-array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address-pointer value, may be read out *repeatedly* an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an LH540203 is operating in a depth-expanded configuration.

The Reset ($\overline{RS}$) control signal returns the LH540203 to an initial state, empty and ready to be filled. An LH540203 should be reset during every system power-up sequence. A reset operation causes the internal FIFO-memory-array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the LH540203's first physical memory location. Any information which previously had been stored within the LH540203 is not recoverable after a reset operation.

A cascading (depth-expansion) scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}/\overline{HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual LH540203 devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one LH540203 device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL}/\overline{RT}$) control input; the remaining LH540203 devices are designated as 'slaves,' by tying their $\overline{FL}/\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' LH540203 devices operating in cascaded mode.

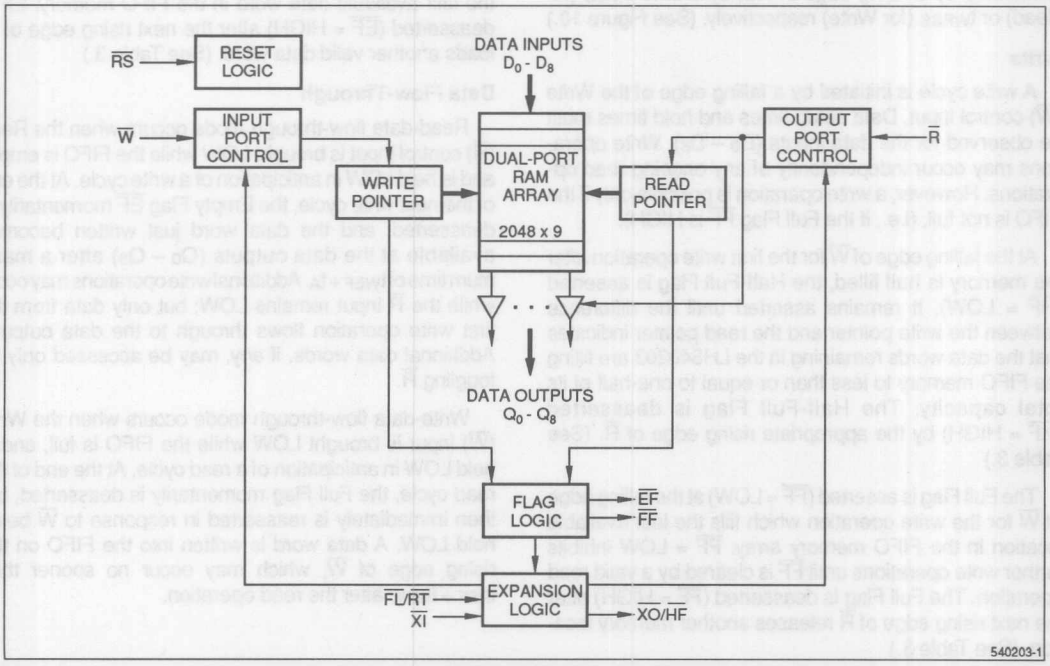


Figure 3. LH540203 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

OPERATIONAL DESCRIPTION

Reset

The LH540203 is reset whenever the Reset input ($\overline{RS}$) is taken LOW. A reset operation initializes both the read-address pointer and the write-address pointer to point to location zero, the first physical memory location. During a reset operation, the state of the $\overline{XI}$ and $\overline{FL}/\overline{RT}$ inputs determines whether the device is in standalone mode or in depth-cascaded mode. (See Tables 1 and 2.)

A reset operation is required whenever the LH540203 first is powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) inputs may be in any state when the reset operation is initiated; but they must be HIGH, before the reset operation is terminated by a rising edge of $\overline{RS}$, by a time t_{RRSS} (for Read) or t_{WRSS} (for Write) respectively. (See Figure 10.)

Write

A write cycle is initiated by a falling edge of the Write ($\overline{W}$) control input. Data setup times and hold times must be observed for the data inputs ($D_0 - D_8$). Write operations may occur independently of any ongoing read operations. However, a write operation is possible only if the FIFO is not full, (i.e., if the Full Flag $\overline{FF}$ is HIGH).

At the falling edge of $\overline{W}$ for the first write operation after the memory is half filled, the Half-Full Flag is asserted ($\overline{HF}$ = LOW). It remains asserted until the difference between the write pointer and the read pointer indicates that the data words remaining in the LH540203 are filling the FIFO memory to less than or equal to one-half of its total capacity. The Half-Full Flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$. (See Table 3.)

The Full Flag is asserted ($\overline{FF}$ = LOW) at the falling edge of $\overline{W}$ for the write operation which fills the last available location in the FIFO memory array. $\overline{FF}$ = LOW inhibits further write operations until $\overline{FF}$ is cleared by a valid read operation. The Full Flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location. (See Table 3.)

Read

A read cycle is initiated by a falling edge of the Read ($\overline{R}$) control input. Read data becomes valid at the data outputs ($Q_0 - Q_8$) after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data outputs return to a high-impedance state. Read operations may occur independently of any ongoing write operations. However, a read operation is possible only if the FIFO is not empty (i.e., if the Empty Flag $\overline{EF}$ is HIGH).

The LH540203's internal read-address and write-address pointers operate in such a way that consecutive read operations always access data words in the same order that they were written. The Empty Flag is asserted ($\overline{EF}$ = LOW) after that falling edge of $\overline{R}$ which accesses the last available data word in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another valid data word. (See Table 3.)

Data Flow-Through

Read-data flow-through mode occurs when the Read ($\overline{R}$) control input is brought LOW while the FIFO is empty, and is held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty Flag $\overline{EF}$ momentarily is deasserted, and the data word just written becomes available at the data outputs ($Q_0 - Q_8$) after a maximum time of $t_{WEF} + t_A$. Additional write operations may occur while the $\overline{R}$ input remains LOW; but only data from the first write operation flows through to the data outputs. Additional data words, if any, may be accessed only by toggling $\overline{R}$.

Write-data flow-through mode occurs when the Write ($\overline{W}$) input is brought LOW while the FIFO is full, and is held LOW in anticipation of a read cycle. At the end of the read cycle, the Full Flag momentarily is deasserted, but then immediately is reasserted in response to $\overline{W}$ being held LOW. A data word is written into the FIFO on the rising edge of $\overline{W}$, which may occur no sooner than $t_{RFF} + t_{WPW}$ after the read operation.

OPERATIONAL DESCRIPTION (cont'd)

Retransmit

The FIFO can be made to reread previously-read data by means of the Retransmit function. A retransmit operation is initiated by pulsing the $\overline{RT}$ input LOW. Both $\overline{R}$ and $\overline{W}$ must be deasserted (HIGH) for the duration of the retransmit pulse. The FIFO's internal read-address pointer is reset to point to location zero, the first physical memory location, while the internal write-address pointer remains unchanged.

After a retransmit operation, those data words in the region in between the read-address pointer and the write-address pointer may be reaccessed by subsequent read operations. A retransmit operation may affect the state of the status flags $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$, depending on the relocation of the read-address pointer. There is no restriction on the number of times that a block of data within an LH540203 may be read out, by repeating the retransmit operation and the subsequent read operations.

The maximum length of a data block which may be retransmitted is 2048 words. Note that if the write-address pointer ever 'wraps around' (i.e., passes location zero more than once) during a sequence of retransmit operations, some data words will be lost.

The Retransmit function is not available when the LH540203 is operating in depth-cascaded mode, because the $\overline{FL}/\overline{RT}$ control pin must be used for first-load selection rather than for retransmission control.

Table 1. Grouping-Mode Determination During a Reset Operation

$\overline{XI}$	$\overline{FL}/\overline{RT}$	MODE	$\overline{XO}/\overline{HF}$ USAGE	$\overline{XI}$ USAGE	$\overline{FL}/\overline{RT}$ USAGE
H [1]	H	Cascaded Slave [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
H [1]	L	Cascaded Master [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
L	X	Standalone	$\overline{HF}$	(none)	$\overline{RT}$

NOTES:
1. A reset operation forces $\overline{XO}$ HIGH for the nth FIFO, thus forcing $\overline{XI}$ HIGH for the n+1st FIFO.
2. The terms 'master' and 'slave' refer to operation in depth-cascaded grouping mode.
3. H = HIGH; L = LOW; X = Don't Care.

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	STANDALONE	CASCADED MASTER	CASCADED SLAVE
I	$\overline{XI}$	Grounded	From $\overline{XO}$ (n-1st FIFO)	From $\overline{XO}$ (n-1st FIFO)
O	$\overline{XO}/\overline{HF}$	Becomes $\overline{HF}$	To $\overline{XI}$ (n+1st FIFO)	To $\overline{XI}$ (n+1st FIFO)
I	$\overline{FL}/\overline{RT}$	Becomes $\overline{RT}$	Grounded (Logic LOW)	Logic HIGH

Table 3. Status Flags

NUMBER OF UNREAD DATA WORDS PRESENT WITHIN 2048 × 9 FIFO	$\overline{FF}$	$\overline{HF}$	$\overline{EF}$
0	H	H	L
1 to 1024	H	H	H
1025 to 2047	H	L	H
2048	L	L	H

OPERATIONAL MODES

Standalone Configuration

When depth cascading is not required for a given application, the LH540203 is placed in standalone mode by tying the Expansion In input ($\overline{XI}$) to ground. This input is internally sampled during a reset operation. (See Table 1.)

Width Expansion

Word-width expansion is implemented by placing multiple LH540203 devices in parallel. Each LH540203 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 4, 5, and 6.)

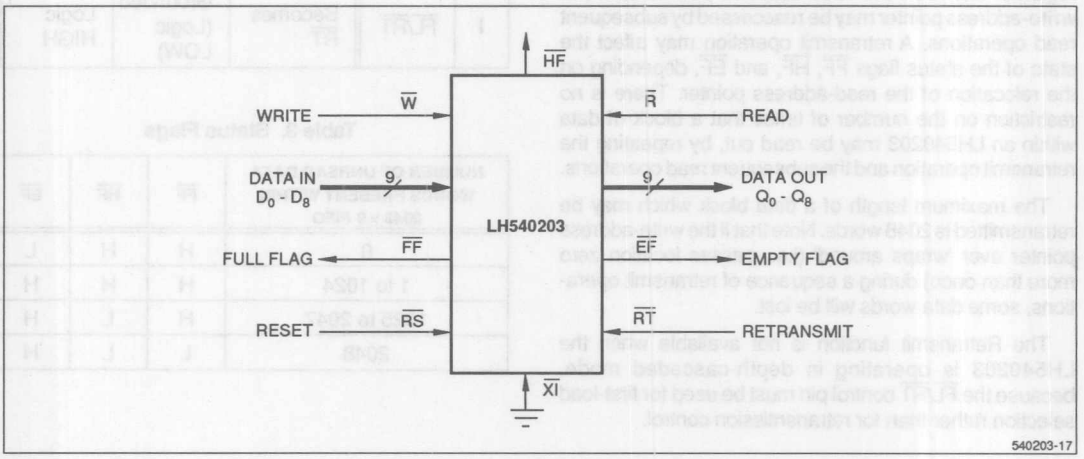


Figure 4. Standalone FIFO (2048 × 9)

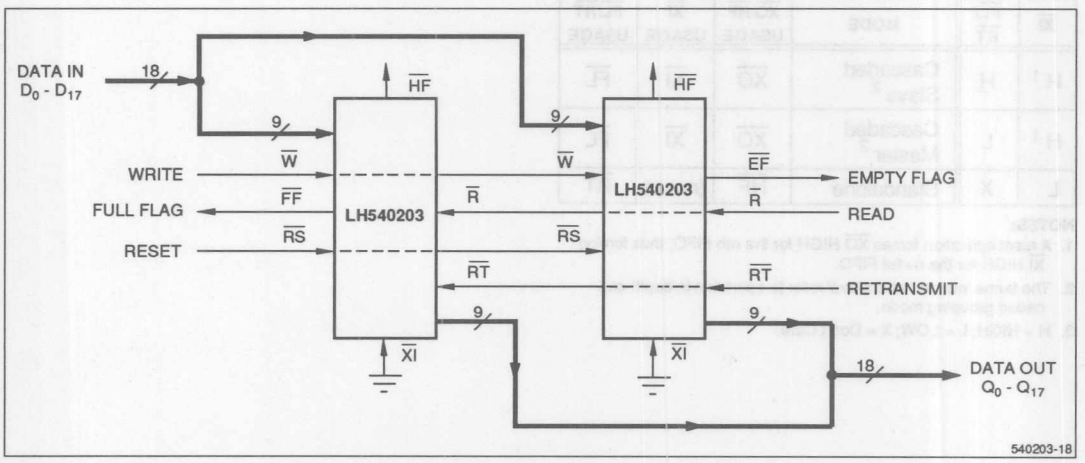


Figure 5. FIFO Word-Width Expansion (2048 × 18)

OPERATIONAL MODES (cont'd)

Depth Cascading

Depth cascading is implemented by configuring the required number of LH540203s in depth-cascaded mode. In this arrangement, the FIFOs are connected in a circular fashion, with the Expansion Out output ($\overline{XO}$) of each device tied to the Expansion In input ($\overline{XI}$) of the next device. One FIFO in the cascade must be designated as the 'first-load' device, by tying its First Load input ($\overline{FL}/\overline{RT}$) to ground. All other devices must have their $\overline{FL}/\overline{RT}$ inputs tied HIGH. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while logic within each LH540203 controls the steering of data. Only one LH540203 is enabled during any given write cycle; thus, the common Data In inputs of all devices are tied together. Likewise, only one LH540203 is enabled during any given read cycle; thus, the common Data Out outputs of all devices are wire-ORed together.

In depth-cascaded mode, external logic should be used to generate a composite Full Flag and a composite Empty Flag, by ANDing the $\overline{FF}$ outputs of all LH540203 devices together and ANDing the $\overline{EF}$ outputs of all devices together. Since $\overline{FF}$ and $\overline{EF}$ are assertive-LOW signals, this 'ANDing' actually is implemented using an assertive-HIGH physical OR gate. The Half-Full Flag and the Retransmit function are not available in depth-cascaded mode.

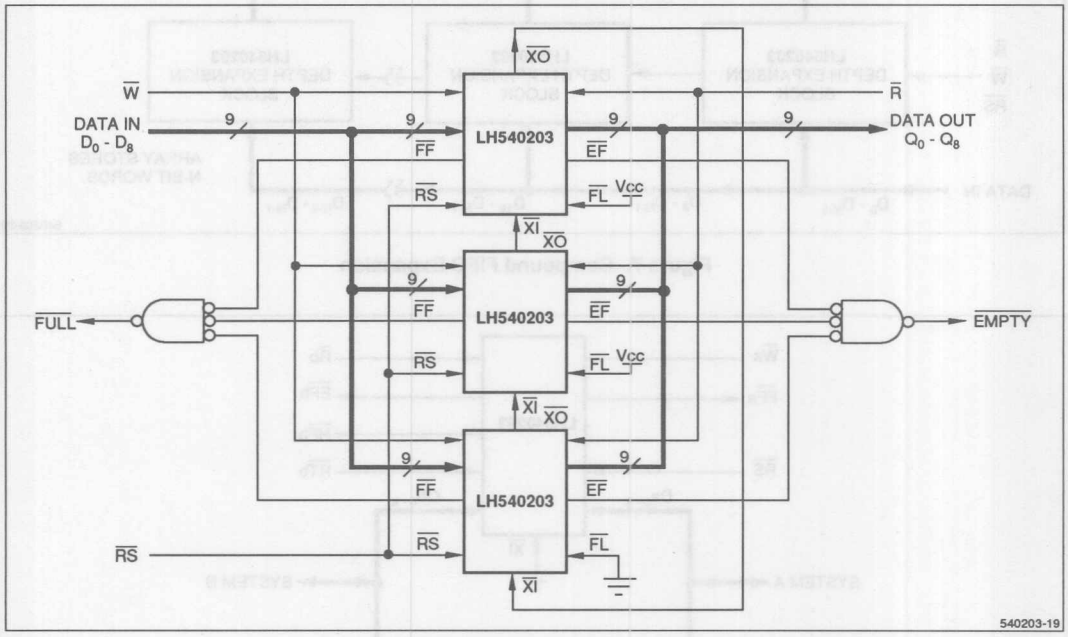


Figure 6. FIFO Depth Cascading (6144 × 9)

OPERATIONAL MODES (cont'd)

Compound FIFO Expansion

A combination of word-width expansion and depth cascading may be implemented easily by operating groups of depth-cascaded FIFOs in parallel.

Bidirectional FIFO Operation

Bidirectional data buffering between two systems may be implemented by operating LH540203 devices in parallel, but in opposite directions. The Data In inputs of each LH540203 are tied to the corresponding Data Out outputs of another LH540203, which is operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both word-width expansion and depth cascading may be used in bidirectional applications.

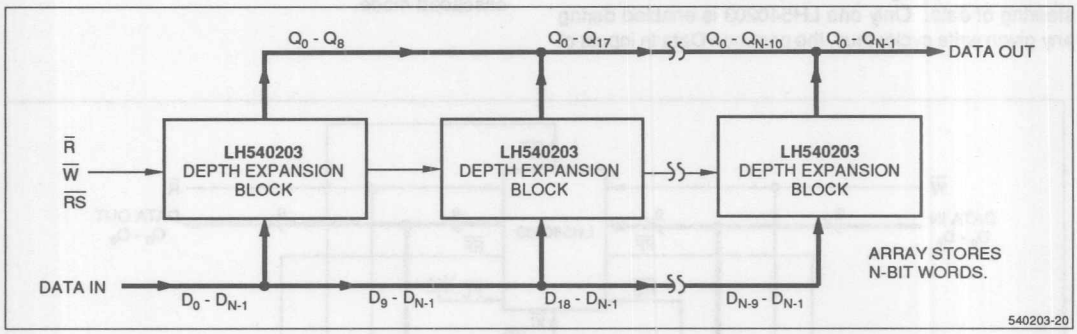


Figure 7. Compound FIFO Expansion

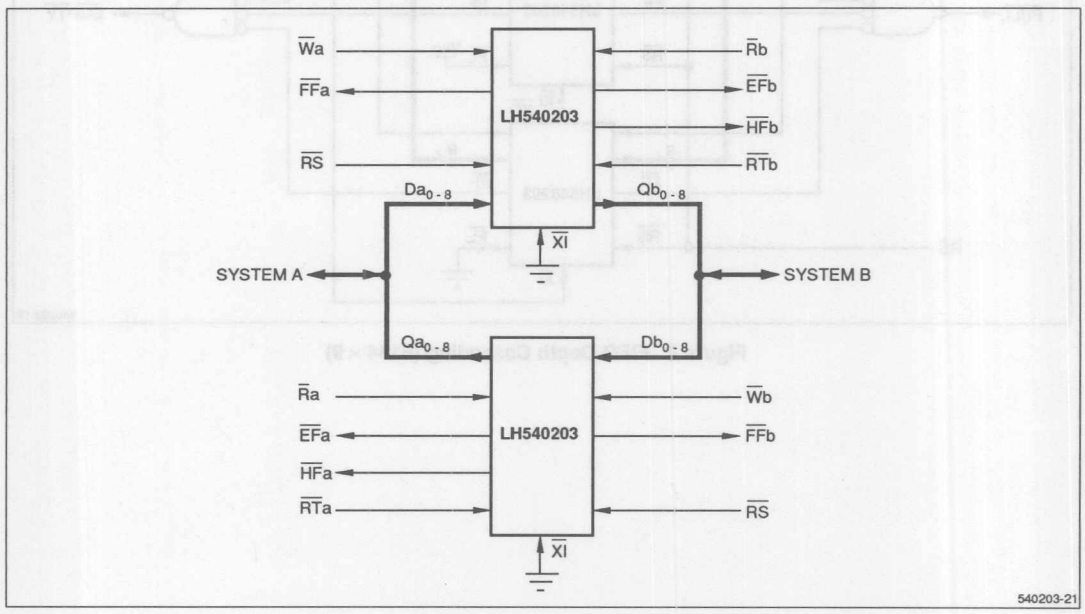


Figure 8. Bidirectional FIFO Operation (2048 × 9 × 2)

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [2]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside of those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

NOTES:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		100	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		5	mA

NOTES:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 9

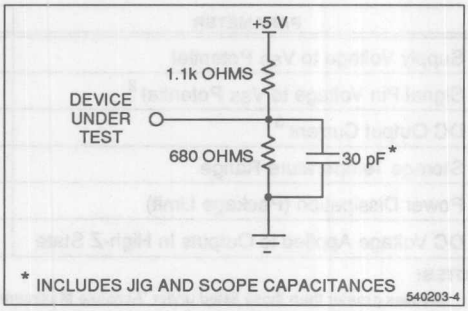


Figure 9. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
C_O MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz, with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS) [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 15 ns		t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING																
t_{RC}	Read Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	15	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [4,5]	10	–	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING																
t_{WC}	Write Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING																
t_{RSC}	Reset Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65		80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	15	–	20	–	25	–	35	–	50	–	65		80	–	ns
RETRANSMIT TIMING [5]																
t_{RTC}	Retransmit Cycle Time	25	–	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING																
t_{EFL}	Reset LOW to Empty Flag LOW	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset HIGH to Half-Full and Full Flags HIGH	–	25	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	15	–	20	–	25	–	35	–	45	–	60	–	60	ns
EXPANSION TIMING																
t_{XOL}	Expansion Out LOW	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	18	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	15	–	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion In Setup Time	7	–	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements are performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values are guaranteed by design; not currently tested.
4. Only applies to read-data flow-through mode.
5. See also Note 2, Figure 19.

TIMING DIAGRAMS

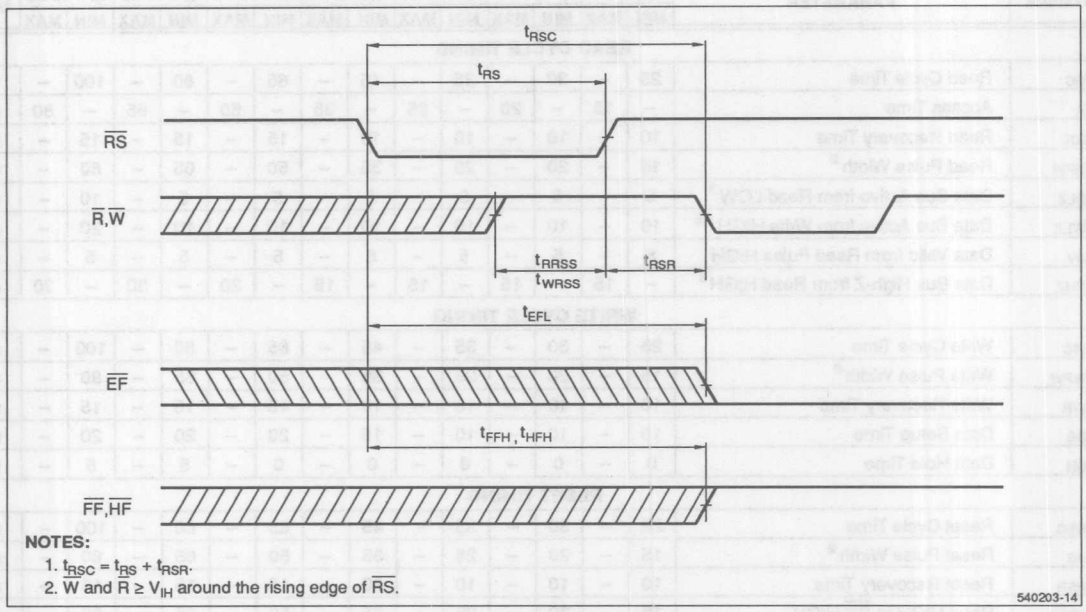


Figure 10. Reset Timing

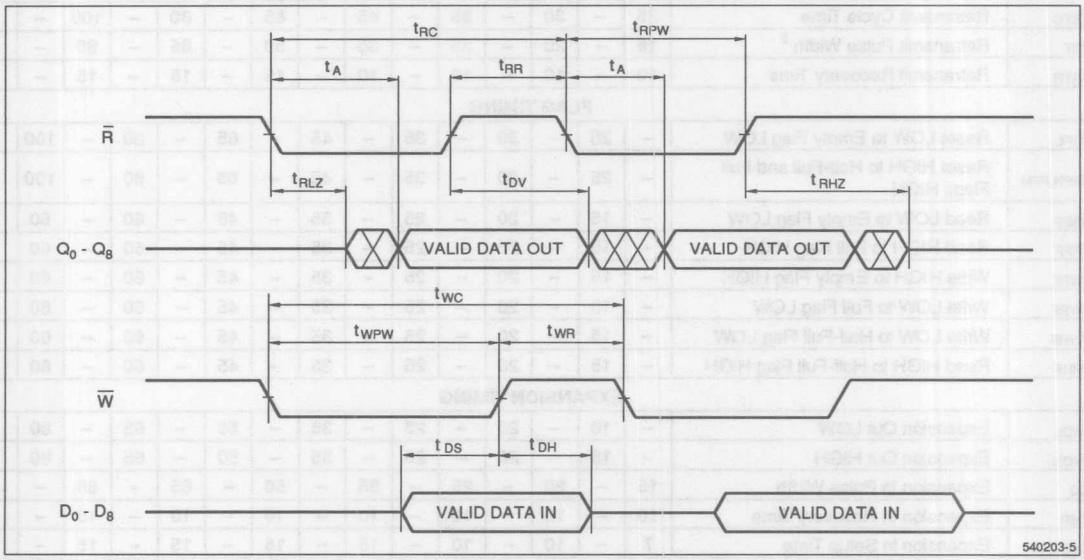


Figure 11. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

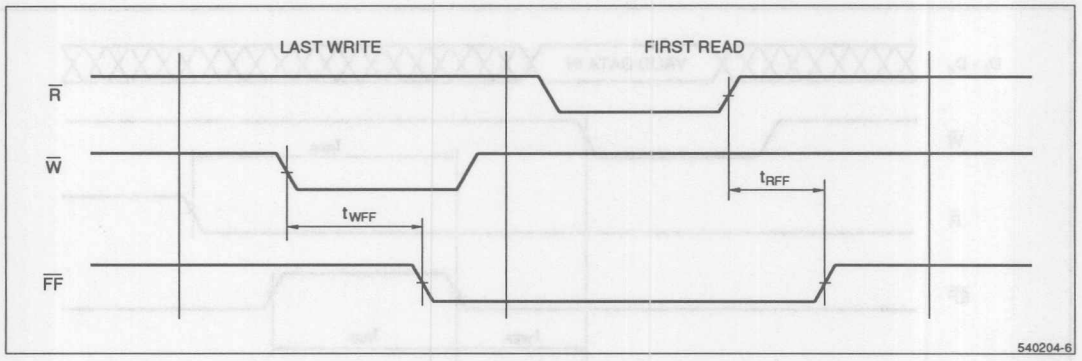


Figure 12. Full Flag From Last Write to First Read

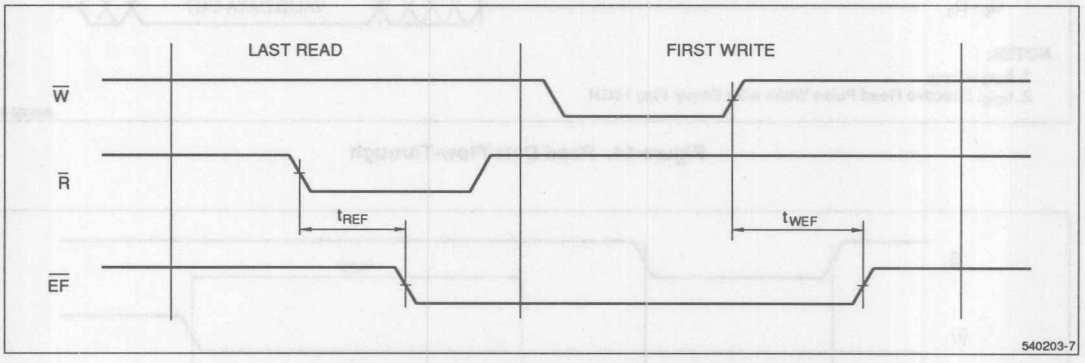


Figure 13. Empty Flag From Last Read to First Write

TIMING DIAGRAMS (cont'd)

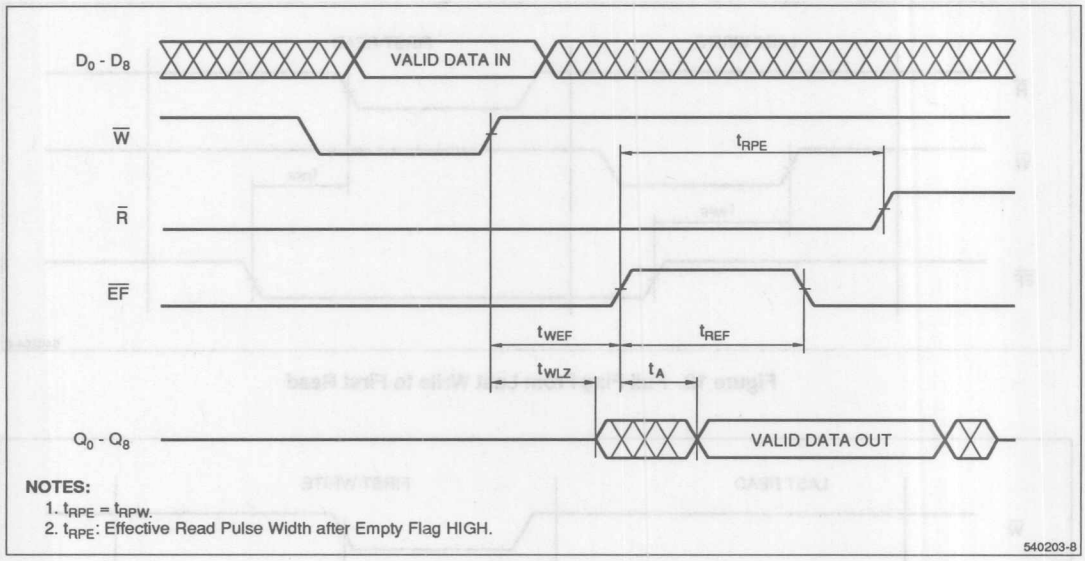


Figure 14. Read Data Flow-Through

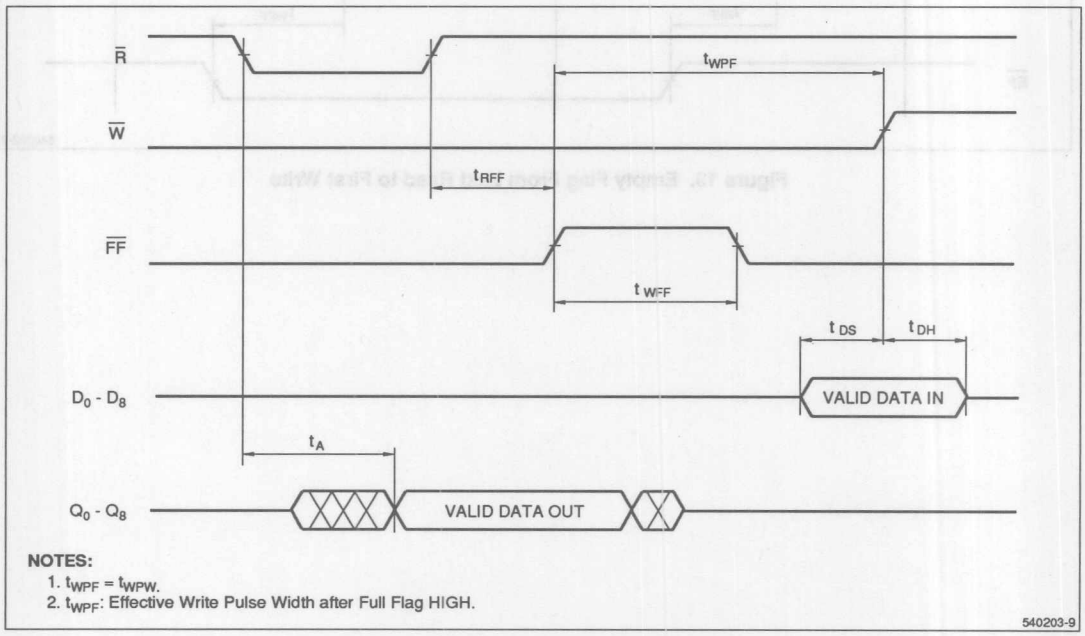


Figure 15. Write Data Flow-Through

TIMING DIAGRAMS (cont'd)

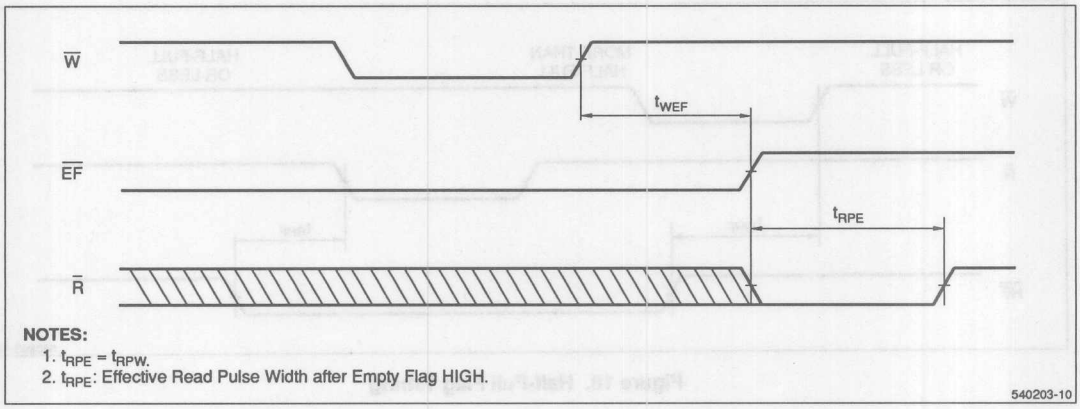


Figure 16. Empty Flag Timing

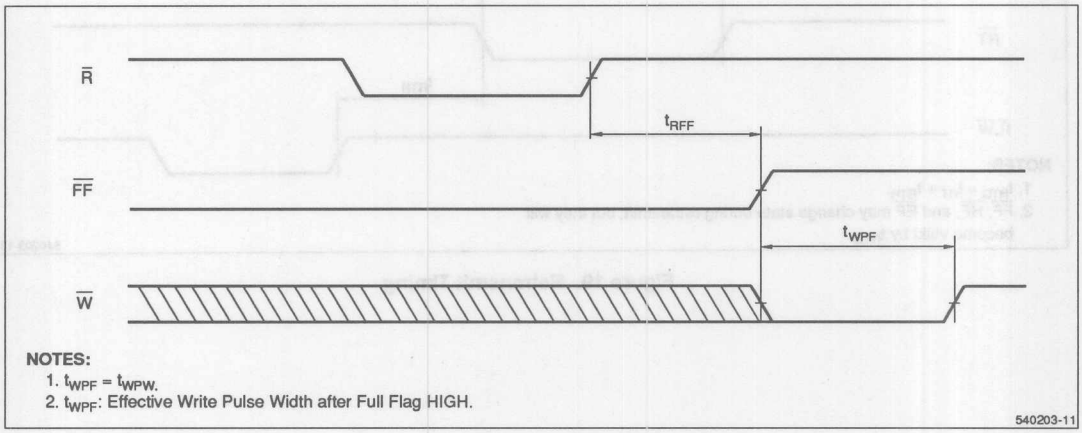


Figure 17. Full Flag Timing

TIMING DIAGRAMS (cont'd)

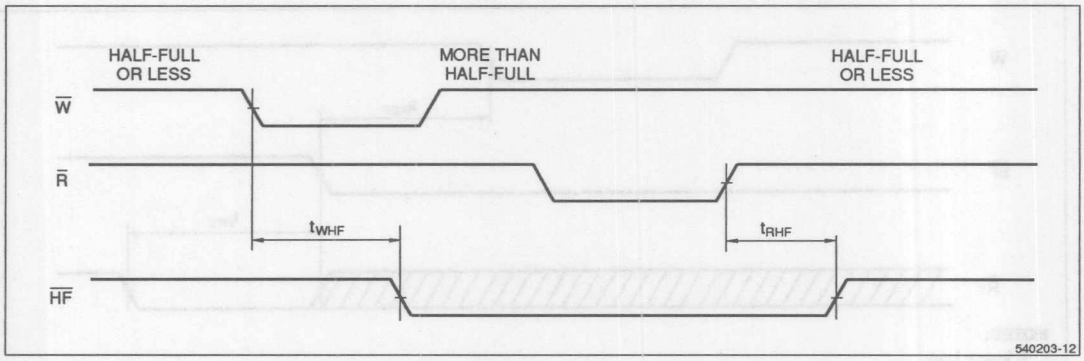


Figure 18. Half-Full Flag Timing

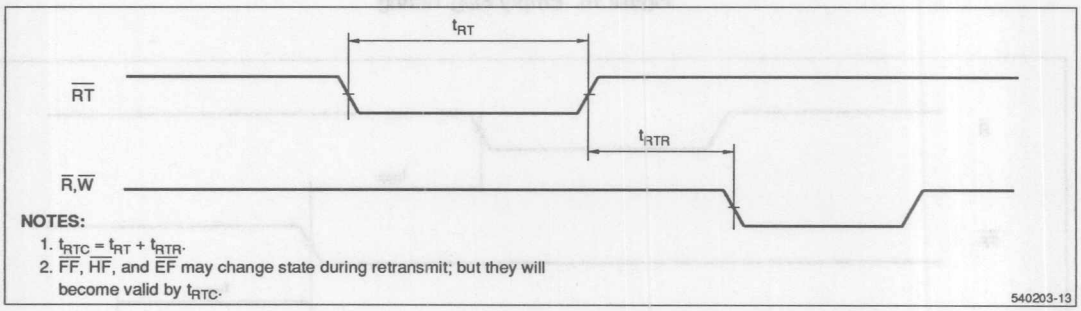


Figure 19. Retransmit Timing

TIMING DIAGRAMS (cont'd)

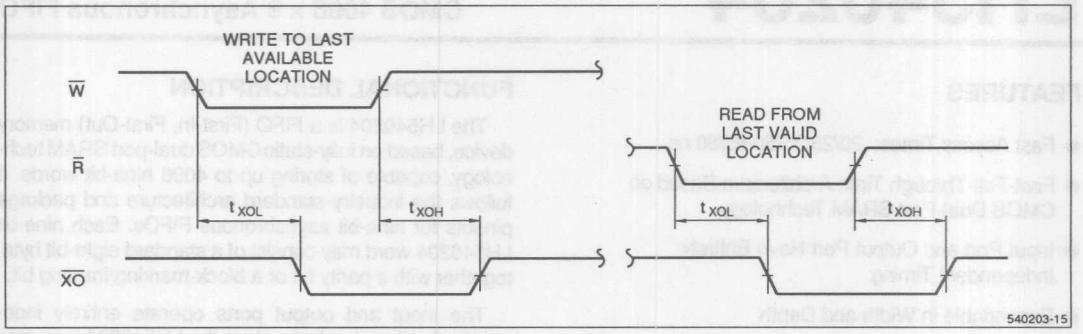


Figure 20. Expansion-Out Timing

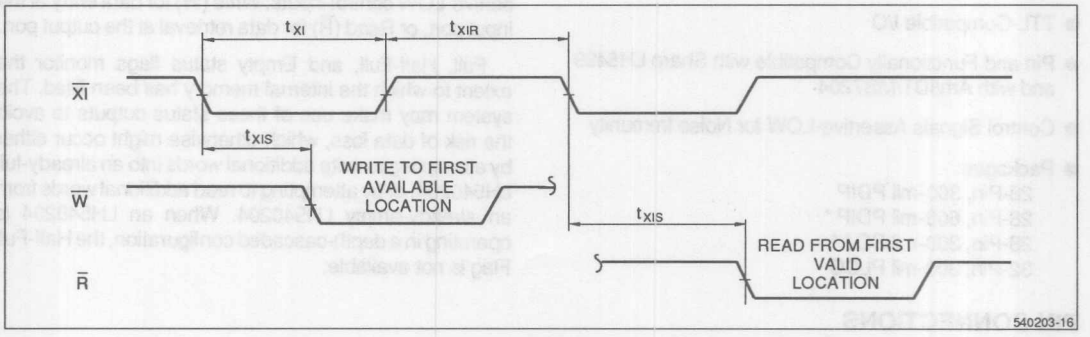


Figure 21. Expansion-In Timing

ORDERING INFORMATION

LH540203	X	- ##
Device Type	Package	Speed

Speed:
- 15
- 20
- 25
- 35
- 50
- 65
- 80

Access Time (ns)

Package:
- Blank 28-pin, 600-mil Plastic DIP * (DIP28-P-600)
- D 28-pin, 300-mil Plastic DIP (DIP28-W-300)
- K 28-pin, 300-mil SOJ * (SOJ28-P-300)
- U 32-pin Plastic Leaded Chip Carrier (PLCC32-P-R450)

Device Type: CMOS 2048 x 9 FIFO

* This is a Preliminary data sheet; except that all references to the 600-mil Plastic DIP and SOJ packages still have Advance information status.

Example: LH540203U-25 (CMOS 2048 x 9 FIFO, 32-pin PLCC, 25 ns)

540203MD

LH540204

ADVANCE INFORMATION

CMOS 4096 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 20/25/35/50/65/80 ns
- Fast-Fall-Through Time Architecture Based on CMOS Dual-Port SRAM Technology
- Input Port and Output Port Have Entirely Independent Timing
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Data Retransmission Capability
- TTL-Compatible I/O
- Pin and Functionally Compatible with Sharp LH5499 and with Am/IDT/MS7204
- Control Signals Assertive-LOW for Noise Immunity
- Packages:
  - 28-Pin, 300-mil PDIP
  - 28-Pin, 600-mil PDIP *
  - 28-Pin, 300-mil SOJ *
  - 32-Pin, 300-mil PLCC

FUNCTIONAL DESCRIPTION

The LH540204 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 4096 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit LH540204 word may consist of a standard eight-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the LH540204 becomes either totally full or else totally empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full LH540204, or by attempting to read additional words from an already-empty LH540204. When an LH540204 is operating in a depth-cascaded configuration, the Half-Full Flag is not available.

PIN CONNECTIONS

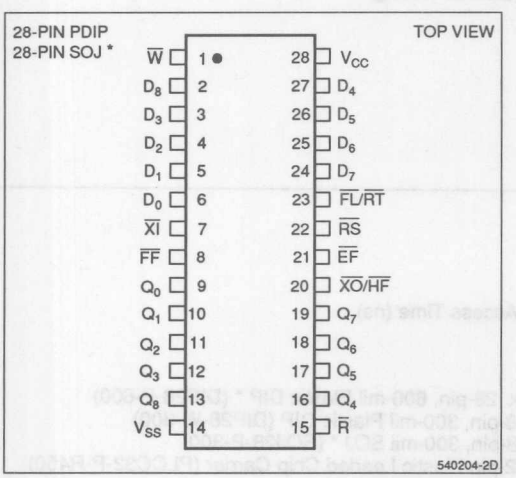


Figure 1. Pin Connections for PDIP * and SOJ * Packages

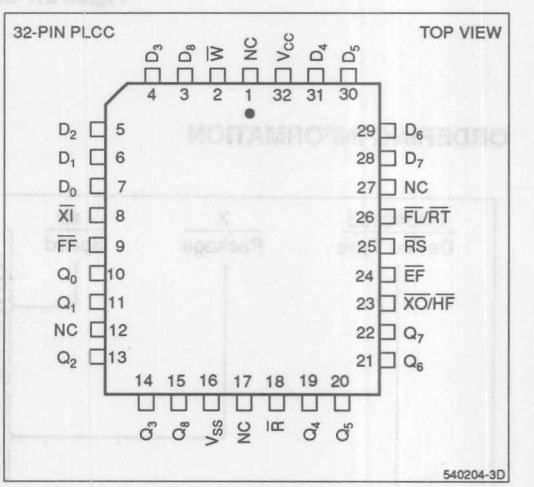


Figure 2. Pin Connections for PLCC Package

* This is an Advance Information data sheet; except that all references to the 600-mil PDIP and SOJ packages still have Product Preview status.

FUNCTIONAL DESCRIPTION (cont'd)

Data words are read out from the LH540204's output port in precisely the same order that they were written in at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the LH540204 device.

Drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO-memory-array read-address pointer to be set back to zero, to point to the LH540204's first physical memory location, without affecting the internal FIFO-memory-array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address-pointer value, may be read out *repeatedly* an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an LH540204 is operating in a depth-expanded configuration.

The Reset ($\overline{RS}$) control signal returns the LH540204 to an initial state, empty and ready to be filled. An LH540204 should be reset during every system power-up sequence. A reset operation causes the internal FIFO-memory-array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the LH540204's first physical memory location. Any information which previously had been stored within the LH540204 is not recoverable after a reset operation.

A cascading (depth-expansion) scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}/\overline{HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual LH540204 devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one LH540204 device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL}/\overline{RT}$) control input; the remaining LH540204 devices are designated as 'slaves,' by tying their $\overline{FL}/\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' LH540204 devices operating in cascaded mode.

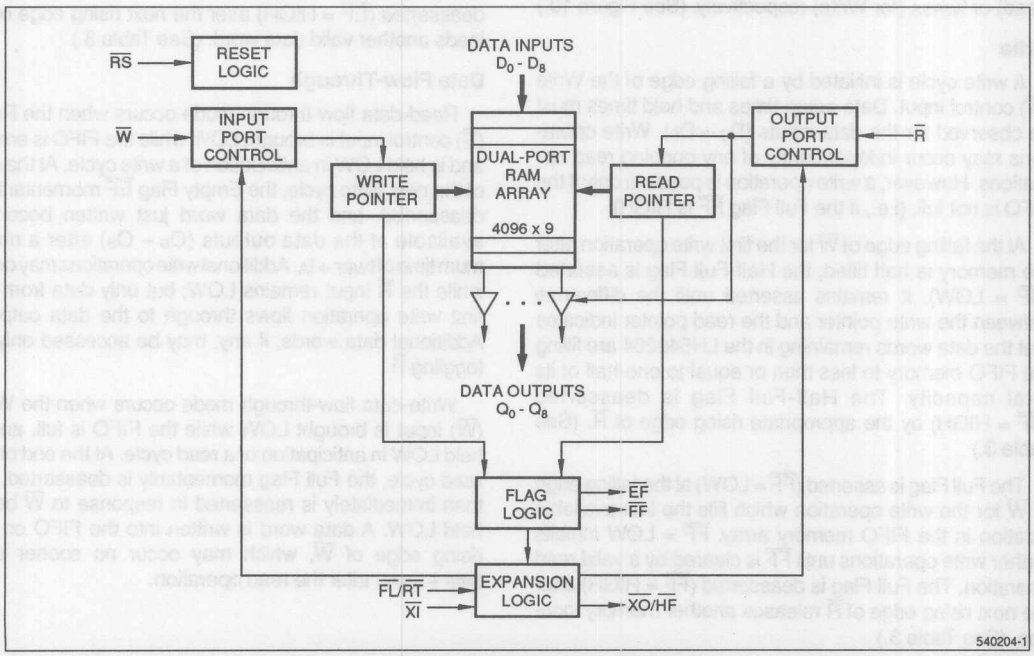


Figure 3. LH540204 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

OPERATIONAL DESCRIPTION

Reset

The LH540204 is reset whenever the Reset input ($\overline{RS}$) is taken LOW. A reset operation initializes both the read-address pointer and the write-address pointer to point to location zero, the first physical memory location. During a reset operation, the state of the $\overline{XI}$ and $\overline{FL}/\overline{RT}$ inputs determines whether the device is in standalone mode or in depth-cascaded mode. (See Tables 1 and 2.)

A reset operation is required whenever the LH540204 first is powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) inputs may be in any state when the reset operation is initiated; but they must be HIGH, before the reset operation is terminated by a rising edge of $\overline{RS}$, by a time t_{RRSS} (for Read) or t_{WRSS} (for Write) respectively. (See Figure 10.)

Write

A write cycle is initiated by a falling edge of the Write ($\overline{W}$) control input. Data setup times and hold times must be observed for the data inputs ($D_0 - D_8$). Write operations may occur independently of any ongoing read operations. However, a write operation is possible only if the FIFO is not full, (i.e., if the Full Flag $\overline{FF}$ is HIGH).

At the falling edge of $\overline{W}$ for the first write operation after the memory is half filled, the Half-Full Flag is asserted ($\overline{HF}$ = LOW). It remains asserted until the difference between the write pointer and the read pointer indicates that the data words remaining in the LH540204 are filling the FIFO memory to less than or equal to one-half of its total capacity. The Half-Full Flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$. (See Table 3.)

The Full Flag is asserted ($\overline{FF}$ = LOW) at the falling edge of $\overline{W}$ for the write operation which fills the last available location in the FIFO memory array. $\overline{FF}$ = LOW inhibits further write operations until $\overline{FF}$ is cleared by a valid read operation. The Full Flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location. (See Table 3.)

Read

A read cycle is initiated by a falling edge of the Read ($\overline{R}$) control input. Read data becomes valid at the data outputs ($Q_0 - Q_8$) after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data outputs return to a high-impedance state. Read operations may occur independently of any ongoing write operations. However, a read operation is possible only if the FIFO is not empty (i.e., if the Empty Flag $\overline{EF}$ is HIGH).

The LH540204's internal read-address and write-address pointers operate in such a way that consecutive read operations always access data words in the same order that they were written. The Empty Flag is asserted ($\overline{EF}$ = LOW) after that falling edge of $\overline{R}$ which accesses the last available data word in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another valid data word. (See Table 3.)

Data Flow-Through

Read-data flow-through mode occurs when the Read ($\overline{R}$) control input is brought LOW while the FIFO is empty, and is held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty Flag $\overline{EF}$ momentarily is deasserted, and the data word just written becomes available at the data outputs ($Q_0 - Q_8$) after a maximum time of $t_{WEF} + t_A$. Additional write operations may occur while the $\overline{R}$ input remains LOW; but only data from the first write operation flows through to the data outputs. Additional data words, if any, may be accessed only by toggling $\overline{R}$.

Write-data flow-through mode occurs when the Write ($\overline{W}$) input is brought LOW while the FIFO is full, and is held LOW in anticipation of a read cycle. At the end of the read cycle, the Full Flag momentarily is deasserted, but then immediately is reasserted in response to $\overline{W}$ being held LOW. A data word is written into the FIFO on the rising edge of $\overline{W}$, which may occur no sooner than $t_{RFF} + t_{WPW}$ after the read operation.

OPERATIONAL DESCRIPTION (cont'd)

Retransmit

The FIFO can be made to reread previously-read data by means of the Retransmit function. A retransmit operation is initiated by pulsing the $\overline{RT}$ input LOW. Both $\overline{R}$ and $\overline{W}$ must be deasserted (HIGH) for the duration of the retransmit pulse. The FIFO's internal read-address pointer is reset to point to location zero, the first physical memory location, while the internal write-address pointer remains unchanged.

After a retransmit operation, those data words in the region in between the read-address pointer and the write-address pointer may be reaccessed by subsequent read operations. A retransmit operation may affect the state of the status flags $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$, depending on the relocation of the read-address pointer. There is no restriction on the number of times that a block of data within an LH540204 may be read out, by repeating the retransmit operation and the subsequent read operations.

The maximum length of a data block which may be retransmitted is 4096 words. Note that if the write-address pointer ever 'wraps around' (i.e., passes location zero more than once) during a sequence of retransmit operations, some data words will be lost.

The Retransmit function is not available when the LH540204 is operating in depth-cascaded mode, because the $\overline{FL}/\overline{RT}$ control pin must be used for first-load selection rather than for retransmission control.

Table 1. Grouping-Mode Determination During a Reset Operation

$\overline{XI}$	$\overline{FL}/\overline{RT}$	MODE	$\overline{XO}/\overline{HF}$ USAGE	$\overline{XI}$ USAGE	$\overline{FL}/\overline{RT}$ USAGE
H [1]	H	Cascaded Slave [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
H [1]	L	Cascaded Master [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
L	X	Standalone	$\overline{HF}$	(none)	$\overline{RT}$

NOTES:
1. A reset operation forces $\overline{XO}$ HIGH for the nth FIFO, thus forcing $\overline{XI}$ HIGH for the n+1st FIFO.
2. The terms 'master' and 'slave' refer to operation in depth-cascaded grouping mode.
3. H = HIGH; L = LOW; X = Don't Care.

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	STANDALONE	CASCADED MASTER	CASCADED SLAVE
I	$\overline{XI}$	Grounded	From $\overline{XO}$ (n-1st FIFO)	From $\overline{XO}$ (n-1st FIFO)
O	$\overline{XO}/\overline{HF}$	Becomes $\overline{HF}$	To $\overline{XI}$ (n+1st FIFO)	To $\overline{XI}$ (n+1st FIFO)
I	$\overline{FL}/\overline{RT}$	Becomes $\overline{RT}$	Grounded (Logic LOW)	Logic HIGH

Table 3. Status Flags

NUMBER OF UNREAD DATA WORDS PRESENT WITHIN 4096 × 9 FIFO	$\overline{FF}$	$\overline{HF}$	$\overline{EF}$
0	H	H	L
1 to 2048	H	H	H
2049 to 4095	H	L	H
4096	L	L	H

OPERATIONAL MODES

Standalone Configuration

When depth cascading is not required for a given application, the LH540204 is placed in standalone mode by tying the Expansion In input ($\overline{XI}$) to ground. This input is internally sampled during a reset operation. (See Table 1.)

Width Expansion

Word-width expansion is implemented by placing multiple LH540204 devices in parallel. Each LH540204 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 4, 5, and 6.)

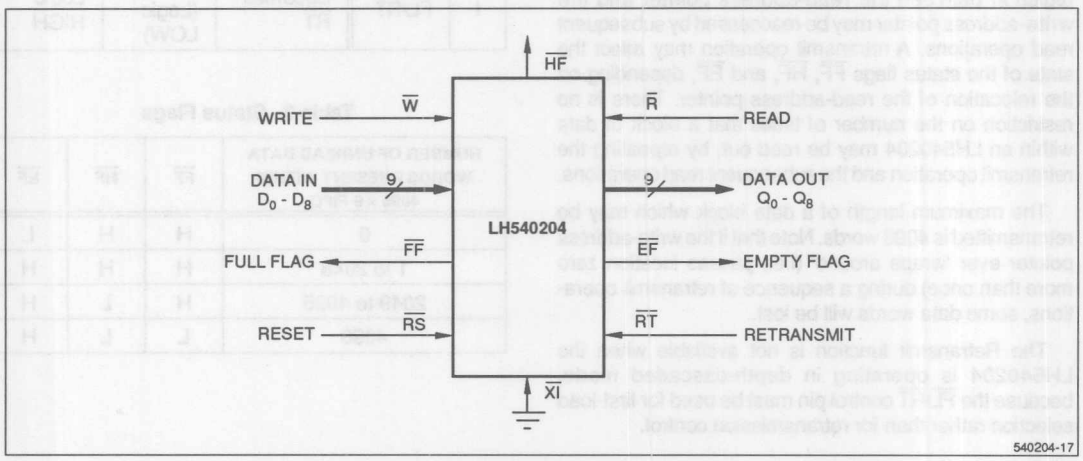


Figure 4. Standalone FIFO (4096 × 9)

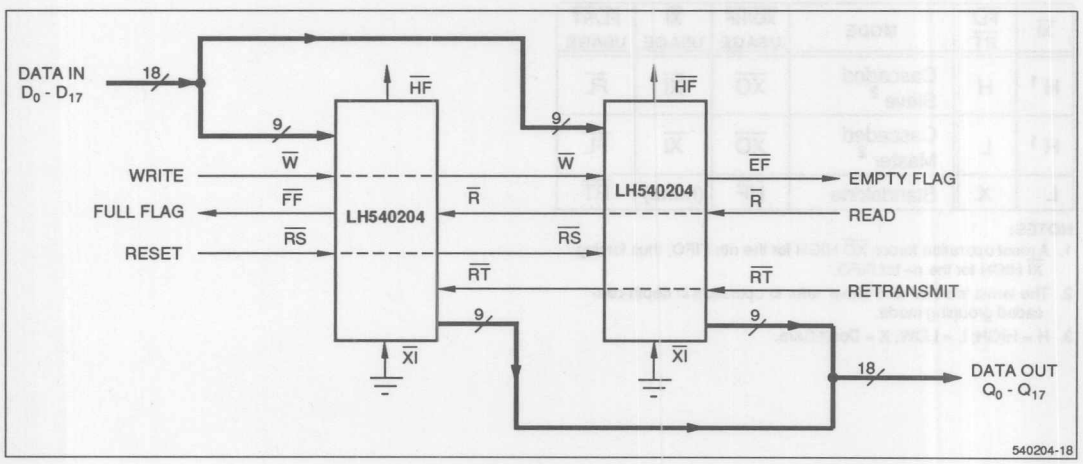


Figure 5. FIFO Word-Width Expansion (4096 × 18)

OPERATIONAL MODES (cont'd)

Depth Cascading

Depth cascading is implemented by configuring the required number of LH540204s in depth-cascaded mode. In this arrangement, the FIFOs are connected in a circular fashion, with the Expansion Out output ($\overline{XO}$) of each device tied to the Expansion In input ($\overline{XI}$) of the next device. One FIFO in the cascade must be designated as the 'first-load' device, by tying its First Load input ($\overline{FL}/\overline{RT}$) to ground. All other devices must have their $\overline{FL}/\overline{RT}$ inputs tied HIGH. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while logic within each LH540204 controls the steering of data. Only one LH540204 is enabled during any given write cycle; thus, the common Data In inputs of all devices are tied together. Likewise, only one LH540204 is enabled during any given read cycle; thus, the common Data Out outputs of all devices are wire-ORed together.

In depth-cascaded mode, external logic should be used to generate a composite Full Flag and a composite Empty Flag, by ANDing the $\overline{FF}$ outputs of all LH540204 devices together and ANDing the $\overline{EF}$ outputs of all devices together. Since $\overline{FF}$ and $\overline{EF}$ are assertive-LOW signals, this 'ANDing' actually is implemented using an assertive-HIGH physical OR gate. The Half-Full Flag and the Retransmit function are not available in depth-cascaded mode.

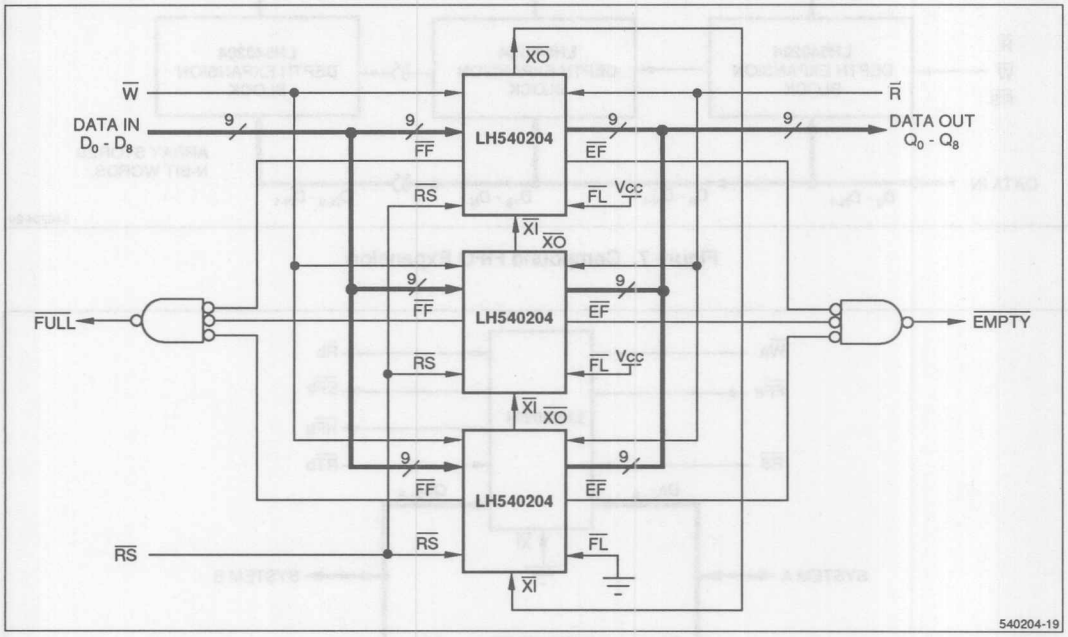


Figure 6. FIFO Depth Cascading (12288 × 9)

OPERATIONAL MODES (cont'd)

Compound FIFO Expansion

A combination of word-width expansion and depth cascading may be implemented easily by operating groups of depth-cascaded FIFOs in parallel.

Bidirectional FIFO Operation

Bidirectional data buffering between two systems may be implemented by operating LH540204 devices in parallel, but in opposite directions. The Data In inputs of each LH540204 are tied to the corresponding Data Out outputs of another LH540204, which is operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both word-width expansion and depth cascading may be used in bidirectional applications.

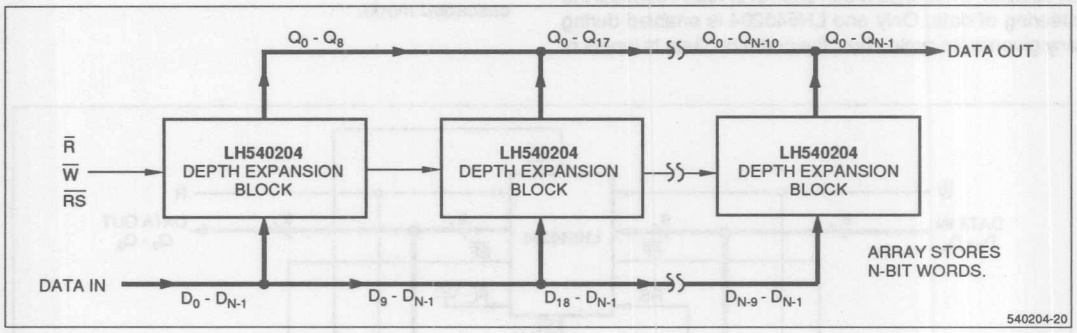


Figure 7. Compound FIFO Expansion

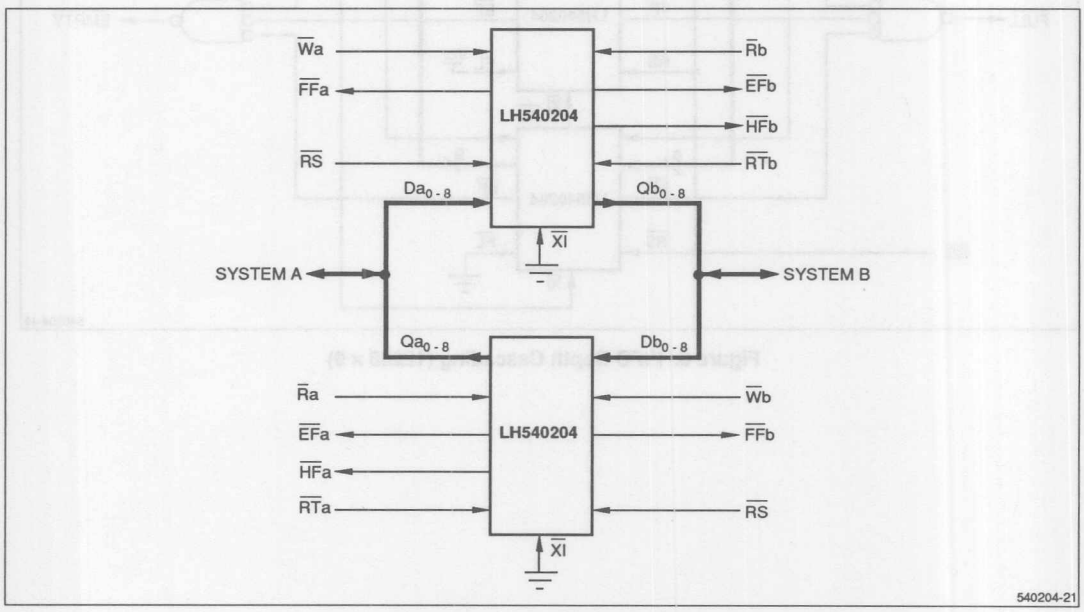


Figure 8. Bidirectional FIFO Operation (4096 × 9 × 2)

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [2]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside of those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

NOTES:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ V_{OUT} ≤ V_{CC}	−10	10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		110	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		8	mA

NOTES:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 9

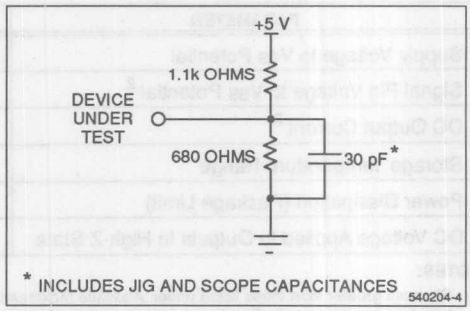


Figure 9. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
C_O MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz, with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS) [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING														
t_{RC}	Read Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Held Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING														
t_{WC}	Write Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING														
t_{RSC}	Reset Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	65		80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	65		80	–	ns
RETRANSMIT TIMING [5]														
t_{RTC}	Retransmit Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING														
t_{EFL}	Reset LOW to Empty Flag LOW	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset HIGH to Half-Full and Full Flags HIGH	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	20	–	25	–	35	–	45	–	60	–	60	ns
EXPANSION TIMING														
t_{XOL}	Expansion Out LOW	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements are performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values are guaranteed by design; not currently tested.
4. Only applies to read-data flow-through mode.
5. See also Note 2, Figure 19.

TIMING DIAGRAMS

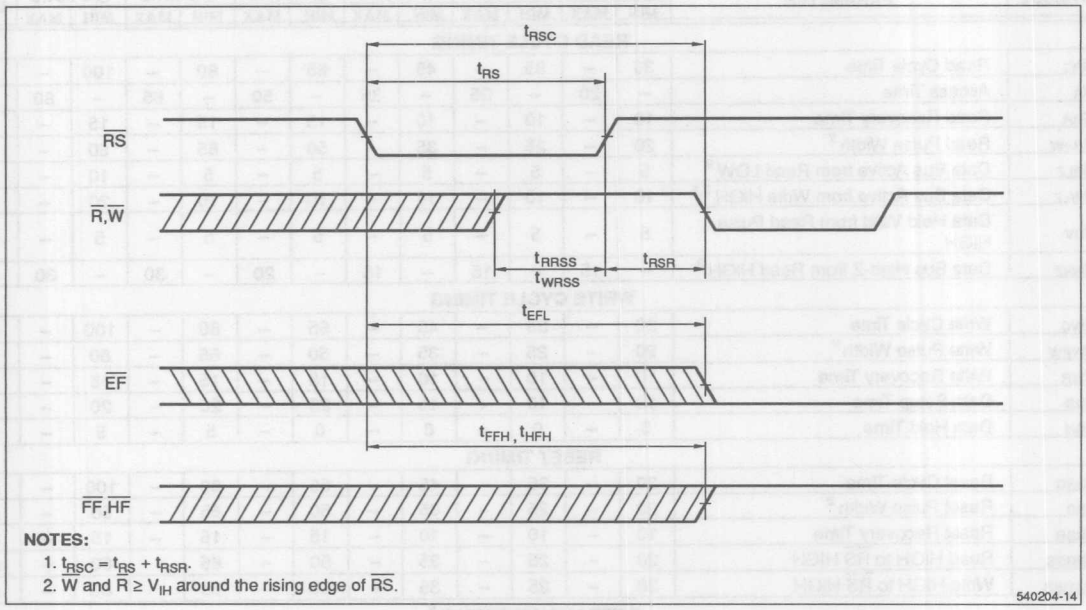


Figure 10. Reset Timing

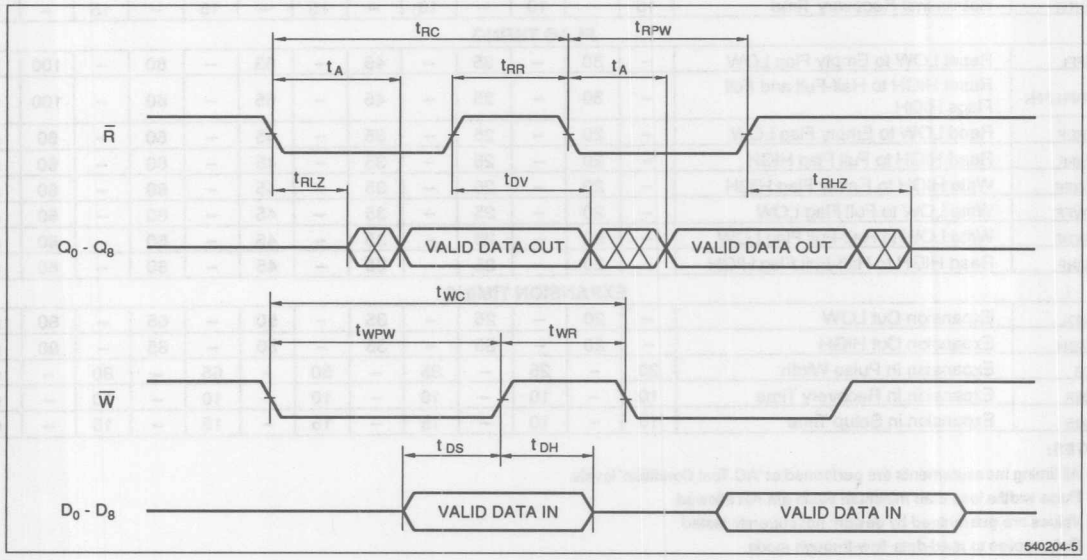


Figure 11. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

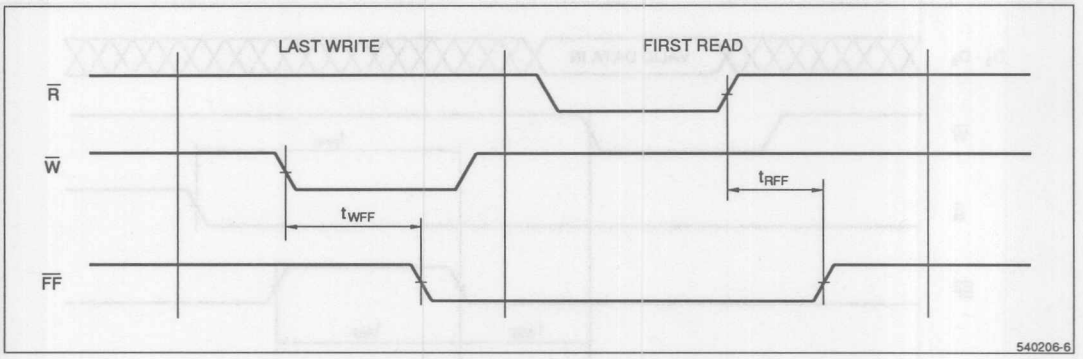


Figure 12. Full Flag From Last Write to First Read

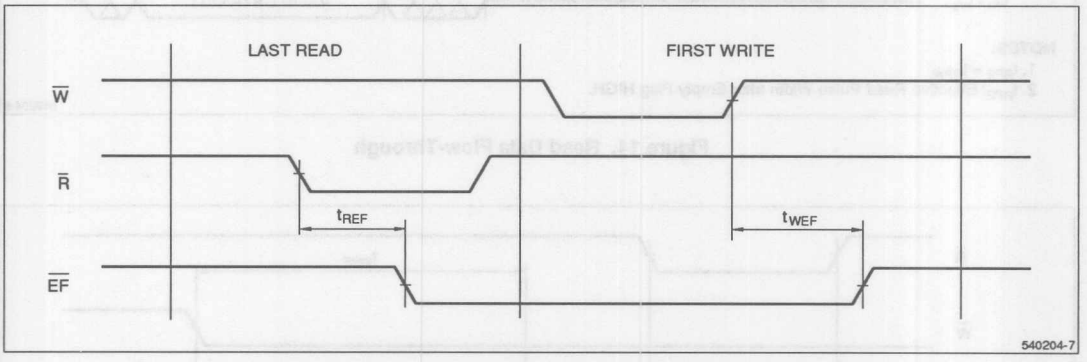


Figure 13. Empty Flag From Last Read to First Write

TIMING DIAGRAMS (cont'd)

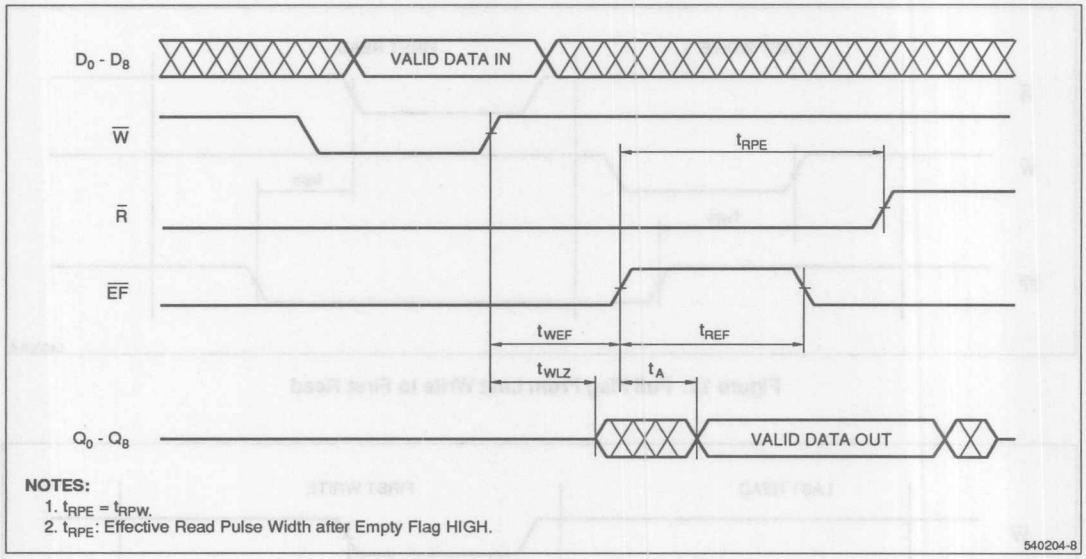


Figure 14. Read Data Flow-Through

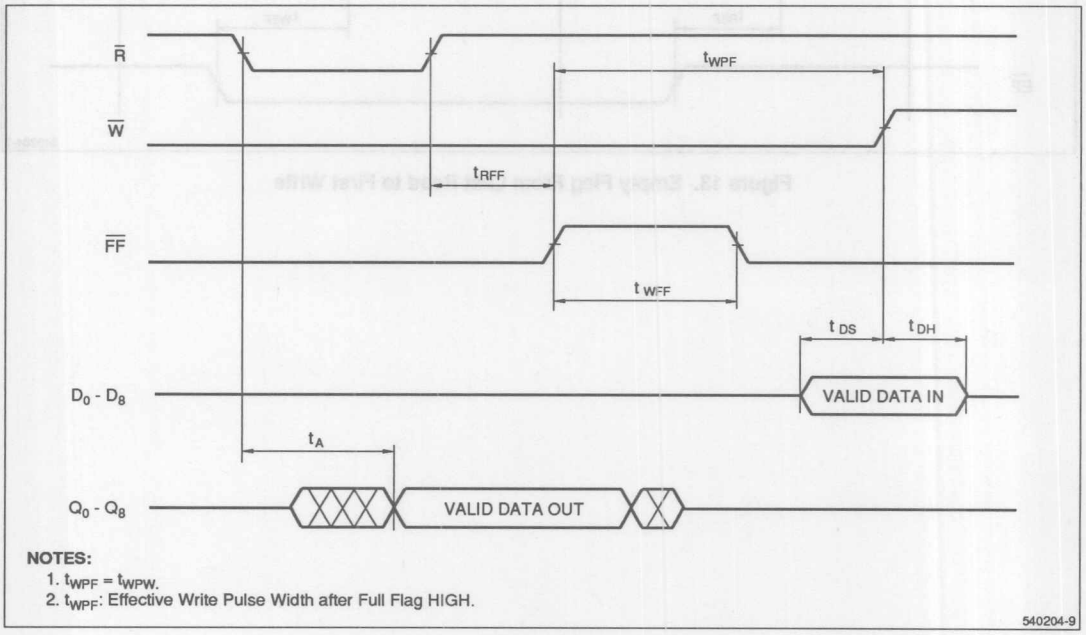
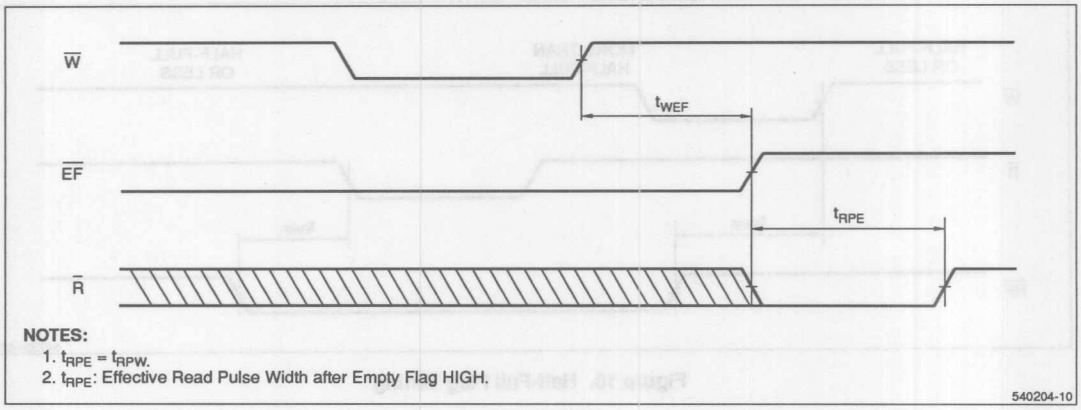


Figure 15. Write Data Flow-Through

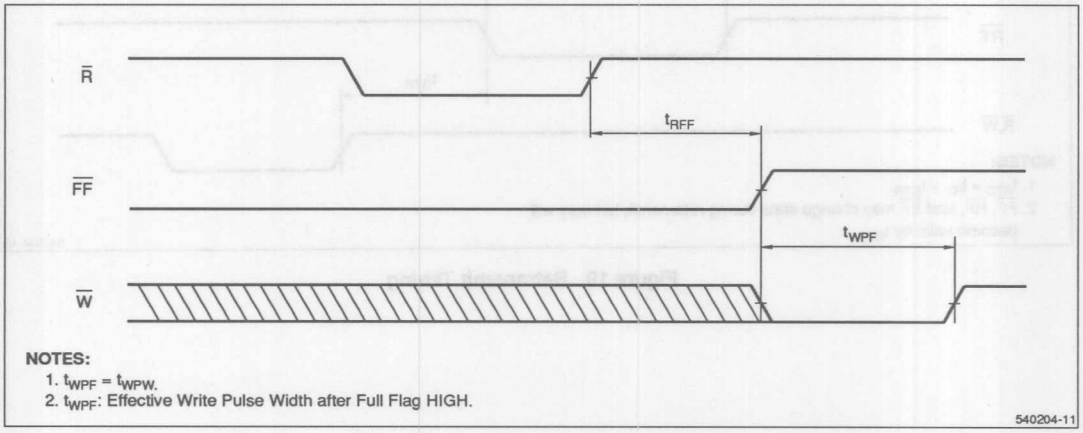
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540204-10

Figure 16. Empty Flag Timing



NOTES:
1. $t_{WPF} = t_{WPW}$.
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540204-11

Figure 17. Full Flag Timing

TIMING DIAGRAMS (cont'd)

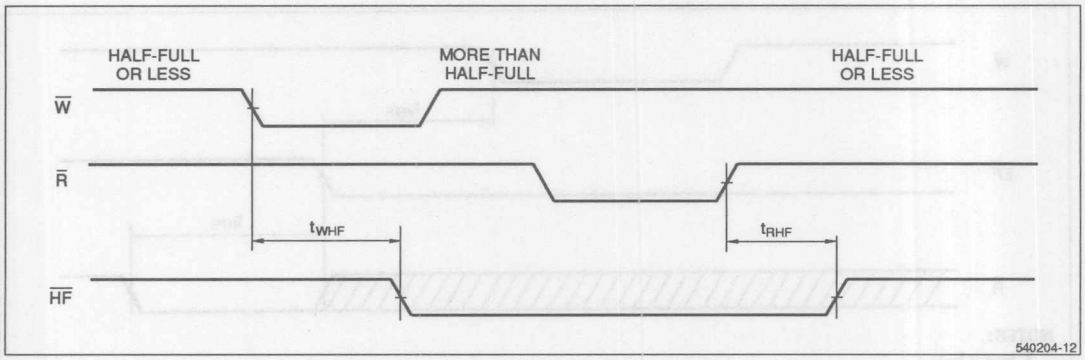


Figure 18. Half-Full Flag Timing

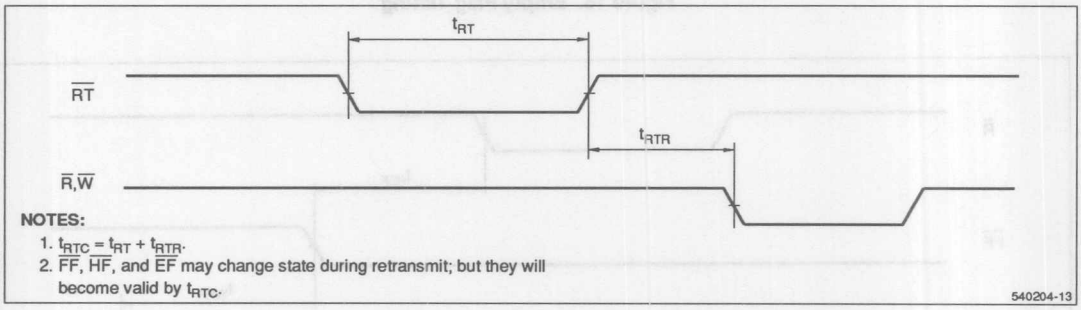


Figure 19. Retransmit Timing

TIMING DIAGRAMS (cont'd)

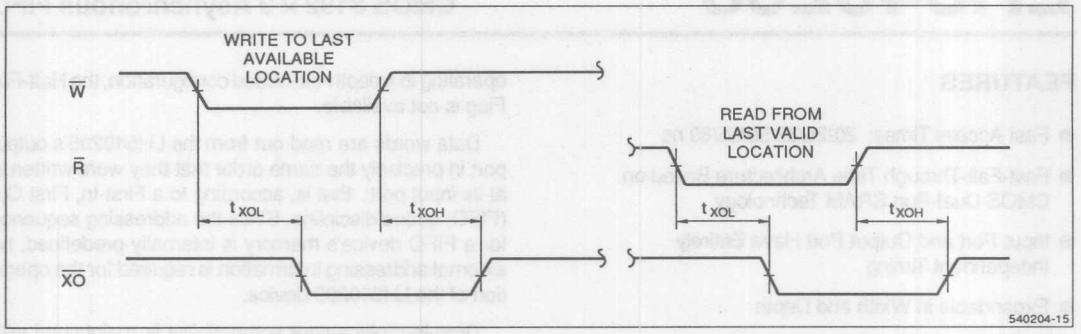


Figure 20. Expansion-Out Timing

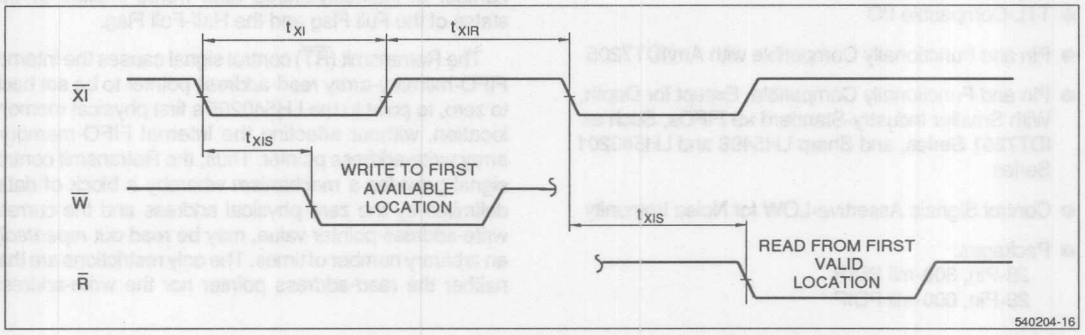


Figure 21. Expansion-In Timing

ORDERING INFORMATION

LH540204 — Device Type
X — Package
- ## — Speed

Speed:
- 20
- 25
- 35
- 50
- 65
- 80

Access Time (ns)

Package:
- Blank 28-pin, 600-mil Plastic DIP * (DIP28-P-600)
- D 28-pin, 300-mil Plastic DIP (DIP28-W-300)
- K 28-pin, 300-mil SOJ * (SOJ28-P-300)
- U 32-pin Plastic Leaded Chip Carrier (PLCC32-P-R450)

Device Type: CMOS 4096 x 9 FIFO

* This is an Advance information data sheet; except that all references to the 600-mil Plastic DIP and SOJ packages still have Product Preview status.

Example: LH540204U-25 (CMOS 4096 x 9 FIFO, 32-pin PLCC, 25 ns)

540204MD

LH540205

ADVANCE INFORMATION

CMOS 8192 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 20/25/35/50/65/80 ns
- Fast-Fall-Through Time Architecture Based on CMOS Dual-Port SRAM Technology
- Input Port and Output Port Have Entirely Independent Timing
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Data Retransmission Capability
- TTL-Compatible I/O
- Pin and Functionally Compatible with Am/IDT7205
- Pin and Functionally Compatible, Except for Depth, With Smaller Industry-Standard ×9 FIFOs, Such as IDT7201 Series, and Sharp LH5496 and LH540201 Series
- Control Signals Assertive-LOW for Noise Immunity
- Packages:
  28-Pin, 300-mil PDIP
  28-Pin, 600-mil PDIP *

FUNCTIONAL DESCRIPTION

The LH540205 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 8192 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit LH540205 word may consist of a standard eight-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the LH540205 becomes either totally full or else totally empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full LH540205, or by attempting to read additional words from an already-empty LH540205. When an LH540205 is operating in a depth-cascaded configuration, the Half-Full Flag is not available.

Data words are read out from the LH540205's output port in precisely the same order that they were written in at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the LH540205 device.

Drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO-memory-array read-address pointer to be set back to zero, to point to the LH540205's first physical memory location, without affecting the internal FIFO-memory-array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address-pointer value, may be read out *repeatedly* an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address

PIN CONNECTIONS

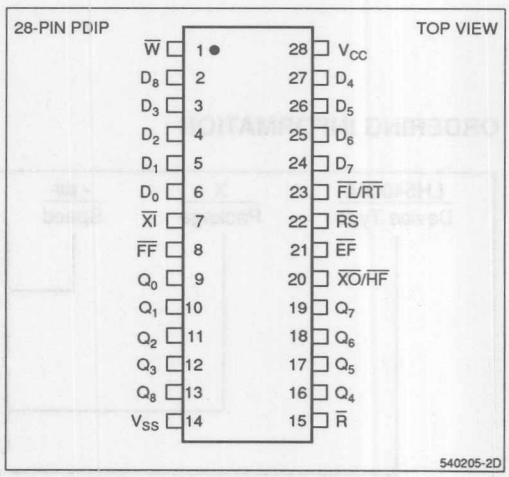


Figure 1. Pin Connections for PDIP Package

* This is an Advance Information data sheet; except that all references to the 600-mil PDIP still have Product Preview status.

FUNCTIONAL DESCRIPTION (cont'd)

pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an LH540205 is operating in a depth-expanded configuration.

The Reset ($\overline{RS}$) control signal returns the LH540205 to an initial state, empty and ready to be filled. An LH540205 should be reset during every system power-up sequence. A reset operation causes the internal FIFO-memory-array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the LH540205's first physical memory location. Any information which previously had been stored within the LH540205 is not recoverable after a reset operation.

A cascading (depth-expansion) scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}/\overline{HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual LH540205 devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one LH540205 device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL}/\overline{RT}$) control input; the remaining LH540205 devices are designated as 'slaves,' by tying their $\overline{FL}/\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' LH540205 devices operating in cascaded mode.

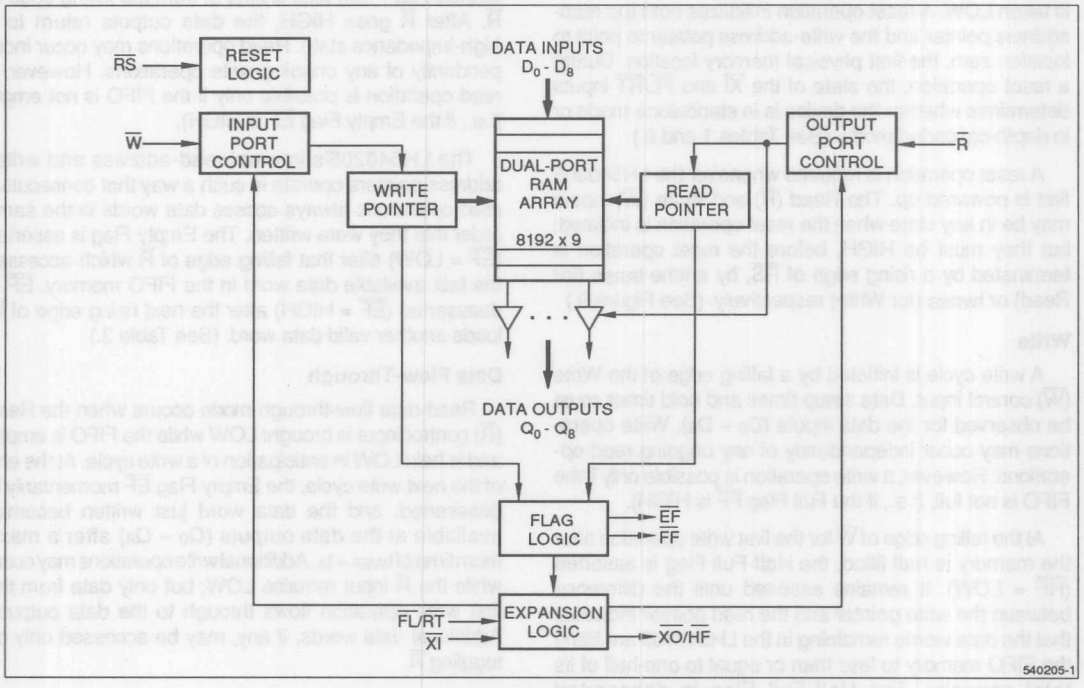


Figure 2. LH54205 Block Diagram

PIN DESCRIPTIONS

PIN	PIN TYPE *	DESCRIPTION
$D_0 - D_8$	I	Input Data Bus
$Q_0 - Q_8$	O/Z	Output Data Bus
$\overline{W}$	I	Write Request
$\overline{R}$	I	Read Request
$\overline{EF}$	O	Empty Flag
$\overline{FF}$	O	Full Flag
$\overline{XO}/\overline{HF}$	O	Expansion Out/Half-Full Flag
$\overline{XI}$	I	Expansion In
$\overline{FL}/\overline{RT}$	I	First Load/Retransmit
$\overline{RS}$	I	Reset
V_{CC}	V	Positive Power Supply
V_{SS}	V	Ground

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

OPERATIONAL DESCRIPTION

Reset

The LH540205 is reset whenever the Reset input ($\overline{RS}$) is taken LOW. A reset operation initializes both the read-address pointer and the write-address pointer to point to location zero, the first physical memory location. During a reset operation, the state of the $\overline{XI}$ and $\overline{FL}/\overline{RT}$ inputs determines whether the device is in standalone mode or in depth-cascaded mode. (See Tables 1 and 2.)

A reset operation is required whenever the LH540205 first is powered up. The Read ($\overline{R}$) and Write ($\overline{W}$) inputs may be in any state when the reset operation is initiated; but they must be HIGH, before the reset operation is terminated by a rising edge of $\overline{RS}$, by a time t_{RRSS} (for Read) or t_{WRSS} (for Write) respectively. (See Figure 9.)

Write

A write cycle is initiated by a falling edge of the Write ($\overline{W}$) control input. Data setup times and hold times must be observed for the data inputs ($D_0 - D_8$). Write operations may occur independently of any ongoing read operations. However, a write operation is possible only if the FIFO is not full, (i.e., if the Full Flag $\overline{FF}$ is HIGH).

At the falling edge of $\overline{W}$ for the first write operation after the memory is half filled, the Half-Full Flag is asserted ($\overline{HF}$ = LOW). It remains asserted until the difference between the write pointer and the read pointer indicates that the data words remaining in the LH540205 are filling the FIFO memory to less than or equal to one-half of its total capacity. The Half-Full Flag is deasserted ($\overline{HF}$ = HIGH) by the appropriate rising edge of $\overline{R}$. (See Table 3.)

The Full Flag is asserted ($\overline{FF}$ = LOW) at the falling edge of $\overline{W}$ for the write operation which fills the last available location in the FIFO memory array. $\overline{FF}$ = LOW inhibits further write operations until $\overline{FF}$ is cleared by a valid read operation. The Full Flag is deasserted ($\overline{FF}$ = HIGH) after the next rising edge of $\overline{R}$ releases another memory location. (See Table 3.)

Read

A read cycle is initiated by a falling edge of the Read ($\overline{R}$) control input. Read data becomes valid at the data outputs ($Q_0 - Q_8$) after a time t_A from the falling edge of $\overline{R}$. After $\overline{R}$ goes HIGH, the data outputs return to a high-impedance state. Read operations may occur independently of any ongoing write operations. However, a read operation is possible only if the FIFO is not empty (i.e., if the Empty Flag $\overline{EF}$ is HIGH).

The LH540205's internal read-address and write-address pointers operate in such a way that consecutive read operations always access data words in the same order that they were written. The Empty Flag is asserted ($\overline{EF}$ = LOW) after that falling edge of $\overline{R}$ which accesses the last available data word in the FIFO memory. $\overline{EF}$ is deasserted ($\overline{EF}$ = HIGH) after the next rising edge of $\overline{W}$ loads another valid data word. (See Table 3.)

Data Flow-Through

Read-data flow-through mode occurs when the Read ($\overline{R}$) control input is brought LOW while the FIFO is empty, and is held LOW in anticipation of a write cycle. At the end of the next write cycle, the Empty Flag $\overline{EF}$ momentarily is deasserted, and the data word just written becomes available at the data outputs ($Q_0 - Q_8$) after a maximum time of $t_{WEF} + t_A$. Additional write operations may occur while the $\overline{R}$ input remains LOW; but only data from the first write operation flows through to the data outputs. Additional data words, if any, may be accessed only by toggling $\overline{R}$.

Write-data flow-through mode occurs when the Write ($\overline{W}$) input is brought LOW while the FIFO is full, and is held LOW in anticipation of a read cycle. At the end of the read cycle, the Full Flag momentarily is deasserted, but then immediately is reasserted in response to $\overline{W}$ being held LOW. A data word is written into the FIFO on the rising edge of $\overline{W}$, which may occur no sooner than $t_{RFF} + t_{WPW}$ after the read operation.

OPERATIONAL DESCRIPTION (cont'd)

Retransmit

The FIFO can be made to reread previously-read data by means of the Retransmit function. A retransmit operation is initiated by pulsing the $\overline{RT}$ input LOW. Both $\overline{R}$ and $\overline{W}$ must be deasserted (HIGH) for the duration of the retransmit pulse. The FIFO's internal read-address pointer is reset to point to location zero, the first physical memory location, while the internal write-address pointer remains unchanged.

After a retransmit operation, those data words in the region in between the read-address pointer and the write-address pointer may be reaccessed by subsequent read operations. A retransmit operation may affect the state of the status flags $\overline{FF}$, $\overline{HF}$, and $\overline{EF}$, depending on the relocation of the read-address pointer. There is no restriction on the number of times that a block of data within an LH540205 may be read out, by repeating the retransmit operation and the subsequent read operations.

The maximum length of a data block which may be retransmitted is 8192 words. Note that if the write-address pointer ever 'wraps around' (i.e., passes location zero more than once) during a sequence of retransmit operations, some data words will be lost.

The Retransmit function is not available when the LH540205 is operating in depth-cascaded mode, because the $\overline{FL}/\overline{RT}$ control pin must be used for first-load selection rather than for retransmission control.

Table 1. Grouping-Mode Determination During a Reset Operation

$\overline{XI}$	$\overline{FL}/\overline{RT}$	MODE	$\overline{XO}/\overline{HF}$ USAGE	$\overline{XI}$ USAGE	$\overline{FL}/\overline{RT}$ USAGE
H [1]	H	Cascaded Slave [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
H [1]	L	Cascaded Master [2]	$\overline{XO}$	$\overline{XI}$	$\overline{FL}$
L	X	Standalone	$\overline{HF}$	(none)	$\overline{RT}$

NOTES:
1. A reset operation forces $\overline{XO}$ HIGH for the nth FIFO, thus forcing $\overline{XI}$ HIGH for the n+1st FIFO.
2. The terms 'master' and 'slave' refer to operation in depth-cascaded grouping mode.
3. H = HIGH; L = LOW; X = Don't Care.

Table 2. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	STANDALONE	CASCADED MASTER	CASCADED SLAVE
I	$\overline{XI}$	Grounded	From $\overline{XO}$ (n-1st FIFO)	From $\overline{XO}$ (n-1st FIFO)
O	$\overline{XO}/\overline{HF}$	Becomes $\overline{HF}$	To $\overline{XI}$ (n+1st FIFO)	To $\overline{XI}$ (n+1st FIFO)
I	$\overline{FL}/\overline{RT}$	Becomes $\overline{RT}$	Grounded (Logic LOW)	Logic HIGH

Table 3. Status Flags

NUMBER OF UNREAD DATA WORDS PRESENT WITHIN 8192 × 9 FIFO	$\overline{FF}$	$\overline{HF}$	$\overline{EF}$
0	H	H	L
1 to 4096	H	H	H
4097 to 8191	H	L	H
8192	L	L	H

OPERATIONAL MODES

Standalone Configuration

When depth cascading is not required for a given application, the LH540205 is placed in standalone mode by tying the Expansion In input ($\overline{XI}$) to ground. This input is internally sampled during a reset operation. (See Table 1.)

Width Expansion

Word-width expansion is implemented by placing multiple LH540205 devices in parallel. Each LH540205 should be configured for standalone mode. In this arrangement, the behavior of the status flags is identical for all devices; so, in principle, a representative value for each of these flags could be derived from any one device. In practice, it is better to derive 'composite' flag values using external logic, since there may be minor speed variations between different actual devices. (See Figures 3 and 4.)

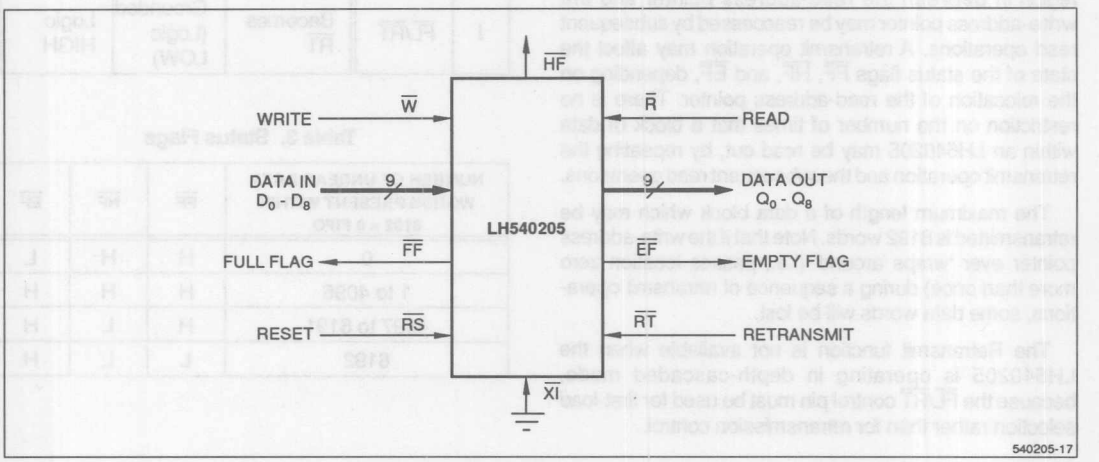


Figure 3. Standalone FIFO (8192 × 9)

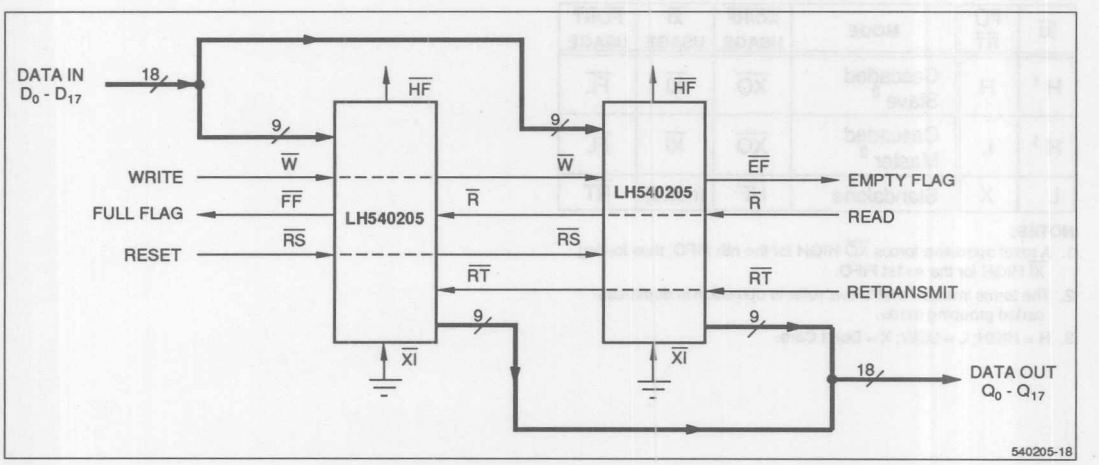


Figure 4. FIFO Word-Width Expansion (8192 × 18)

OPERATIONAL MODES (cont'd)

Depth Cascading

Depth cascading is implemented by configuring the required number of LH540205s in depth-cascaded mode. In this arrangement, the FIFOs are connected in a circular fashion, with the Expansion Out output ($\overline{XO}$) of each device tied to the Expansion In input ($\overline{XI}$) of the next device. One FIFO in the cascade must be designated as the 'first-load' device, by tying its First Load input ($\overline{FL}/\overline{RT}$) to ground. All other devices must have their $\overline{FL}/\overline{RT}$ inputs tied HIGH. In this mode, $\overline{W}$ and $\overline{R}$ signals are shared by all devices, while logic within each LH540205 controls the steering of data. Only one LH540205 is enabled during any given write cycle; thus, the common Data In inputs of all devices are tied together. Likewise, only one LH540205 is enabled during any given read cycle; thus, the common Data Out outputs of all devices are wire-ORed together

In depth-cascaded mode, external logic should be used to generate a composite Full Flag and a composite Empty Flag, by ANDing the $\overline{FF}$ outputs of all LH540205 devices together and ANDing the $\overline{EF}$ outputs of all devices together. Since $\overline{FF}$ and $\overline{EF}$ are assertive-LOW signals, this 'ANDing' actually is implemented using an assertive-HIGH physical OR gate. The Half-Full Flag and the Retransmit function are not available in depth-cascaded mode.

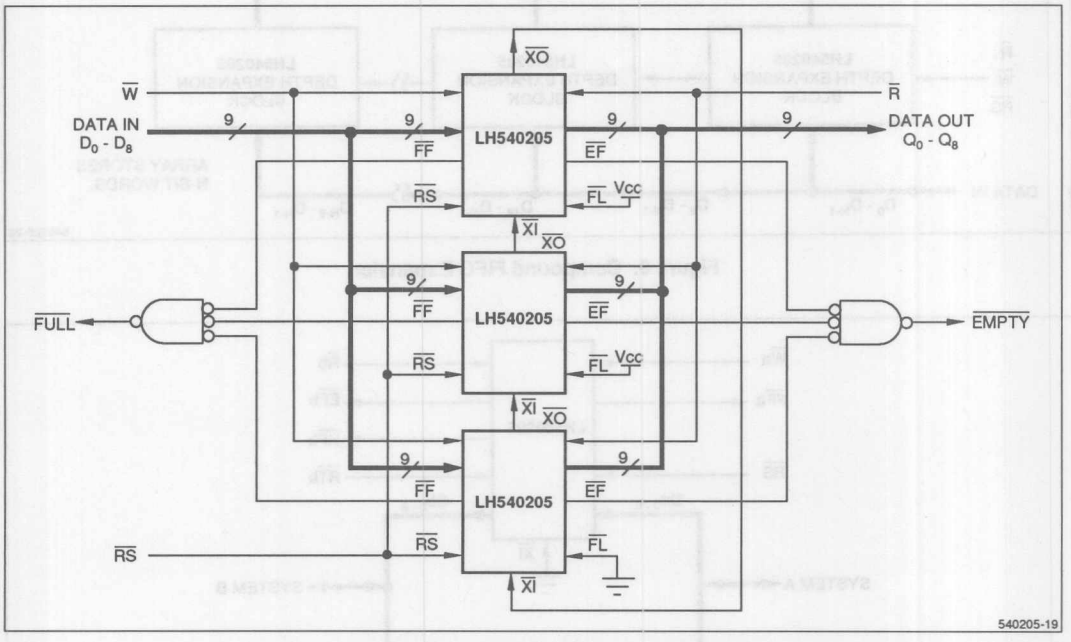


Figure 5. FIFO Depth Cascading (24576 × 9)

OPERATIONAL MODES (cont'd)

Compound FIFO Expansion

A combination of word-width expansion and depth cascading may be implemented easily by operating groups of depth-cascaded FIFOs in parallel.

Bidirectional FIFO Operation

Bidirectional data buffering between two systems may be implemented by operating LH540205 devices in parallel, but in opposite directions. The Data In inputs of each LH540205 are tied to the corresponding Data Out outputs of another LH540205, which is operating in the opposite direction, to form a single bidirectional bus interface. Care must be taken to assure that the appropriate read, write, and flag signals are routed to each system. Both word-width expansion and depth cascading may be used in bidirectional applications.

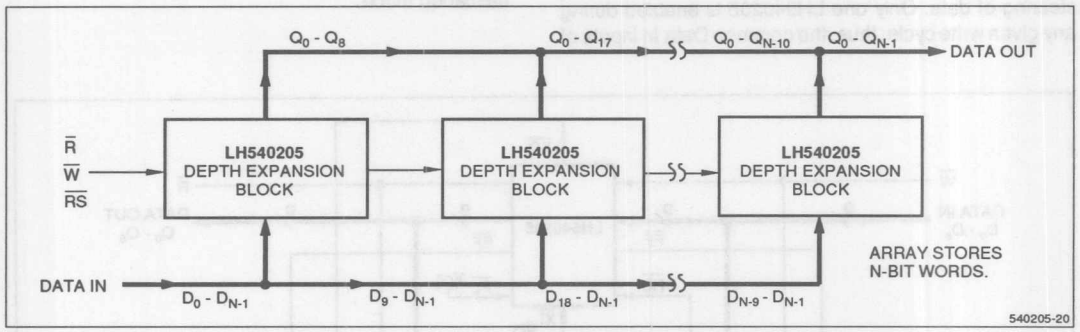


Figure 6. Compound FIFO Expansion

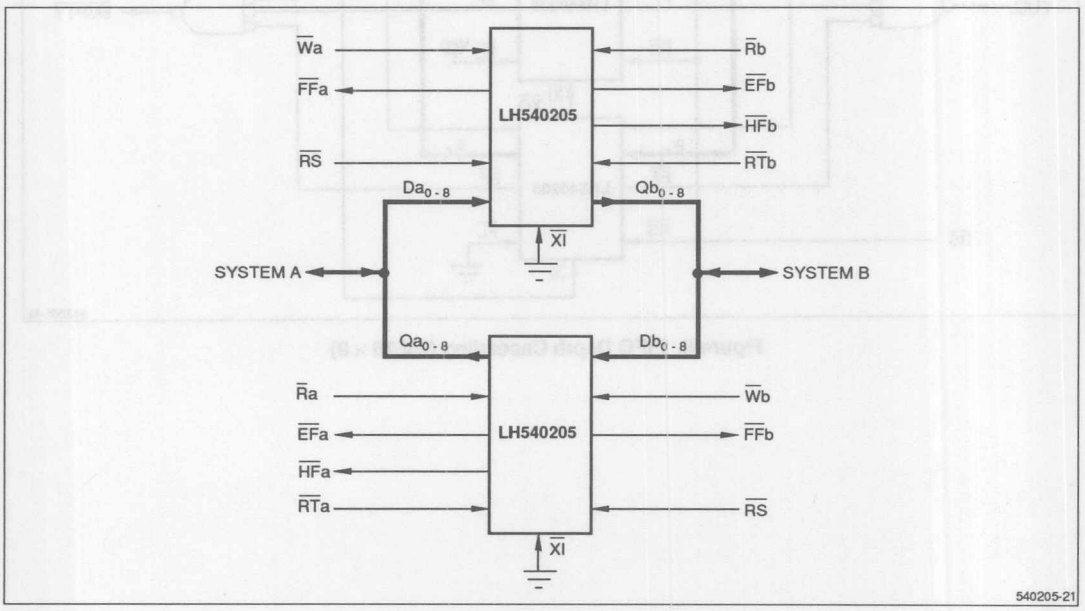


Figure 7. Bidirectional FIFO Operation (8192 × 9 × 2)

ABSOLUTE MAXIMUM RATINGS [1]

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential [2]	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)
DC Output Current [3]	± 50 mA
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	1.0 W
DC Voltage Applied to Outputs In High-Z State	−0.5 V to V_{CC} + 0.5 V (not to exceed 7 V)

NOTES:

1. Stresses greater than those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating for transient conditions only. Functional operation of the device at these or any other conditions outside of those indicated in the 'Operating Range' of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.
3. Outputs should not be shorted for more than 30 seconds. No more than one output should be shorted at any time.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	°C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage [1]	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

NOTES:

1. Negative undershoots of 1.5 V in amplitude are permitted for up to 10 ns once per cycle.

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage Current	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−10	10	µA
I_{LO}	Output Leakage Current	$\overline{R} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−10	10	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −2.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 8.0 mA		0.4	V
I_{CC}	Average Supply Current [1]	Measured at f = 40 MHz		110	mA
I_{CC2}	Average Standby Current [1]	All Inputs = V_{IH}		15	mA
I_{CC3}	Power Down Current [1]	All Inputs = V_{CC} − 0.2V		8	mA

NOTES:

1. I_{CC}, I_{CC2}, and I_{CC3} are dependent upon actual output loading and cycle rates. Specified values are with outputs open.

AC TEST CONDITIONS

PARAMETER	RATING
Input Pulse Levels	Vss to 3 V
Input Rise and Fall Times (10% to 90%)	5 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load, Timing Tests	Figure 8

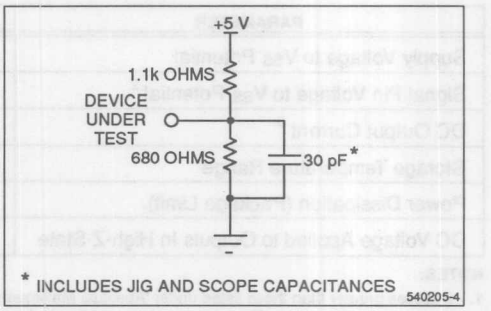


Figure 8. Output Load Circuit

CAPACITANCE [1,2]

PARAMETER	RATING
C_{IN} MAX (Input Capacitance)	5 pF
C_O MAX (Output Capacitance)	7 pF

NOTES:

1. Sample tested only.
2. Capacitances are maximum values at 25°C, measured at 1.0MHz, with V_{IN} = 0 V.

AC ELECTRICAL CHARACTERISTICS) [1] (Over Operating Range)

SYMBOL	PARAMETER	t_A = 20 ns		t_A = 25 ns		t_A = 35 ns		t_A = 50 ns		t_A = 65 ns		t_A = 80 ns		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
READ CYCLE TIMING														
t_{RC}	Read Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_A	Access Time	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{RR}	Read Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RPW}	Read Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RLZ}	Data Bus Active from Read LOW [3]	5	–	5	–	5	–	5	–	5	–	10	–	ns
t_{WLZ}	Data Bus Active from Write HIGH [3,4]	10	–	10	–	10	–	10	–	10	–	20	–	ns
t_{DV}	Data Held Valid from Read Pulse HIGH	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{RHZ}	Data Bus High-Z from Read HIGH [3]	–	15	–	15	–	15	–	20	–	30	–	30	ns
WRITE CYCLE TIMING														
t_{WC}	Write Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{WPW}	Write Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{WR}	Write Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{DS}	Data Setup Time	10	–	10	–	15	–	20	–	20	–	20	–	ns
t_{DH}	Data Hold Time	0	–	0	–	0	–	0	–	5	–	5	–	ns
RESET TIMING														
t_{RSC}	Reset Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RS}	Reset Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RSR}	Reset Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
t_{RRSS}	Read HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	65		80	–	ns
t_{WRSS}	Write HIGH to $\overline{RS}$ HIGH	20	–	25	–	35	–	50	–	65		80	–	ns
RETRANSMIT TIMING [5]														
t_{RTC}	Retransmit Cycle Time	30	–	35	–	45	–	65	–	80	–	100	–	ns
t_{RT}	Retransmit Pulse Width [2]	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{RTR}	Retransmit Recovery Time	10	–	10	–	10	–	15	–	15	–	15	–	ns
FLAG TIMING														
t_{EFL}	Reset LOW to Empty Flag LOW	–	30	–	35	–	45	–	65	–	80	–	100	ns
$t_{HFH,FFH}$	Reset HIGH to Half-Full and Full Flags HIGH	–	30	–	35	–	45	–	65	–	80	–	100	ns
t_{REF}	Read LOW to Empty Flag LOW	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{RFF}	Read HIGH to Full Flag HIGH	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WEF}	Write HIGH to Empty Flag HIGH	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WFF}	Write LOW to Full Flag LOW	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{WHF}	Write LOW to Half-Full Flag LOW	–	20	–	25	–	35	–	45	–	60	–	60	ns
t_{RHF}	Read HIGH to Half-Full Flag HIGH	–	20	–	25	–	35	–	45	–	60	–	60	ns
EXPANSION TIMING														
t_{XOL}	Expansion Out LOW	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XOH}	Expansion Out HIGH	–	20	–	25	–	35	–	50	–	65	–	80	ns
t_{XI}	Expansion In Pulse Width	20	–	25	–	35	–	50	–	65	–	80	–	ns
t_{XIR}	Expansion In Recovery Time	10	–	10	–	10	–	10	–	10	–	10	–	ns
t_{XIS}	Expansion in Setup Time	10	–	10	–	15	–	15	–	15	–	15	–	ns

NOTES:

1. All timing measurements are performed at 'AC Test Condition' levels.
2. Pulse widths less than minimum value are not allowed.
3. Values are guaranteed by design; not currently tested.
4. Only applies to read-data flow-through mode.
5. See also Note 2, Figure 18.

TIMING DIAGRAMS

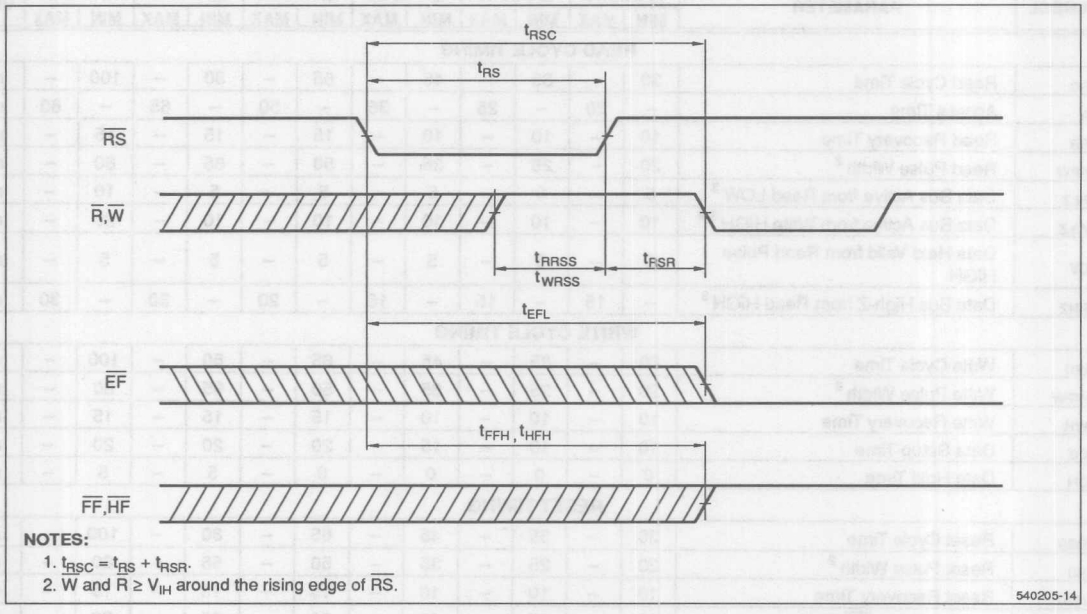


Figure 9. Reset Timing

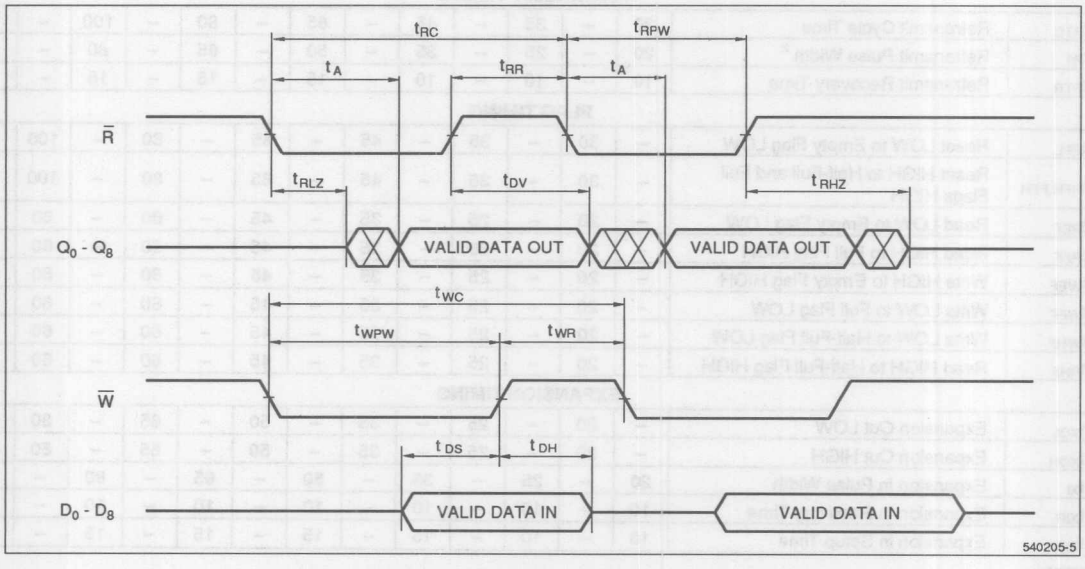


Figure 10. Asynchronous Write and Read Operation

TIMING DIAGRAMS (cont'd)

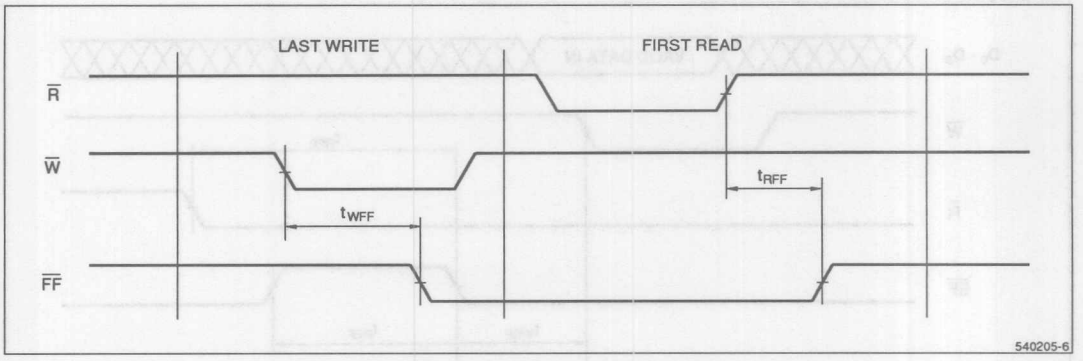


Figure 11. Full Flag From Last Write to First Read

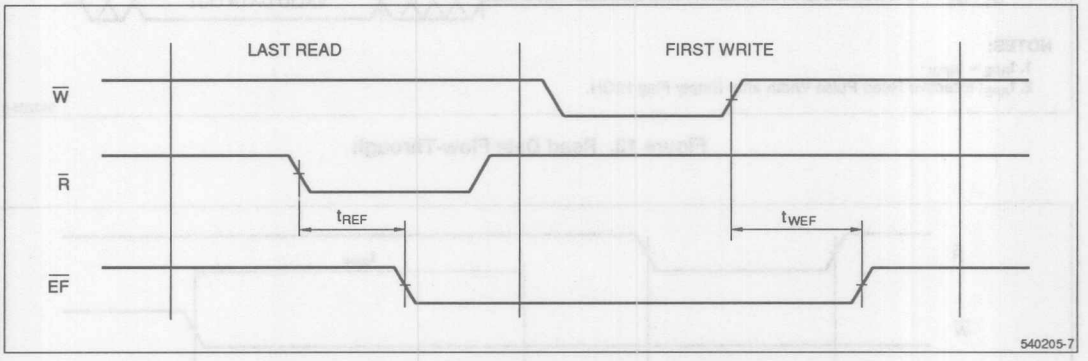
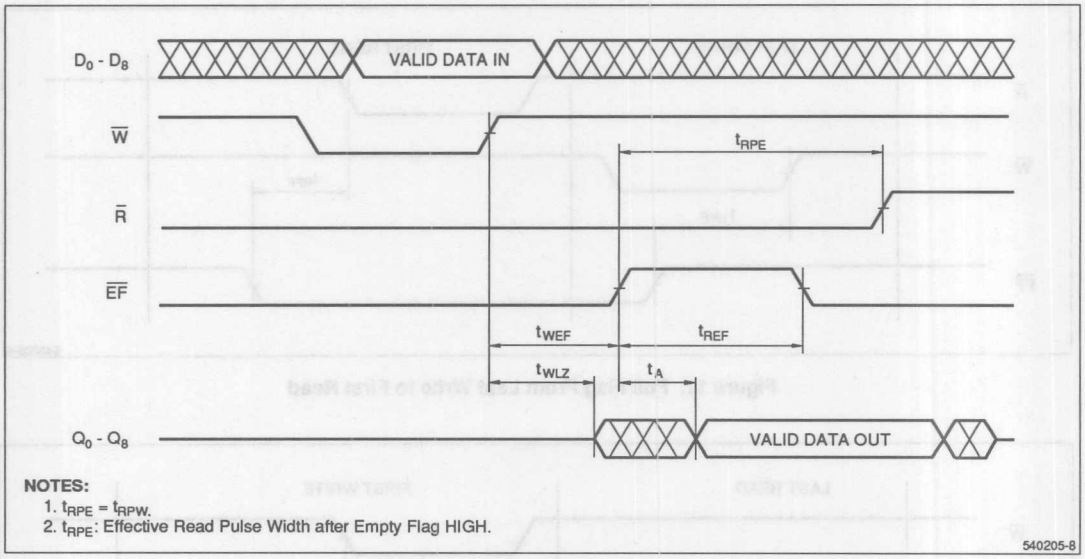


Figure 12. Empty Flag From Last Read to First Write

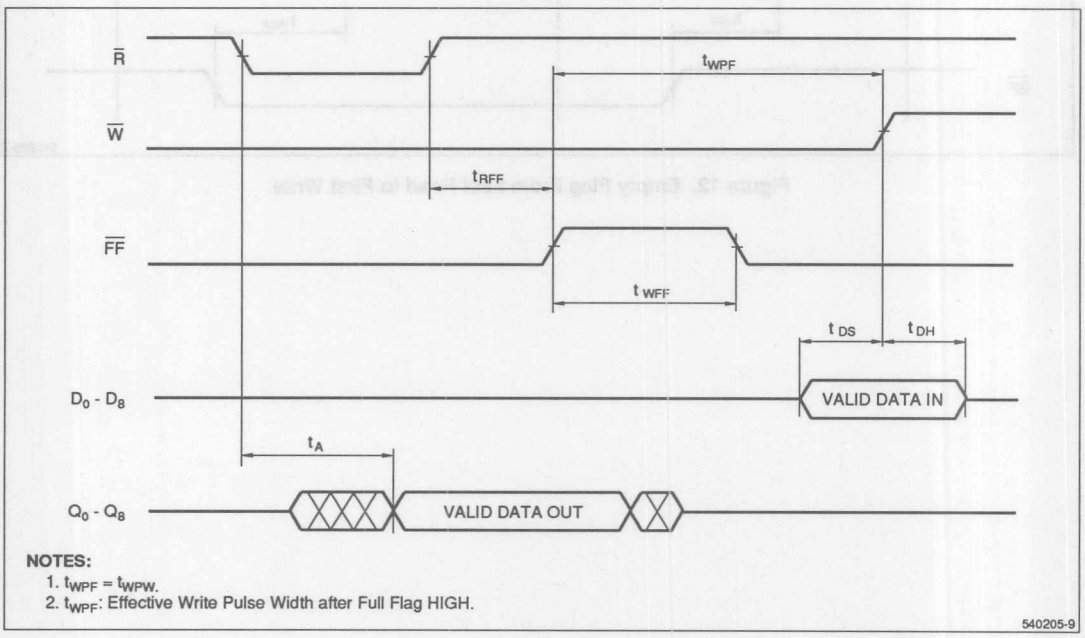
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540205-8

Figure 13. Read Data Flow-Through

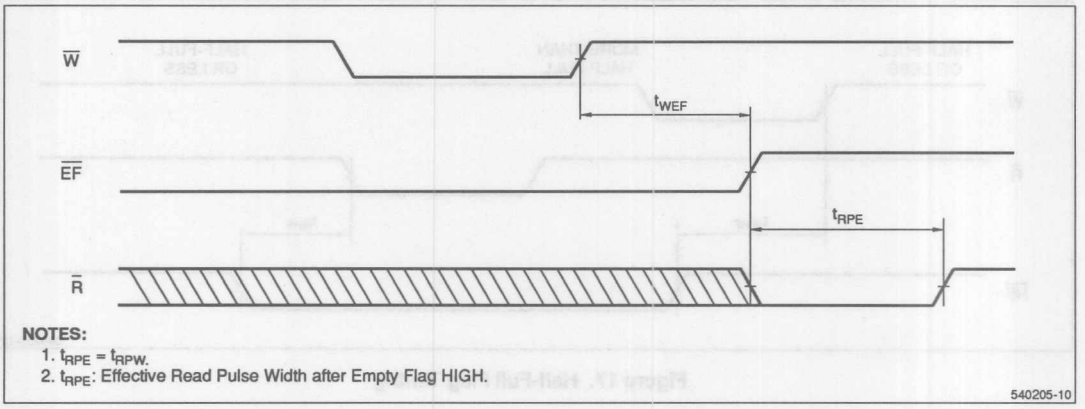


NOTES:
1. $t_{WPF} = t_{WPW}$.
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540205-9

Figure 14. Write Data Flow-Through

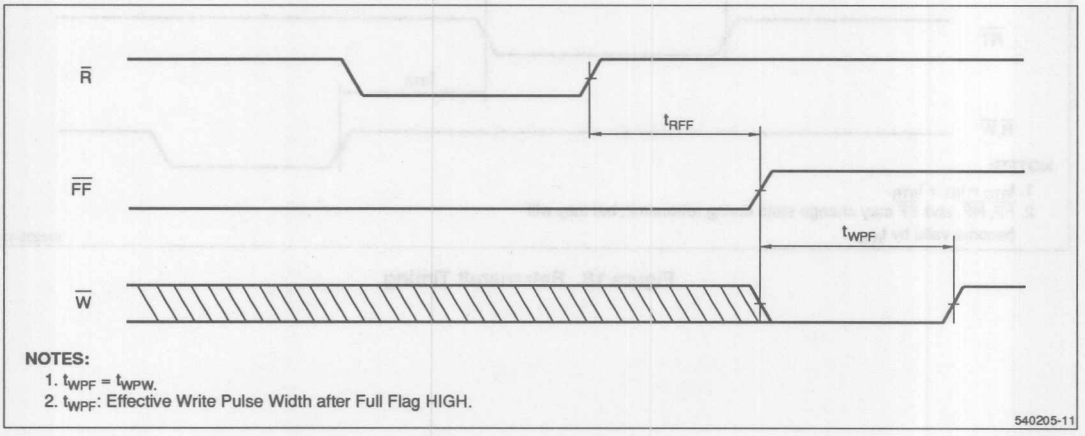
TIMING DIAGRAMS (cont'd)



NOTES:
1. $t_{RPE} = t_{RPW}$.
2. t_{RPE}: Effective Read Pulse Width after Empty Flag HIGH.

540205-10

Figure 15. Empty Flag Timing



NOTES:
1. $t_{WPF} = t_{WPW}$.
2. t_{WPF}: Effective Write Pulse Width after Full Flag HIGH.

540205-11

Figure 16. Full Flag Timing

TIMING DIAGRAMS (cont'd)

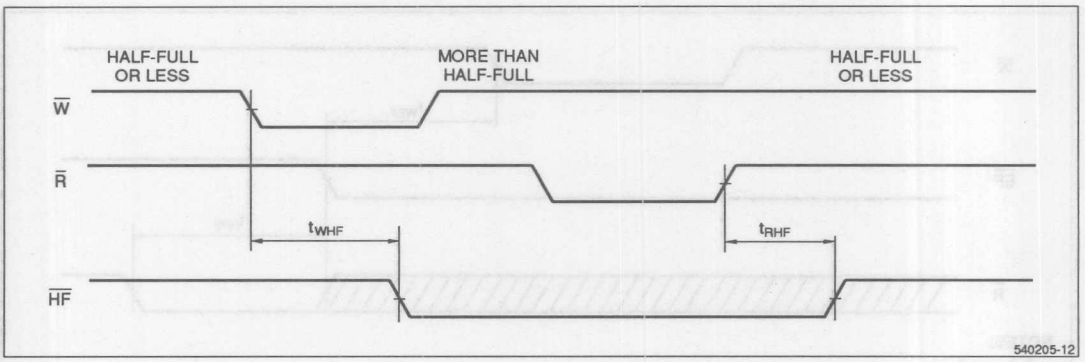


Figure 17. Half-Full Flag Timing

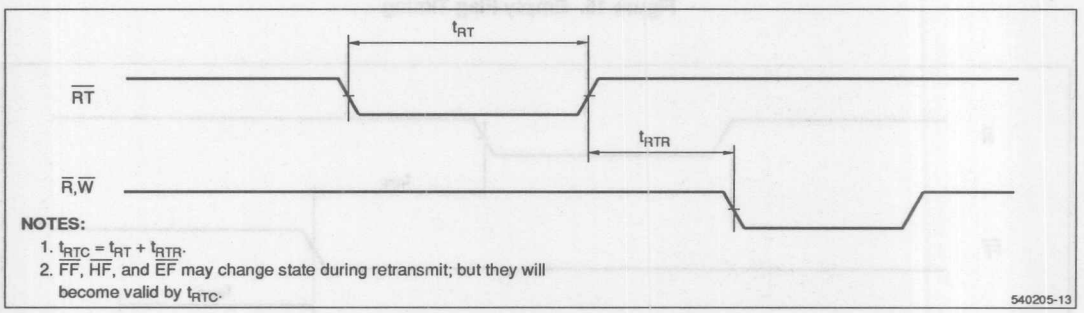


Figure 18. Retransmit Timing

TIMING DIAGRAMS (cont'd)

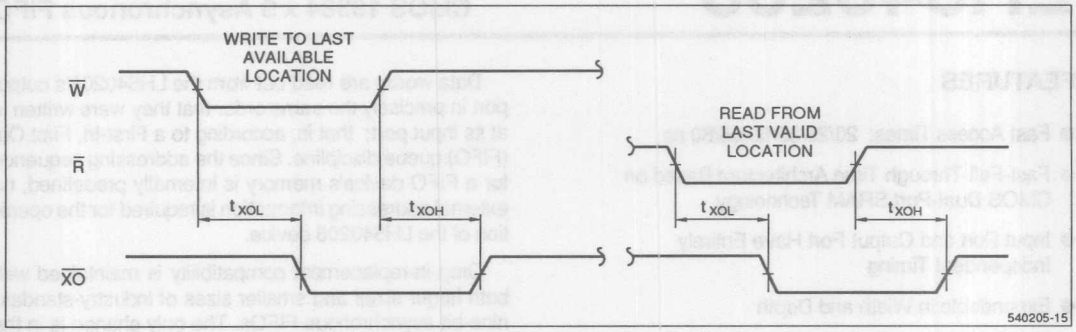


Figure 19. Expansion-Out Timing

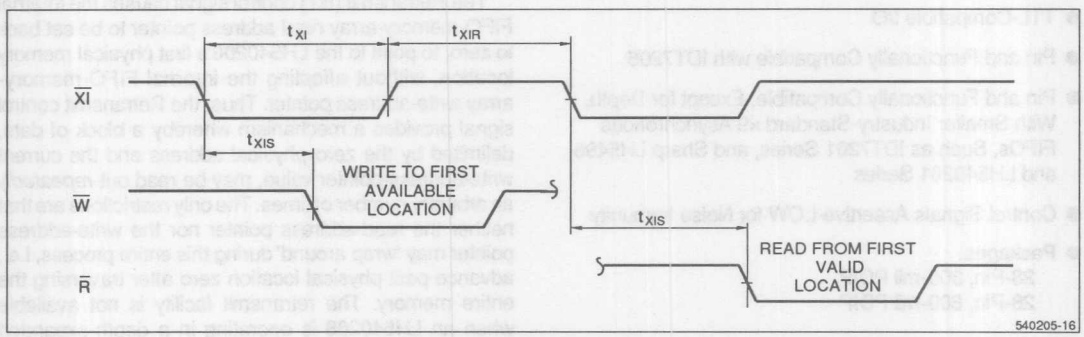
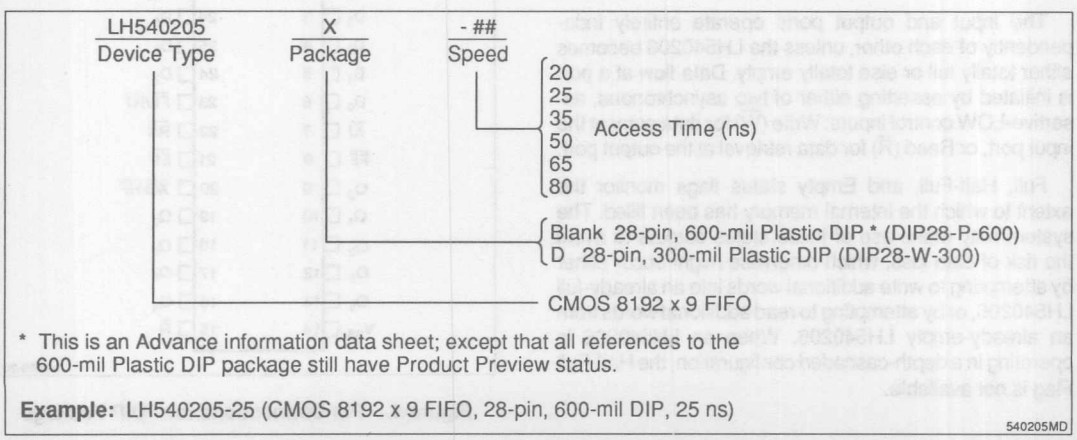


Figure 20. Expansion-In Timing

ORDERING INFORMATION



LH540206

PRODUCT PREVIEW

CMOS 16384 × 9 Asynchronous FIFO

FEATURES

- Fast Access Times: 20/25/35/50/65/80 ns
- Fast-Fall-Through Time Architecture Based on CMOS Dual-Port SRAM Technology
- Input Port and Output Port Have Entirely Independent Timing
- Expandable in Width and Depth
- Full, Half-Full, and Empty Status Flags
- Data Retransmission Capability
- TTL-Compatible I/O
- Pin and Functionally Compatible with IDT7206
- Pin and Functionally Compatible, Except for Depth, With Smaller Industry-Standard ×9 Asynchronous FIFOs, Such as IDT7201 Series, and Sharp LH5496 and LH540201 Series
- Control Signals Assertive-LOW for Noise Immunity
- Packages:
  28-Pin, 300-mil PDIP
  28-Pin, 600-mil PDIP

FUNCTIONAL DESCRIPTION

The LH540206 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS dual-port SRAM technology, capable of storing up to 16384 nine-bit words. It follows the industry-standard architecture and package pinouts for nine-bit asynchronous FIFOs. Each nine-bit LH540206 word may consist of a standard eight-bit byte, together with a parity bit or a block-marking/framing bit.

The input and output ports operate entirely independently of each other, unless the LH540206 becomes either totally full or else totally empty. Data flow at a port is initiated by asserting either of two asynchronous, assertive-LOW control inputs: Write ($\overline{W}$) for data entry at the input port, or Read ($\overline{R}$) for data retrieval at the output port.

Full, Half-Full, and Empty status flags monitor the extent to which the internal memory has been filled. The system may make use of these status outputs to avoid the risk of data loss, which otherwise might occur either by attempting to write additional words into an already-full LH540206, or by attempting to read additional words from an already-empty LH540206. When an LH540206 is operating in a depth-cascaded configuration, the Half-Full Flag is not available.

Data words are read out from the LH540206's output port in precisely the same order that they were written in at its input port; that is, according to a First-In, First Out (FIFO) queue discipline. Since the addressing sequence for a FIFO device's memory is internally predefined, no external addressing information is required for the operation of the LH540206 device.

Drop-in-replacement compatibility is maintained with both larger sizes and smaller sizes of industry-standard nine-bit asynchronous FIFOs. The only change is in the number of internally-stored data words implied by the states of the Full Flag and the Half-Full Flag.

The Retransmit ($\overline{RT}$) control signal causes the internal FIFO-memory-array read-address pointer to be set back to zero, to point to the LH540206's first physical memory location, without affecting the internal FIFO-memory-array write-address pointer. Thus, the Retransmit control signal provides a mechanism whereby a block of data, delimited by the zero physical address and the current write-address-pointer value, may be read out *repeatedly* an arbitrary number of times. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, i.e., advance past physical location zero after traversing the entire memory. The retransmit facility is not available when an LH540206 is operating in a depth-expanded configuration.

PIN CONNECTIONS

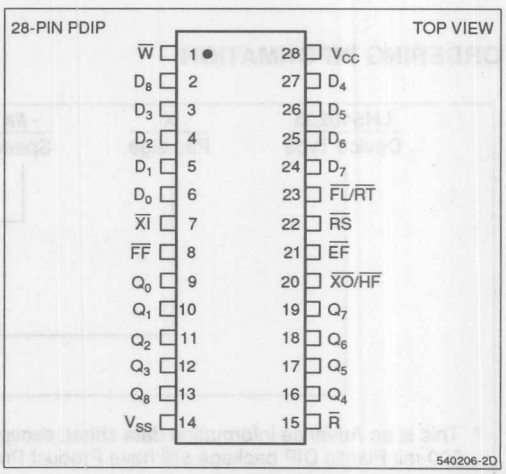


Figure 1. Pin Connections for PDIP Package

FUNCTIONAL DESCRIPTION (cont'd)

The Reset ($\overline{RS}$) control signal returns the LH540206 to an initial state, empty and ready to be filled. An LH540206 should be reset during every system power-up sequence. A reset operation causes the internal FIFO-memory-array write-address pointer, as well as the read-address pointer, to be set back to zero, to point to the LH540206's first physical memory location. Any information which previously had been stored within the LH540206 is not recoverable after a reset operation.

A cascading (depth-expansion) scheme may be implemented by using the Expansion In ($\overline{XI}$) input signal and the Expansion Out ($\overline{XO}/\overline{HF}$) output signal. This scheme allows a deeper 'effective FIFO' to be implemented by using two or more individual LH540206 devices, without incurring additional latency ('fallthrough' or 'bubblethrough') delays, and without the necessity of storing and retrieving any given data word more than once. In this cascaded operating mode, one LH540206 device must be designated as the 'first-load' or 'master' device, by grounding its First-Load ($\overline{FL}/\overline{RT}$) control input; the remaining LH540206 devices are designated as 'slaves,' by tying their $\overline{FL}/\overline{RT}$ inputs HIGH. Because of the need to share control signals on pins, the Half-Full Flag and the retransmission capability are not available for either 'master' or 'slave' LH540206 devices operating in cascaded mode.

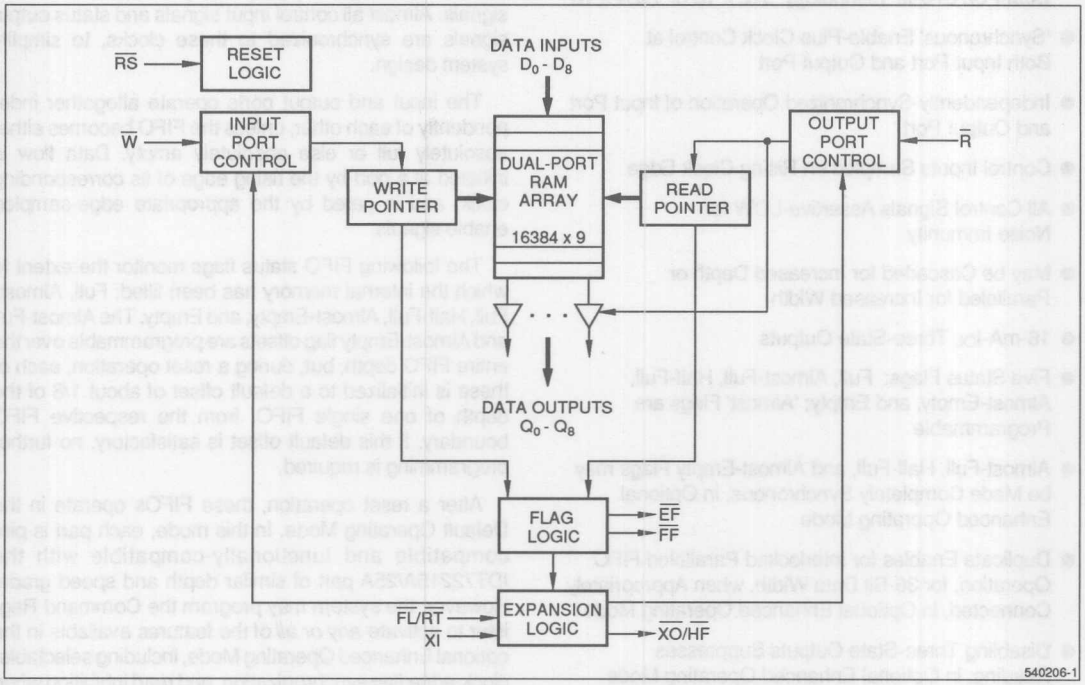


Figure 2. LH540206 Block Diagram

LH540215/25

PRELIMINARY

512 × 18 / 1024 × 18 Synchronous FIFO

FEATURES

- Fast Cycle Times: 15/20/25/50 ns
- Pin-Compatible Drop-In Replacements for IDT72215A/25A FIFOs; Default Operating Mode is Functionally IDT-Compatible
- Device Comes Up into Known Default State at Reset; Programming is Allowed, but is not Required
- Internal Memory Array Architecture Based on CMOS Dual-Port SRAM Technology, 512 × 18 or 1024 × 18
- 'Synchronous' Enable-Plus-Clock Control at Both Input Port and Output Port
- Independently-Synchronized Operation of Input Port and Output Port
- Control Inputs Sampled on Rising Clock Edge
- All Control Signals Assertive-LOW for Noise Immunity
- May be Cascaded for Increased Depth or Paralleled for Increased Width
- 16-mA-I_{OL} Three-State Outputs
- Five Status Flags: Full, Almost-Full, Half-Full, Almost-Empty, and Empty; 'Almost' Flags are Programmable
- Almost-Full, Half-Full, and Almost-Empty Flags may be Made Completely Synchronous, in Optional Enhanced Operating Mode
- Duplicate Enables for Interlocked Paralleled FIFO Operation, for 36-Bit Data Width, when Appropriately Connected, in Optional Enhanced Operating Mode
- Disabling Three-State Outputs Suppresses Reading, in Optional Enhanced Operating Mode
- Data Retransmit Function
- TTL/CMOS-Compatible I/O
- Space-Saving 68-Pin PLCC Package

FUNCTIONAL DESCRIPTION

The LH540215/25 are FIFO (First-In, First-Out) memory devices, based on fully-static CMOS dual-port SRAM technology, capable of containing up to 512 or 1024 18-bit words respectively. They can replace two or more byte-wide FIFOs in many applications, for microprocessor-to-microprocessor or microprocessor-to-bus communication. Their architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design.

The input and output ports operate altogether independently of each other, unless the FIFO becomes either absolutely full or else absolutely empty. Data flow is initiated at a port by the rising edge of its corresponding clock, and is gated by the appropriate edge-sampled enable signals.

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Almost-Full and Almost-Empty flag offsets are programmable over the entire FIFO depth; but, during a reset operation, each of these is initialized to a default offset of about 1/8 of the depth of one single FIFO, from the respective FIFO boundary. If this default offset is satisfactory, no further programming is required.

After a reset operation, these FIFOs operate in the Default Operating Mode. In this mode, each part is pin-compatible and functionally-compatible with the IDT72215A/25A part of similar depth and speed grade. However, the system may program the Command Register to activate *any or all* of the features available in the optional Enhanced Operating Mode, including selectable-clock-edge flag synchronization, and read inhibition when the data outputs are disabled. Interlocked-operation paralleling is also available, by appropriate interconnection of the FIFO's expansion inputs. Also, assertion of the $\overline{\text{EMODE}}$ control input leaves Command Register bits 06-10 set, which causes the FIFO to operate in the Enhanced Operating Mode.

The Retransmit control signal causes the internal FIFO read-address pointer to be set back to zero, without affecting the internal FIFO write-address pointer. Thus, the Retransmit control signal also provides a mechanism whereby a block of data delimited by the zero physical address and the current write-address pointer address may be read out *repeatedly*, an arbitrary number of times.

FUNCTIONAL DESCRIPTION (cont'd)

The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' during this entire process, and that the retransmit facility is not available when a FIFO is operating in IDT-compatible depth-cascaded mode.

Programming the programmable-flag offsets, the number of FIFOs to be cascaded in depth, the timing synchronization of the various status flags, and the optional read-suppression functionality of $\overline{OE}$ may be individually controlled by asserting the signal $\overline{LD}$, without any reset operation. When $\overline{LD}$ is asserted, while writing is enabled by asserting $\overline{WEN}$, some or all of the input bus word $D_0 - D_{17}$ is used at the next rising edge of WCLK to program one or more of the resource registers on successive write clocks. Likewise, the values programmed into these resource registers may be read out for verification by asserting $\overline{REN}$, with the outputs $Q_0 - Q_{17}$ enabled. Reading out these resource registers should not be initiated while they are being written into.

Coordinated operation of two 18-bit FIFOs as one 36-bit FIFO may be ensured by 'interlocked' crosscoupling of status-flag outputs from each port to expansion inputs of the other one; that is, $\overline{EF}$ to $\overline{WXI}/WEN_2$, and $\overline{FF}$ to $\overline{RXI}/REN_2$, in *both* directions between two paralleled FIFOs. This 'interlocked' operation takes effect automatically, if two paralleled FIFOs are crossconnected in this manner. (See Table 2.) IDT-compatible depth cascading is no longer available when operating in this mode; however, pipelined depth cascading remains possible.

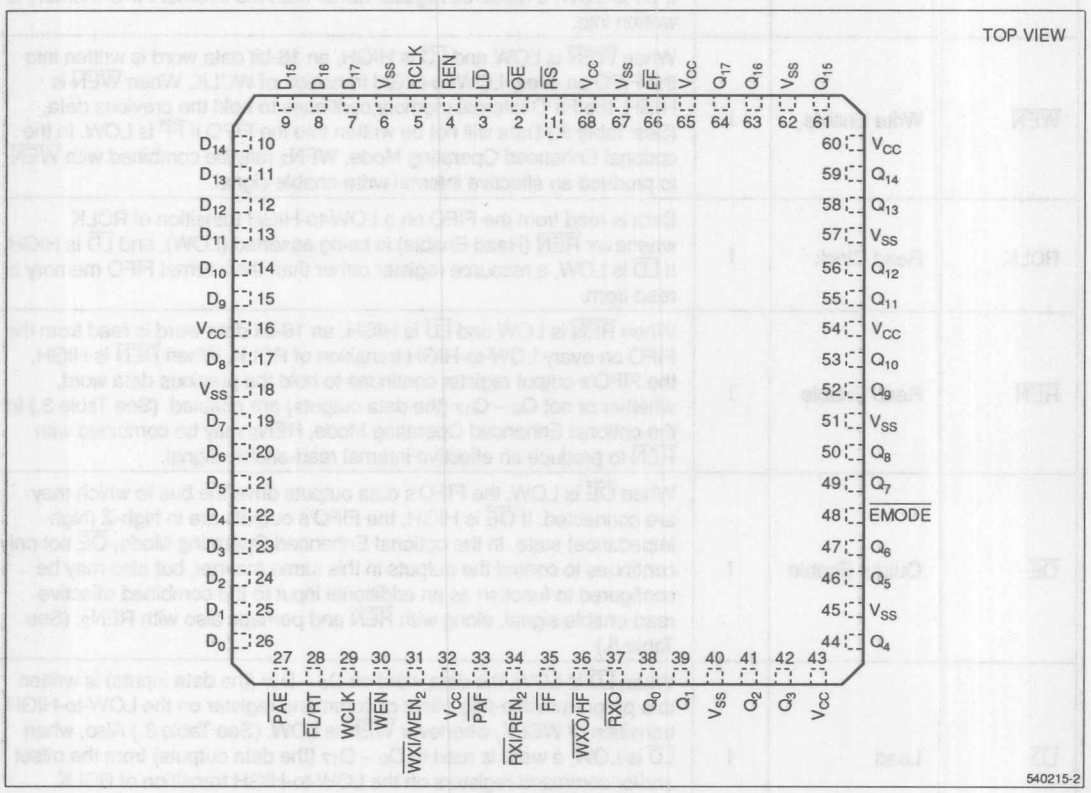


Figure 1. Pin Connections for PLCC Package

PIN DESCRIPTIONS

PIN	NAME	PIN TYPE *	DESCRIPTION
$D_0 - D_{17}$	Data Inputs	I	Data inputs from an 18-bit bus.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is taken LOW, the FIFO's internal read and write pointers are set to address the first physical location of the RAM array; $\overline{FF}$ and $\overline{PAF}$ go HIGH; and $\overline{PAE}$ and $\overline{EF}$ go LOW. The programmable-flag-offset registers and the Command Register are set to their default values. A reset is required before an initial write after power-up.
$\overline{EMODE}$	Enhanced Operating Mode	I	When $\overline{EMODE}$ is held LOW, Command Register bits 06-10 are forced HIGH rather than LOW, thus enabling all Enhanced Operating Mode features. (See Table 5.) If this behavior is always desired, $\overline{EMODE}$ may be grounded. Alternatively, $\overline{EMODE}$ may be tied to V_{CC}, so that the FIFO is functionally IDT-compatible.
WCLK	Write Clock	I	Data is written into the FIFO on a LOW-to-HIGH transition of WCLK, whenever $\overline{WEN}$ (Write Enable) is being asserted (LOW), and $\overline{LD}$ is HIGH. If $\overline{LD}$ is LOW, a resource register rather than the internal FIFO memory is written into.
$\overline{WEN}$	Write Enable	I	When $\overline{WEN}$ is LOW and $\overline{LD}$ is HIGH, an 18-bit data word is written into the FIFO on every LOW-to-HIGH transition of WCLK. When $\overline{WEN}$ is HIGH, the FIFO internal memory continues to hold the previous data. (See Table 3.) Data will not be written into the FIFO if $\overline{FF}$ is LOW. In the optional Enhanced Operating Mode, WEN_2 may be combined with $\overline{WEN}$ to produce an effective internal write-enable signal.
RCLK	Read Clock	I	Data is read from the FIFO on a LOW-to-HIGH transition of RCLK whenever $\overline{REN}$ (Read Enable) is being asserted (LOW), and $\overline{LD}$ is HIGH. If $\overline{LD}$ is LOW, a resource register rather than the internal FIFO memory is read from.
$\overline{REN}$	Read Enable	I	When $\overline{REN}$ is LOW and $\overline{LD}$ is HIGH, an 18-bit data word is read from the FIFO on every LOW-to-HIGH transition of RCLK. When $\overline{REN}$ is HIGH, the FIFO's output register continues to hold the previous data word, whether or not $Q_0 - Q_{17}$ (the data outputs) are enabled. (See Table 3.) In the optional Enhanced Operating Mode, REN_2 may be combined with $\overline{REN}$ to produce an effective internal read-enable signal.
$\overline{OE}$	Output Enable	I	When $\overline{OE}$ is LOW, the FIFO's data outputs drive the bus to which they are connected. If $\overline{OE}$ is HIGH, the FIFO's outputs are in high-Z (high-impedance) state. In the optional Enhanced Operating Mode, $\overline{OE}$ not only continues to control the outputs in this same manner, but also may be configured to function as an additional input to the combined effective read-enable signal, along with $\overline{REN}$ and perhaps also with REN_2. (See Table 5.)
$\overline{LD}$	Load	I	When $\overline{LD}$ is LOW, the data word on $D_0 - D_{17}$ (the data inputs) is written to a programmable-flag-offset or command register on the LOW-to-HIGH transition of WCLK, whenever $\overline{WEN}$ is LOW. (See Table 3.) Also, when $\overline{LD}$ is LOW, a word is read to $Q_0 - Q_{17}$ (the data outputs) from the offset and/or command registers on the LOW-to-HIGH transition of RCLK, whenever $\overline{REN}$ is LOW. (See again Table 3.) When $\overline{LD}$ is HIGH, normal FIFO write and read operations are enabled.

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

PIN DESCRIPTIONS (cont'd)

PIN	NAME	PIN TYPE *	DESCRIPTION
$\overline{FL}/RT$	First Load/ Retransmit	I	In the standalone or paralleled configuration, $\overline{FL}$ may be grounded. However, in the standalone or paralleled configuration, if $\overline{FL}$ is taken HIGH, it functions instead as RT (Retransmit), and resets the FIFO's internal read pointer to the first physical location of the RAM array. In the cascaded configuration, $\overline{FL}$ has an entirely different function; it is grounded for the first FIFO device (the 'master' device or 'first-load' device), and is set to HIGH for all other FIFO devices in the daisy chain.
$\overline{WXI}/WEN_2$	Write Expansion Input/ Write Enable 2	I	This signal is dual-purpose; its functionality is determined during a reset operation, according to its own state, and also according to the states of the two other control inputs $\overline{RXI}/REN_2$ and $\overline{FL}/RT$. (See Tables 2 and 6.) In the standalone or paralleled configuration, $\overline{WXI}/WEN_2$ is grounded. In the cascaded configuration, $\overline{WXI}/WEN_2$ is connected to $\overline{WXO}$ (Write Expansion Output) of the previous device, and functions as $\overline{WXI}$. In the optional Enhanced Operating Mode, $\overline{WXI}/WEN_2$ functions as a second write-enable signal, WEN_2, which is combined with $\overline{WEN}$ to produce an effective internal write-enable signal.
$\overline{RXI}/REN_2$	Read Expansion Input/ Read Enable 2	I	This signal is dual-purpose; its functionality is determined during a reset operation, according to its own state, and also according to the states of the two other control inputs $\overline{WXI}/WEN_2$ and $\overline{FL}/RT$. (See Tables 2 and 6.) In the standalone or paralleled configuration, $\overline{RXI}/REN_2$ is grounded. In the cascaded configuration, $\overline{RXI}/REN_2$ is connected to $\overline{RXO}$ (Read Expansion Output) of the previous device, and functions as $\overline{RXI}$. In the optional Enhanced Operating Mode, $\overline{RXI}/REN_2$ functions as a second read-enable signal, REN_2, which is combined with $\overline{REN}$ – and perhaps also with $\overline{OE}$, if Command-Register bit 10 is set – to produce an effective internal read-enable signal.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ is LOW, the FIFO is full; further advancement of its internal write-address pointer, and further data writes into its inputs, are inhibited. When $\overline{FF}$ is HIGH, the FIFO is not full. $\overline{FF}$ is synchronized to WCLK. $\overline{FF}$ is functionally equivalent to an assertive-HIGH 'Input Ready' control input signal.
$\overline{PAF}$	Programmable Almost-Full Flag	O	When $\overline{PAF}$ is LOW, the FIFO is 'almost full,' based on the almost-full offset programmed into the FIFO. The default value of this offset at reset is about 1/8 of the FIFO capacity, measured from 'full.' (See Table 4.) In Default Mode, $\overline{PAF}$ is asynchronous; in the optional Enhanced Operating Mode, $\overline{PAF}$ is synchronized to WCLK. (See Table 5.)
$\overline{WXO}/\overline{HF}$	Write Expansion Output/ Half-Full Flag	O	This signal is dual-purpose; its functionality is determined during a reset operation according to the states of the two control inputs $\overline{WXI}/WEN_2$ and $\overline{RXI}/REN_2$. (See Tables 2 and 6.) In the standalone or paralleled configuration, whenever $\overline{HF}$ is LOW the device is more than half full. In Default Mode, $\overline{HF}$ is asynchronous; in the optional Enhanced Operating Mode, $\overline{HF}$ may be synchronized either to WCLK or to RCLK. (See Table 5.) In the cascaded configuration, a pulse is sent from $\overline{WXO}$ to $\overline{WXI}$ of the next device whenever the last location in the FIFO is written.
$\overline{PAE}$	Programmable Almost-Empty Flag	O	When PAE is LOW, the FIFO is 'almost empty,' based on the almost-empty offset programmed into the FIFO. The default value of this offset at reset is about 1/8 of the FIFO capacity, measured from 'empty.' (See Table 4.) In Default Mode, $\overline{PAE}$ is asynchronous; in the optional Enhanced Operating Mode, $\overline{PAE}$ is synchronized to RCLK. (See Table 5.)

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

PIN DESCRIPTIONS (cont'd)

PIN	NAME	PIN TYPE *	DESCRIPTION
$\overline{EF}$	Empty Flag	O	When EF is LOW, the FIFO is empty; further advancement of its internal read-address pointer, and further changes in the data word present at its outputs, are inhibited. When $\overline{EF}$ is HIGH, the FIFO is not empty. $\overline{EF}$ is synchronized to RCLK. $\overline{EF}$ is functionally equivalent to an assertive-HIGH 'Output Ready' input control signal.
$\overline{RXO}$	Read Expansion Output	O	In the IDT-compatible cascaded configuration, a pulse is sent from $\overline{RXO}$ to $\overline{RXI}$ of the next FIFO whenever the last location in the FIFO is read.
$Q_0 - Q_{17}$	Data Outputs	O/Z	Data outputs to drive an 18-bit bus.
V_{CC}	Power	V	Seven +5 V power-supply pins.
V_{SS}	Ground	V	Eight 0 V ground pins.

* I = Input, O = Output, Z = High-Impedance, V = Power Voltage Level

Table 1. Depth-Code Programming

DEPTH CODE d	TOTAL DEPTH	
	WITH LH540215s	WITH LH540225s
0	512	1024
1	512	1024
2	1024	2048
3	1536	3072
...	...	...
d	512d	1024d
...	...	...
31	15872	31744
32	16384	32768

Table 2. Grouping-Mode Determination During a Reset Operation

$\overline{EMODE}$	$\overline{WXI}/WEN_2$	$\overline{RXI}/REN_2$	$\overline{FL}/RT$	MODE	$\overline{WXO}/\overline{HF}$ USAGE	$\overline{WXI}/WEN_2$ USAGE	$\overline{RXI}/REN_2$ USAGE	$\overline{FL}/RT$ USAGE
H	H	H	H	Cascaded Slave [1]	$\overline{WXO}$	$\overline{WXI}$	$\overline{RXI}$	$\overline{FL}$
H	H	H	L	Cascaded Master [1]	$\overline{WXO}$	$\overline{WXI}$	$\overline{RXI}$	$\overline{FL}$
H	H	L	X	(Reserved)	($\overline{HF}$)	($\overline{WXI}$)	($\overline{RXI}$)	(RT)
H	L	H	X	(Reserved)	($\overline{WXO}$)	($\overline{WXI}$)	($\overline{RXI}$)	($\overline{FL}$)
H	L	L	H	(Reserved)	($\overline{HF}$)	(none)	(none)	(RT)
H	L	L	L [2]	Standalone	$\overline{HF}$	(none)	(none)	RT
H	L	L	H	(Reserved)	($\overline{HF}$)	(none)	(none)	(RT)
L	X	X	L [2]	terlocked Paralleled	$\overline{HF}$	WEN_2	REN_2	RT

NOTES:

1. The terms 'master' and 'slave' refer to IDT-compatible cascading. In pipelined cascading, there is no such distinction.
2. Once grouping mode has been determined, $\overline{FL}$/RT is allowed to go HIGH to control retransmission.
3. H = HIGH; L = LOW; X = Don't Care.

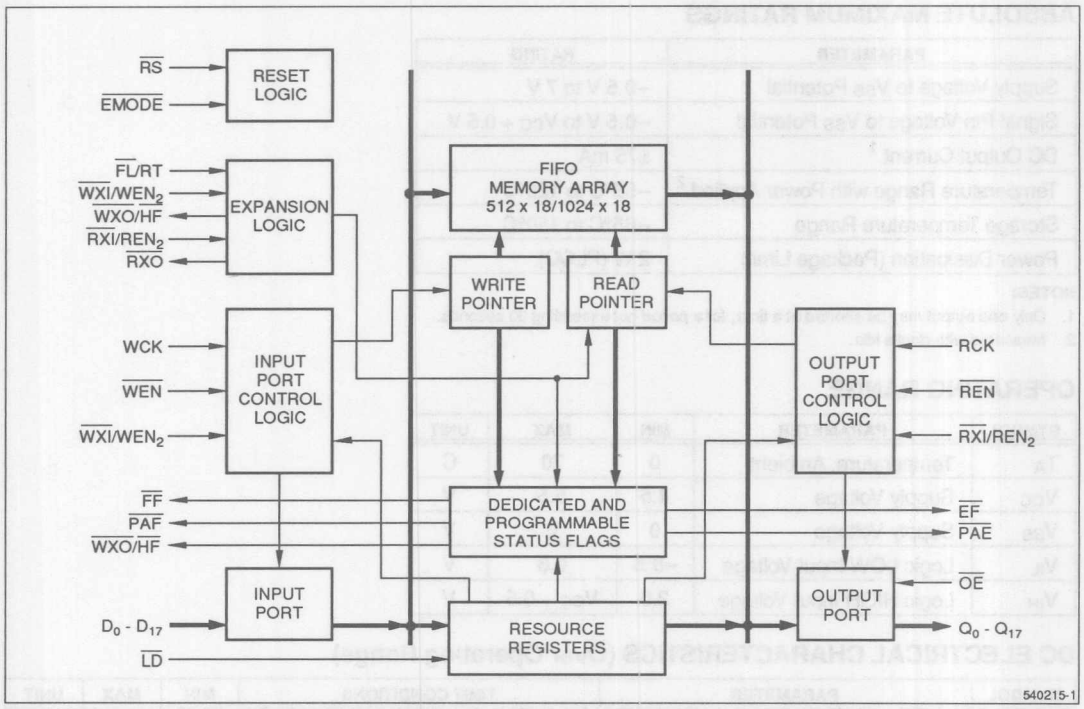


Figure 2. LH540215/25 Block Diagram

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING
Supply Voltage to V_{SS} Potential	−0.5 V to 7 V
Signal Pin Voltage to V_{SS} Potential	−0.5 V to V_{CC} + 0.5 V
DC Output Current [1]	±75 mA
Temperature Range with Power Applied [2]	−55°C to 125°C
Storage Temperature Range	−65°C to 150°C
Power Dissipation (Package Limit)	2 W (PLCC)

NOTES:
1. Only one output may be shorted at a time, for a period not exceeding 30 seconds.
2. Measured with clocks idle.

OPERATING RANGE

SYMBOL	PARAMETER	MIN	MAX	UNIT
T_A	Temperature, Ambient	0	70	C
V_{CC}	Supply Voltage	4.5	5.5	V
V_{SS}	Supply Voltage	0	0	V
V_{IL}	Logic LOW Input Voltage	−0.5	0.8	V
V_{IH}	Logic HIGH Input Voltage	2.0	V_{CC} + 0.5	V

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
I_{LI}	Input Leakage	V_{CC} = 5.5 V, V_{IN} = 0 V to V_{CC}	−1	1	µA
I_{LO}	I/O Leakage	$\overline{OE} \geq V_{IH}$, 0 V ≤ $V_{OUT} \leq V_{CC}$	−2	2	µA
V_{OH}	Output HIGH Voltage	I_{OH} = −8.0 mA	2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 16.0 mA		0.4	V
I_{CC}	Average Operating Supply Current	Measured at fc = max		250	mA
I_{CC2}	Average Standby Supply Current	All inputs = V_{IHMIN} (clock idle)		60	mA
I_{CC3}	Power-Down Supply Current	All inputs = V_{CC} − 0.2 V (clock idle)		1	mA

AC TEST CONDITIONS

PARAMETER		RATING
Input Pulse Levels		V_{SS} to 3 V
Input Rise and Fall Times (10% to 90%)		3 ns
Output Reference Levels		1.5 V
Input Timing Reference Levels		1.5 V
Output Load, Timing Tests	R_1 (Top Resistor)	1.1k Ohms
	R_2 (Bottom Resistor)	680 Ohms
	C_L (Load Capacitance)	30 pF

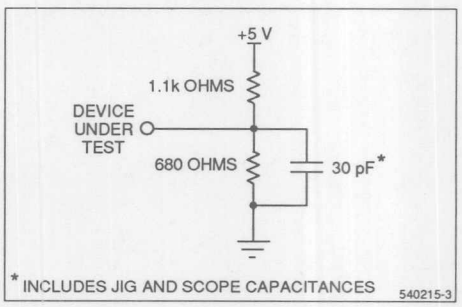


Figure 3. Output Load Circuit

CAPACITANCE

PARAMETER	RATING
C_{IN} (Input Capacitance) V_{IN} = 0 V	7 pF
C_O (Output Capacitance) V_{OUT} = 0 V	7 pF

AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	-15		-20		-25		-50	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
f_S	Clock Cycle Frequency		67		50		40		20
t_A	Data Access Time	2	11	2	14	3	15	3	25
t_{CLK}	Clock Cycle Time	15		20		25		50	
t_{CLKH}	Clock HIGH Time	6		8		10		20	
t_{CLKL}	Clock LOW Time	7		9		10		20	
t_{DS}	Data Setup Time	4		5		6		10	
t_{DH}	Data Hold Time	1		1		1		2	
t_{ENS}	Enable Setup Time	4		5		6		10	
t_{ENH}	Enable Hold Time	1		1		1		2	
t_{RS}	Reset Pulse Width [1]	15		20		25		50	
t_{RSS}	Reset Setup Time [2]	9		12		15		30	
t_{RSF}	Reset to Flag and Output Time		15		20		25		50
t_{OLZ}	Output Enable to Output in Low-Z [2]	0		0		0		0	
t_{OE}	Output Enable to Output Valid		7		9		12		20
t_{OHZ}	Output Enable to Output in High-Z [2]	1	7	1	9	1	12	1	20
t_{WFF}	Write Clock to Full Flag		11		14		16		30
t_{REF}	Read Clock to Empty Flag		11		12		15		30
t_{PAF}	Clock to Programmable Almost-Full Flag (Default Mode)		15		20		22		35
t_{PAE}	Clock to Programmable Almost-Empty Flag (Default Mode)		15		20		22		35
t_{HF}	Clock to Half-Full Flag (Default Mode)		15		20		22		35
t_{PAFS}	Clock to Programmable Almost-Full Flag (Enhanced Mode)		11		12		15		30
t_{PAES}	Clock to Programmable Almost-Empty Flag (Enhanced Mode)		11		12		15		30
t_{HFS}	Clock to Half-Full Flag (Enhanced Mode)		11		12		15		30
t_{XO}	Clock to Expansion-Out		9		12		15		30
t_{XI}	Expansion-In Pulse Width	6		8		10		20	
t_{XIS}	Expansion-In Setup Time	6		8		10		20	
t_{SKEW1}	Skew Time Between Read Clock and Write Clock for Full Flag	11		14		16		20	
t_{SKEW2}	Skew Time Between Read Clock and Write Clock for Empty Flag	11		14		16		20	

NOTES:

1. Pulse widths less than the stated minimum values may cause incorrect operation.
2. Values are guaranteed by design; not currently tested.

Table 3. Selection of Read and Write Operations

$\overline{LD}$	$\overline{WEN}$	$\overline{REN}$	WCLK	RCLK	ACTION
L	X	X	–	–	No operation.
L	L	H	∧	–	Write to a resource register. [1]
L	H	H	∧	–	Increment resource-register write counter, but do not write. [2]
L	H	L	–	∧	Read from a resource register. [1]
L	H	H	–	∧	Increment resource-register read counter, but do not read. [2]
L	X	X	∧	∧	Illegal combination, which will cause errors.
H	L	X	∧	X	Normal FIFO write operation.
H	X	L	X	∧	Normal FIFO read operation.
H	L	X	–	X	No write operation.
H	H	X	X	X	No write operation.
H	X	L	X	–	No read operation.
H	X	H	X	X	No read operation.
H	L	L	–	–	No operation.
H	H	H	X	X	No operation.

KEY:

H = Logic 'HIGH'; L = Logic 'LOW'; X = 'Don't-care' (logic 'HIGH,' logic 'LOW,' or any transition);

∧ = A 'LOW'-to-'HIGH' transition; – = Any condition EXCEPT a 'LOW'-to-'HIGH' transition.

NOTES:

1. The selection of a resource register to be written or read is controlled by two simple state machines. One state machine controls the selection for writing; the other state machine controls the selection for reading. These two state machines operate independently of each other. Both state machines are reset to point to Word 0 by a reset operation.
2. The order of the three resource registers, as selected by either state machine, is always:
   Word 0: Almost-Empty Offset Register
   Word 1: Almost-Full Offset Register
   Word 2: Command Register
   Word 0: Almost-Empty Offset Register
   ...
   (repeats indefinitely)
   ...

Table 4. Status Flags

NUMBER OF UNREAD DATA WORDS PRESENT WITHIN FIFO [1, 2]		$\overline{FF}$	$\overline{PAF}$	$\overline{HF}$	$\overline{PAE}$	$\overline{EF}$
512 × 18 FIFO	1024 × 18 FIFO					
0	0	H	H	H	L	L
1 to q	1 to q	H	H	H	L	H
(q + 1) to 256	(q + 1) to 512	H	H	H	H	H
257 to (512 – (p + 1))	513 to (1024 – (p + 1))	H	H	L	H	H
(512 – p) to 511	(1024 – p) to 1023	H	L	L	H	H
512	1024	L	L	L	H	H

NOTES:

1. q = Programmable-Almost-Empty Offset. (Default values: 512 × 18, q = 63; 1024 × 18, q = 127.)
2. p = Programmable-Almost-Full Offset. (Default values: 512 × 18, p = 63; 1024 × 18, p = 127.)

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES

Data Inputs

DATA IN ($D_0 - D_{17}$)

Data, programmable-flag-offset values, and Command-Register codes are input to the FIFO as 18-bit words on $D_0 - D_{17}$. Unused bit positions in offset and Command-Register words should be zero-filled.

Control Inputs

RESET ($\overline{RS}$)

The FIFO is reset whenever the asynchronous Reset ($\overline{RS}$) input is taken to a LOW state. A reset operation is required after power-up, before the first write operation may occur. The state of the FIFO is fully defined after a reset operation. If the default values which are entered into the Programmable-Flag-Offset-Value Registers and the Command Register by a reset operation are acceptable, then no device programming is required. A reset operation initializes the FIFO's internal read-address and write-address pointers to the FIFO's first physical memory location. The five status flags, $\overline{FF}$, $\overline{PAF}$, $\overline{HF}$, $\overline{PAE}$, and $\overline{EF}$, are updated to indicate that the FIFO is completely empty; thus, the first three of these are reset to HIGH, and the last two are reset to LOW. The flag-offset values for $\overline{PAF}$ and $\overline{PAE}$ each are initialized to about 1/8 of the depth of a single FIFO; 63 for a 512-word FIFO, and 127 for a 1024-word FIFO. If $\overline{EMODE}$ is not being asserted (i.e., if $\overline{EMODE}$ is HIGH), the Command Register is initialized to configure the FIFO to operate in the 100% IDT72215A/25A-compatible Default Operating Mode. The Depth Code is initialized to LLLLLH (01_{10}). Until a write operation occurs, the data outputs $D_0 - D_{17}$ all are LOW whenever $\overline{OE}$ is LOW.

ENHANCED OPERATING MODE ($\overline{EMODE}$)

Whenever $\overline{EMODE}$ is being asserted, Command Register bits 06-10 remain HIGH rather than LOW after the completion of the reset operation. Thus, $\overline{EMODE}$ has the effect of activating optional Enhanced Operating Mode features, without the need to configure the Command Register by the normal programming method. The behavior of these optional features is described in Table 5. For permanent Enhanced Operating Mode operation, $\overline{EMODE}$ must be grounded.

Asserting $\overline{EMODE}$ also causes $\overline{WXI}/WEN_2$ to be configured as WEN_2, and $\overline{RXI}/REN_2$ to be configured as REN_2.

WRITE CLOCK (WCLK)

A rising edge (LOW-to-HIGH transition) of WCLK initiates a FIFO write cycle if $\overline{LD}$ is HIGH, or a resource-register write cycle if $\overline{LD}$ is LOW. The 18 data inputs, and all input-side synchronous control inputs, must meet setup and hold times with respect to the rising edge of WCLK. The input-side status flags are meaningful after specified time intervals, following a rising edge of WCLK.

Conceptually, WCLK receives a free-running, periodic 'clock' waveform, used to control other signals which are edge-sensitive. However, there actually is not any absolute requirement that the WCLK waveform *must* be periodic. An 'asynchronous' mode of operation is in fact possible, if $\overline{WEN}$ is continuously asserted (that is, is continuously held LOW), and WCLK receives aperiodic 'clock' pulses of suitable duration. There likewise is no requirement that WCLK must have any particular relation to the read clock RCLK. These two clock inputs may in fact receive the same 'clock' signal; or they may receive totally-different signals, which are not synchronized to each other in any way.

WRITE ENABLE ($\overline{WEN}$)

Whenever $\overline{WEN}$ is being asserted (is LOW) and $\overline{LD}$ is HIGH, and the FIFO is not full, an 18-bit data word is loaded into the input register for the memory array at every WCLK rising edge (LOW-to-HIGH transition). Data words are stored into the two-port memory array sequentially, regardless of any ongoing read operation. Whenever $\overline{WEN}$ is not being asserted (is HIGH), the input register retains whatever data word it contained previously, and no new data word gets loaded into the memory array.

To prevent overrunning the internal FIFO boundaries, further write operations are inhibited whenever the Full Flag ($\overline{FF}$) is being asserted (is LOW). If a valid read operation then occurs, upon the completion of that read cycle $\overline{FF}$ again goes HIGH after a time t_{WFF}, and another write operation is allowed to begin whenever WCLK makes another LOW-to-HIGH transition. Effectively, $\overline{WEN}$ is overridden by $\overline{FF}$; thus, $\overline{WEN}$ has no effect when the FIFO is full.

In the optional Enhanced Operating Mode, if $\overline{EMODE}$ is being asserted (is LOW), $\overline{WXI}/WEN_2$ functions as WEN_2, an additional duplicate (albeit assertive-HIGH) write-enable input, in order to provide an 'interlocking' mechanism for reliable synchronization of two paralleled FIFOs. To control writing, WEN_2 is combined with $\overline{WEN}$; the logic-AND function of $\overline{WEN}$ and WEN_2 then behaves like $\overline{WEN}$ in the foregoing description.

READ CLOCK (RCLK)

A rising edge (LOW-to-HIGH transition) of RCLK initiates a FIFO read cycle if $\overline{LD}$ is HIGH, or a resource-register read cycle if $\overline{LD}$ is LOW. All output-side synchronous control inputs must meet setup and hold times with respect to the rising edge of RCLK. The 18 data outputs, and the output-side status flags, are meaningful after specified time intervals, following a rising edge of RCLK.

Conceptually, RCLK receives a free-running, periodic 'clock' waveform, used to control other signals which are

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

edge-sensitive. However, there actually is not any absolute requirement that the RCLK waveform *must* be periodic. An 'asynchronous' mode of operation is in fact possible, if $\overline{REN}$ is continuously asserted (that is, is continuously held LOW), and RCLK receives aperiodic 'clock' pulses of suitable duration. There likewise is no requirement that RCLK must have any particular relation to the write clock WCLK. These two clock inputs may in fact receive the same 'clock' signal; or they may receive totally-different signals, which are not synchronized to each other in any way.

READ ENABLE ($\overline{REN}$)

Whenever $\overline{REN}$ is being asserted (is LOW), and the FIFO is not full, an 18-bit data word is loaded into the output register from the memory array at every RCLK rising edge (LOW-to-HIGH transition). Data words are read from the two-port memory array sequentially, regardless of any ongoing write operation. Whenever $\overline{REN}$ is not being asserted (is HIGH), the output register retains whatever data word it contained previously, and no new data word gets loaded into it from the memory array.

To prevent underrunning the internal FIFO boundaries, further read operations are inhibited whenever the Empty Flag ($\overline{EF}$) is being asserted (is LOW). If a valid write operation then occurs, upon the completion of that write cycle $\overline{EF}$ again goes HIGH after a time t_{REF}, and another read operation is allowed to begin whenever RCLK makes another LOW-to-HIGH transition. Effectively, $\overline{REN}$ is overridden by $\overline{EF}$; thus, $\overline{REN}$ has no effect when the FIFO is empty.

In the optional Enhanced Operating Mode, one or two additional read enable inputs may be combined with $\overline{REN}$ to control reading; the logic-AND function of these two or three inputs then behaves like $\overline{REN}$ in the foregoing description. If $\overline{EMODE}$ is being asserted (is LOW), $\overline{RXI}/REN_2$ functions as REN_2, an additional duplicate (albeit assertive-HIGH) $\overline{REN}$ input, in order to provide an 'interlocking' mechanism for reliable synchronization of two paralleled FIFOs. Also, if Command Register bit 10 has been set, $\overline{OE}$ takes on the extra role of serving as yet another duplicate $\overline{REN}$ input, *in addition to* its usual function of controlling the FIFO's data outputs, in order to inhibit further read operations whenever the FIFO's data outputs are disabled.

OUTPUT ENABLE ($\overline{OE}$)

$\overline{OE}$ is an assertive-LOW, asynchronous, output enable. In the Default Operating Mode, $\overline{OE}$ has only the effect of enabling or disabling the data outputs $Q_0 - Q_{17}$. That is, disabling $Q_0 - Q_{17}$ does not inhibit a read operation, for data being transmitted to the output register; the same data will remain available later, when the outputs are again enabled, unless subsequently overwritten. When $Q_0 - Q_{17}$ are enabled, each of these 18 data outputs is in a normal HIGH or LOW state, according to the bit pattern of the data word in the output register. When $Q_0 - Q_{17}$ are disabled, each of these outputs is in the high-Z (high-impedance) state.

In the optional Enhanced Operating Mode, if Command Register bit 10 has been set, $\overline{OE}$ behaves as an additional read enable, as well as enabling and disabling the data outputs $Q_0 - Q_{17}$. Under these circumstances, incrementing the read-address pointer is inhibited whenever $Q_0 - Q_{17}$ are in the high-Z state. Thus, 'reading' successive words which fail to reach the outputs is prevented, as a safeguard against data loss.

LOAD ($\overline{LD}$)

The Sharp LH540215/25 FIFOs contain three 18-bit resource registers. The contents of these three registers may be loaded with data from the data inputs $D_0 - D_{17}$, or read out on the data outputs $Q_0 - Q_{17}$. The first two registers are the Programmable-Flag-Offset-Value Registers, for the Programmable Almost-Empty Flag ($\overline{PAE}$) and the Programmable Almost-Full Flag ($\overline{PAF}$) respectively. The third register is the Command Register, which includes the 6-bit IDT72215A/25A 'Depth Code' field d, along with several configuration-control bits for Sharp's optional Enhanced-Operating-Mode features.

None of these three registers makes use of all of its available 18 bits. Figure 4 shows which bit positions of each register are operational. The two Programmable-Flag-Offset-Value Registers each contain the offset value in bits 0-15; bits 16-17 are unused. The Command Register configuration is shown in Table 5. For the Command Register, the default value for any operational bit which has not been programmed is zero (LOW); except, that the default value of the Depth Code is LLLLLH (01_{10}), in conformity with IDT's usage. The default values for both offsets are about 1/8 of the total number of words in the FIFO: 63 for a 512 × 18 FIFO, and 127 for a 1024 × 18 FIFO.

Whenever $\overline{LD}$ and $\overline{WEN}$ are simultaneously being asserted (are both LOW), the 18-bit data word from the data inputs $D_0 - D_{17}$ is written into the Programmable-Empty-Flag-Offset-Value Register at the first rising edge (LOW-to-HIGH transition) of the write clock (WCLK). (See Table 3.) If $\overline{LD}$ and $\overline{WEN}$ continue to be simultaneously asserted, another 18-bit data word from the data inputs $D_0 - D_{17}$ is written into the Programmable-Full-Flag-Offset-Value Register at the second rising edge of WCLK, and still another 18-bit data word from the data inputs $D_0 - D_{17}$ is written into the Command Register at the third rising edge of WCLK. At the fourth rising edge of WCLK, writing again occurs to the Programmable-Empty-Flag-Offset-Value Register; and the writing sequence gets repeated on subsequent WCLK rising edges.

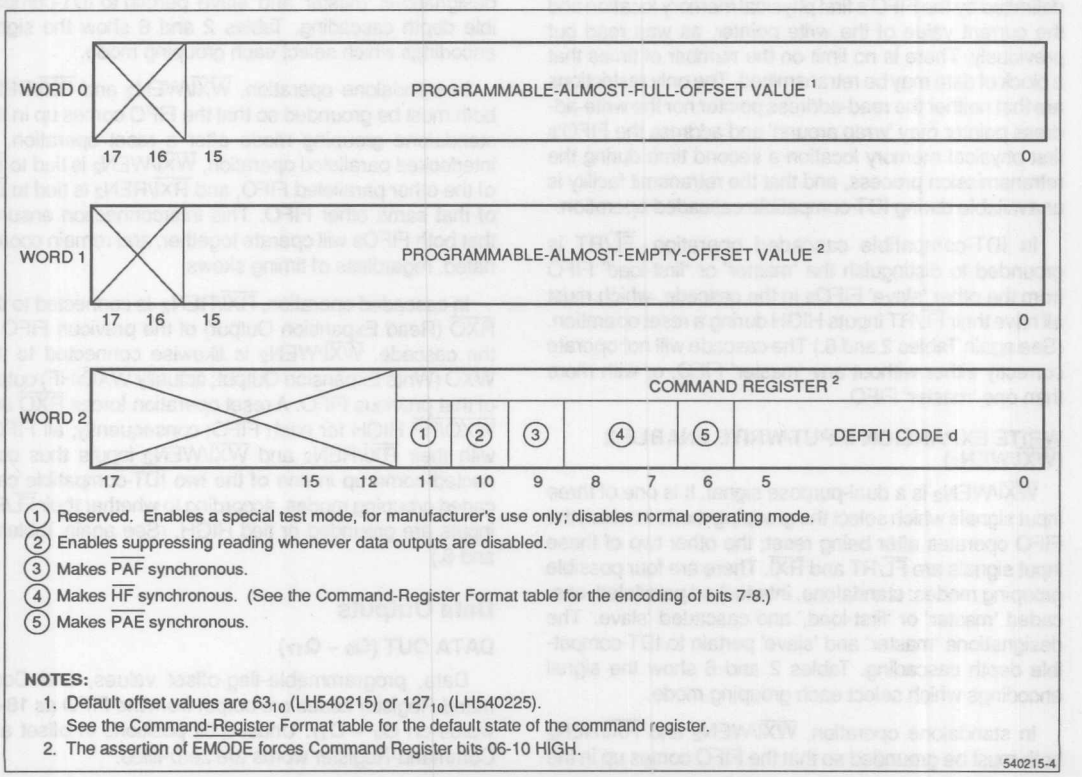
DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

The lower 9 bits of these data words are made use of by the 512-word LH540215, and the lower 10 bits by the 1024-word LH540225. 10 bits are used for the Command Register, by both the LH540215 and the LH540225. There is no restriction on the values which may occur in these data fields; however, unused bit positions should be encoded LOW in order to maintain forward compatibility.

Writing contents to these three resource registers does not have to occur all at one time, or to be effected by one single sequence of steps. Whenever $\overline{LD}$ is being asserted (is LOW) but $\overline{WEN}$ is not being asserted (is HIGH), the FIFO's internal resource-register-write-address pointer advances at each rising edge of WCLK, without any writing actually taking place. (See Table 3.) Thus, for instance, one or two resource registers may be written, after which the FIFO may be returned to normal FIFO-array-read/write operation by deasserting $\overline{LD}$ (to HIGH).

Likewise, whenever $\overline{LD}$ and $\overline{REN}$ are simultaneously being asserted (are both LOW) the 18-bit data word from the Programmable-Empty-Flag-Offset-Value Register is read to the data outputs $Q_0 - Q_{17}$ at the first rising edge (LOW-to-HIGH transition) of the read clock (RCLK). (See Table 3.) If $\overline{LD}$ and $\overline{REN}$ continue to be simultaneously asserted, another 18-bit data word from the Programmable-Full-Flag-Offset-Value Register is read to the data outputs $Q_0 - Q_{17}$ at the second rising edge of RCLK, and still another 18-bit data word from the Command Register is read to the data outputs $Q_0 - Q_{17}$ at the third rising edge of RCLK. At the fourth rising edge of RCLK, reading again occurs from the Programmable-Empty-Flag-Offset-Value Register; and the reading sequence gets repeated on subsequent RCLK rising edges.

Reading contents from these three resource registers does not have to occur all at one time, or to be effected by one single sequence of steps. Whenever $\overline{LD}$ is being asserted (is LOW) but $\overline{REN}$ is not being asserted (is HIGH), the FIFO's internal resource-register-read-address pointer advances at each rising edge of RCLK, without any reading actually taking place. (See Table 3.) Thus, for instance, one or two resource registers may be read, after which the FIFO may be returned to normal FIFO-array-read/write operation by deasserting $\overline{LD}$ (to HIGH).



(1) Reserved. Enables a special test mode, for manufacturer's use only; disables normal operating mode.
(2) Enables suppressing reading whenever data outputs are disabled.
(3) Makes $\overline{PAF}$ synchronous.
(4) Makes $\overline{HF}$ synchronous. (See the Command-Register Format table for the encoding of bits 7-8.)
(5) Makes $\overline{PAE}$ synchronous.

NOTES:
1. Default offset values are 63_{10} (LH540215) or 127_{10} (LH540225).
   See the Command-Register Format table for the default state of the command register.
2. The assertion of EMODE forces Command Register bits 06-10 HIGH.

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Figure 4. Resource Registers

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

To ensure correct operation, rising edges of WCLK and RCLK should not both be occuring at the same time while $\overline{LD}$ is being asserted.

FIRST LOAD/RETRANSMIT ($\overline{FL}$/RT)

$\overline{FL}$/RT is a dual-purpose signal. It is one of three input signals which select the grouping mode in which the FIFO operates after being reset; the other two of these input signals are $\overline{WXI}$/WEN_2 and $\overline{RXI}$/REN_2. There are four possible grouping modes: standalone, interlocked paralleled, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 2 and 6 show the signal encodings which select each grouping mode.

In standalone or paralleled operation, the $\overline{FL}$/RT pin should be grounded for strict IDT72215A/25A-compatible operation. However, if it is taken HIGH, the FIFO's internal read-address pointer is reset to address the FIFO's first physical memory location, without any other reset actions being taken; in particular, the FIFO's internal write-address pointer is unaffected. Subsequent read operations may then again read out the same block of data, delimited by the FIFO's first physical memory location and the current value of the write pointer, as was read out previously. There is no limit on the number of times that a block of data may be retransmitted. The only restrictions are that neither the read-address pointer nor the write-address pointer may 'wrap around' and address the FIFO's first physical memory location a second time during the retransmission process, and that the retransmit facility is unavailable during IDT-compatible cascaded operation.

In IDT-compatible cascaded operation, $\overline{FL}$/RT is grounded to distinguish the 'master' or 'first-load' FIFO from the other 'slave' FIFOs in the cascade, which must all have their $\overline{FL}$/RT inputs HIGH during a reset operation. (See again Tables 2 and 6.) The cascade will not operate correctly either without any 'master' FIFO, or with more than one 'master' FIFO.

WRITE EXPANSION INPUT/WRITE ENABLE 2 ($\overline{WXI}$/WEN_2)

$\overline{WXI}$/WEN_2 is a dual-purpose signal. It is one of three input signals which select the grouping mode in which the FIFO operates after being reset; the other two of these input signals are $\overline{FL}$/RT and $\overline{RXI}$. There are four possible grouping modes: standalone, interlocked paralleled, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 2 and 6 show the signal encodings which select each grouping mode.

In standalone operation, $\overline{WXI}$/WEN_2 and $\overline{RXI}$/REN_2 both must be grounded so that the FIFO comes up in the standalone grouping mode after a reset operation. In interlocked paralleled operation, $\overline{WXI}$/WEN_2 is tied to $\overline{FF}$ of the other paralleled FIFO, and $\overline{RXI}$/REN_2 is tied to $\overline{EF}$ of that same other FIFO. This interconnection ensures that both FIFOs will operate together, and remain coordinated, regardless of timing skews.

In cascaded operation, $\overline{WXI}$/WEN_2 is connected to the $\overline{WXO}$ (Write Expansion Output; actually $\overline{WXO}$/$\overline{HF}$) output of the previous FIFO in the cascade. $\overline{RXI}$/REN_2 is likewise connected to the $\overline{RXO}$ (Read Expansion Output) output of that previous FIFO. A reset operation forces $\overline{WXO}$/$\overline{HF}$ and $\overline{RXO}$ HIGH for each FIFO; consequently, all FIFOs with their $\overline{WXI}$/WEN_2 and $\overline{RXI}$/REN_2 inputs thus connected come up in one of the two cascaded grouping modes, according to whether their $\overline{FL}$/RT inputs are grounded or tied HIGH. (See again Tables 2 and 6.)

READ EXPANSION INPUT/READ ENABLE 2 ($\overline{RXI}$/REN_2)

$\overline{RXI}$/REN_2 is a dual-purpose signal. It is one of three input signals which select the grouping mode in which the FIFO operates after being reset; the other two of these input signals are $\overline{FL}$/RT and $\overline{WXI}$. There are four possible grouping modes: standalone, interlocked paralleled, cascaded 'master' or 'first-load,' and cascaded 'slave.' The designations 'master' and 'slave' pertain to IDT-compatible depth cascading. Tables 2 and 6 show the signal encodings which select each grouping mode.

In standalone operation, $\overline{WXI}$/WEN_2 and $\overline{RXI}$/REN_2 both must be grounded so that the FIFO comes up in the standalone grouping mode after a reset operation. In interlocked paralleled operation, $\overline{WXI}$/WEN_2 is tied to $\overline{FF}$ of the other paralleled FIFO, and $\overline{RXI}$/REN_2 is tied to $\overline{EF}$ of that same other FIFO. This interconnection ensures that both FIFOs will operate together, and remain coordinated, regardless of timing skews.

In cascaded operation, $\overline{RXI}$/REN_2 is connected to the $\overline{RXO}$ (Read Expansion Output) of the previous FIFO in the cascade. $\overline{WXI}$/WEN_2 is likewise connected to the $\overline{WXO}$ (Write Expansion Output; actually $\overline{WXO}$/$\overline{HF}$) output of that previous FIFO. A reset operation forces $\overline{RXO}$ and $\overline{WXO}$/$\overline{HF}$ HIGH for each FIFO; consequently, all FIFOs with their $\overline{RXI}$/REN_2 and $\overline{WXI}$/WEN_2 inputs thus connected come up in one of the two IDT-compatible cascaded grouping modes, according to whether their $\overline{FL}$/RT inputs are grounded or tied HIGH. (See again Tables 2 and 6.)

Data Outputs

DATA OUT ($Q_0 - Q_{17}$)

Data, programmable-flag-offset values, and Command-Register codes are output from the FIFO as 18-bit words on $Q_0 - Q_{17}$. Unused bit positions in offset and Command-Register words are zero-filled.

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

Table 5. Command-Register Format

COMMAND REGISTER BITS	CODE	VALUE AFTER RESET	FLAG AFFECTED, IF ANY	DESCRIPTION	NOTES
00-05	XXXXXX	LLLLLH	–	Depth code d, from 00_{10} to 32_{10}.	Same functionality as in IDT72215A/25A.
06	L	L/H [2]	$\overline{PAE}$	Set by ↑RCLK, reset by ↑WCLK.	Asynchronous flag clocking.
	H			Set and reset by ↑RCLK.	Synchronous flag clocking.
07-08	LL	LL/HH [2]	$\overline{HF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
	LH			Set and reset by ↑RCLK.	Synchronous flag clocking at output port.
	HL			Set and reset by ↑WCLK.	Synchronous flag clocking at input port.
	HH				
09	L	L/H [2]	$\overline{PAF}$	Set by ↑WCLK, reset by ↑RCLK.	Asynchronous flag clocking.
	H			Set and reset by ↑WCLK.	Synchronous flag clocking.
10	L	L/H [2]	–	$\overline{OE}$ has no effect on a read operation.	Allows the read-address pointer to advance even when $Q_0 - Q_{17}$ are not driving the output bus.
	H			$\overline{OE}$ inhibits a read operation whenever the data outputs $Q_0 - Q_{17}$ are in the high-Z state.	Inhibits the read-address pointer from advancing when $Q_0 - Q_{17}$ are not driving the output bus; thus, guards against data loss.
11	L	L	–	Normal operating mode.	For all in-system applications.
	H			Special test mode.	Reserved for testing purposes.

NOTES:

1. When Command Register bits 06-11 are LOW, the FIFO behaves in a manner functionally equivalent to the IDT72215A/25A FIFO of similar depth and speed grade.
2. If $\overline{EMODE}$ is not asserted (is HIGH), Command Register bits 06-10 remain LOW. However, if $\overline{EMODE}$ is asserted (is LOW), Command Register bits 06-10 are forced HIGH, and remain HIGH until changed. Command Register bits 00-05 and 11 are unaffected by $\overline{EMODE}$.

Table 6. Expansion-Pin Usage According to Grouping Mode

I/O	PIN	STANDALONE	INTERLOCKED PARALLELED	MASTER	SLAVE
I	$\overline{WXI}$/WEN_2	Grounded	From $\overline{FF}$ (other FIFO)	From $\overline{WXO}$ (n-1st FIFO)	From $\overline{WXO}$ (n-1st FIFO)
O	$\overline{WXO}$/$\overline{HF}$	Becomes $\overline{HF}$	Becomes $\overline{HF}$	To $\overline{WXI}$ (n+1st FIFO)	To $\overline{WXI}$ (n+1st FIFO)
I	$\overline{RXI}$/REN_2	Grounded	From $\overline{EF}$ (other FIFO)	From $\overline{RXO}$ (n-1st FIFO)	From $\overline{RXO}$ (n-1st FIFO)
O	$\overline{RXO}$	Unused	Unused	To $\overline{RXI}$ (n+1st FIFO)	To $\overline{RXI}$ (n+1st FIFO)
I	$\overline{FL}$/RT	Becomes RT	Becomes RT	Grounded (Logic LOW)	Logic HIGH

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

Control/Status Outputs

FULL FLAG ($\overline{FF}$)

$\overline{FF}$ goes LOW whenever the FIFO is completely full; that is, whenever the FIFO's internal write pointer has completely caught up with its internal read pointer, so that if another word were to be written it would have to overwrite the unread word now in position for reading out by the next requested read operation. Under these conditions, the FIFO is filled to its nominal capacity, which is 512 18-bit words for the LH540215 or 1024 18-bit words for the LH540225 respectively. Write operations are inhibited whenever $\overline{FF}$ is LOW, regardless of the assertion or deassertion of Write Enable ($\overline{WEN}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), $\overline{FF}$ initially is HIGH. But, whenever no read operations have been performed since the completion of the reset operation, $\overline{FF}$ goes LOW after 512 write operations for the LH540215, or after 1024 write operations for the LH540225. (See Table 4.)

$\overline{FF}$ gets updated after a LOW-to-HIGH transition of the Write Clock (WCLK).

PROGRAMMABLE ALMOST-FULL FLAG ($\overline{PAF}$)

$\overline{PAF}$ goes LOW whenever the FIFO is 'almost' full; that is, whenever subtracting the value of the FIFO's internal read pointer from the value of its internal write pointer yields a difference which is less than the value of the Programmable-Almost-Full-Flag Offset 'p.' The subtraction is performed using modular arithmetic, modulo the total nominal number of 18-bit words in the FIFO's physical memory, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

The default value of 'p' after the completion of a reset operation is about 1/8 of this total nominal number of words: 63 for the LH540215 or 127 for the LH540225 respectively. However, 'p' may be set to any value which does not exceed this total nominal number of words, as explained in the description of Load ($\overline{LD}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no read operations have been performed since the completion of the reset operation, $\overline{PAF}$ goes LOW after (512-p) write operations for the LH540215, or after (1024-p) write operations for the LH540225. (See Table 4.)

If p is still at its default value, $\overline{PAF}$ is LOW whenever the FIFO is from 7/8 full to completely full.

In the IDT-compatible Default Operating Mode, $\overline{PAF}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Write Clock WCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Read Clock RCLK. Thus, in this operating mode, $\overline{PAF}$ behaves as an 'asynchronous flag.'

In the optional Enhanced Operating Mode, on the other hand, $\overline{PAF}$ gets updated only after a LOW-to-HIGH transition of the Write Clock WCLK, and thus behaves as a 'synchronous flag.' (See Table 5.) This behavior may be selected by setting Command Register bit 09.

WRITE EXPANSION OUT/HALF-FULL FLAG ($\overline{WXO}/\overline{HF}$)

$\overline{WXO}/\overline{HF}$ is a dual-purpose signal. In 'standalone' operation, it behaves as a Half-Full Flag ($\overline{HF}$), in accordance with Table 4. In IDT-compatible 'cascaded' operation, it behaves as a Write Expansion Output ($\overline{WXO}$) signal to coordinate writing operations with the next FIFO in the cascade. Under these same conditions, also, the dual-purpose $\overline{WXI}/WEN_2$ and $\overline{RXI}/REN_2$ inputs behave as Write Expansion Input ($\overline{WXI}$) and Read Expansion Input ($\overline{RXI}$) signals respectively.

When two or more LH540215 or LH540225 FIFOs are 'cascaded' to operate as a larger 'effective FIFO,' in an IDT-style 'daisy-chain' ring configuration, the Write Expansion Input ($\overline{WXI}$) of each FIFO is connected to $\overline{WXO}$ of the previous FIFO in the ring, with $\overline{WXI}$ of the 'first-load' or 'master' FIFO being connected to $\overline{WXO}$ of the last FIFO so as to complete the ring. Similar connections are made for each FIFO in the ring, parallel to these $\overline{WXO}$-to-$\overline{WXI}$ connections, for Read Expansion Input ($\overline{RXI}$) and Read Expansion Output ($\overline{RXO}$).

When the last physical location has been written in a FIFO operating in cascaded mode, a LOW-going pulse is emitted by that FIFO on its $\overline{WXO}$ output; otherwise, $\overline{WXO}$ remains constantly HIGH whenever the FIFO is operating in cascaded mode. This LOW-going $\overline{WXO}$ pulse serves as a 'token' in the 'token-passing' FIFO-cascading scheme; it is passed on to the next FIFO in the ring via its $\overline{WXI}$ input. When this next FIFO receives the token, it is activated for writing.

The foregoing description applies both to the 'first-load' or 'master' FIFO in the ring, and to any and all 'slave' FIFOs in the ring. However, $\overline{WXO}$ has no necessary function for FIFOs operating in the 'standalone' mode. Consequently, in that mode, the same output pin is used for $\overline{HF}$; it follows that $\overline{HF}$ is not available as an output from any FIFO which is operating in the IDT-compatible cascaded mode. A FIFO is initialized into 'cascaded master' mode, into 'cascaded slave' mode, into interlocked paralleled mode, or into standalone mode according to the

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

state of its $\overline{WXI}/WEN_2$, $\overline{RXI}/REN_2$, and $\overline{FL}/RT$ control inputs during a reset operation, and of $\overline{EMODE}$. (See Table 2, Table 5, and Table 6.)

In standalone or interlocked paralleled operation, $\overline{HF}$ goes LOW whenever the FIFO is more than half full; that is, whenever subtracting the value of the FIFO's internal read pointer from the value of its internal write pointer yields a difference which is less than half of the total nominal number of 18-bit words in the FIFO's physical memory, which is 256 for the LH540215 or 512 for the LH540225 respectively. (See Table 4.) The subtraction is performed using modular arithmetic, modulo this total nominal number of words, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and it is operating in standalone or interlocked paralleled mode, and no read operations have been performed since the completion of the reset operation, $\overline{HF}$ goes LOW after 257 write operations for the LH540215, or after 513 write operations for the LH540225. (See again Table 4.)

In the IDT-compatible Default Operating Mode, $\overline{HF}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Write Clock WCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Read Clock RCLK. Thus, in this operating mode, $\overline{HF}$ behaves as an 'asynchronous flag.'

In the optional Enhanced Operating Mode, on the other hand, $\overline{HF}$ gets updated only after a LOW-to-HIGH transition of the Read Clock RCLK, or else after a LOW-to-HIGH transition of the Write Clock WCLK, according to the setting of bits 07 and 08 of the Command Register. (See Table 5.) Thus, in this mode $\overline{HF}$ behaves as a 'synchronous flag,' and may be synchronized *either* to the input side of the FIFO (i.e., to WCLK), or to the output side of the FIFO (i.e., to RCLK).

PROGRAMMABLE ALMOST-EMPTY FLAG ($\overline{PAE}$)

$\overline{PAE}$ goes LOW whenever the FIFO is 'almost empty'; that is, whenever subtracting the value of the FIFO's internal write pointer from the value of its internal read pointer yields a difference which is less than q + 1, where 'q' is the value of the Programmable-Almost-Empty-Flag Offset. The subtraction is performed using modular arithmetic, modulo the total nominal number of 18-bit words in the FIFO's physical memory, which is 512 for the LH540215 or 1024 for the LH540225 respectively.

The default value of q after the completion of a reset operation is about 1/8 of this total nominal number of words, 63 for the LH540215 or 127 for the LH540225 respectively. However, q may be set to any value which does not exceed this total nominal number of words, as explained in the description of Load ($\overline{LD}$).

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no write operations have been performed since the completion of the reset operation, then $\overline{PAE}$ is LOW. (See Table 4.)

If q is still at its default value, $\overline{PAE}$ is LOW whenever the FIFO is from 1/8 full to completely empty.

In the IDT-compatible Default Operating Mode, $\overline{PAE}$ changes from HIGH to LOW only after a LOW-to-HIGH transition of the Read Clock RCLK, and from LOW to HIGH only after a LOW-to-HIGH transition of the Write Clock WCLK. Thus, in this operating mode, $\overline{PAE}$ behaves as an 'asynchronous flag.'

In the optional Enhanced Operating Mode, on the other hand, $\overline{PAE}$ gets updated only after a LOW-to-HIGH transition of the Read Clock RCLK, and thus behaves as a 'synchronous flag.' (See Table 5.) This behavior may be selected by setting Command Register bit 06.

EMPTY FLAG ($\overline{EF}$)

$\overline{EF}$ goes LOW whenever the FIFO is completely empty; that is, whenever the FIFO's internal read pointer has completely caught up with its internal write pointer, so that if another word were to be read out it would have to come from the physical memory location now in position to be written into by the next requested write operation. Read operations are inhibited whenever $\overline{EF}$ is LOW, regardless of the assertion or deassertion of $\overline{REN}$.

If the FIFO has been reset by asserting $\overline{RS}$ (LOW), and no write operations have been performed since the completion of the reset operation, then $\overline{EF}$ is LOW. (See Table 4.)

$\overline{EF}$ gets updated after a LOW-to-HIGH transition of the Read Clock RCLK.

READ EXPANSION OUT ($\overline{RXO}$)

When two or more LH540215 or LH540225 FIFOs are operating in IDT-compatible 'cascaded' mode as a larger 'effective FIFO,' the dual-purpose $\overline{RXI}/REN_2$ and $\overline{WXI}/WEN_2$ inputs behave as Read Expansion Input ($\overline{RXI}$) and Write Expansion Input ($\overline{WXI}$) signals respectively. An IDT-style cascade of these FIFO devices has a 'daisy-chain' ring configuration; the Read Expansion Input ($\overline{RXI}$) of each FIFO is connected to $\overline{RXO}$ of the previous FIFO in the ring, with $\overline{RXI}$ of the 'first-load' or 'master' FIFO being connected to $\overline{RXO}$ of the last FIFO so as to complete the ring. Similar connections are made for each FIFO in the ring, parallel to these $\overline{RXO}$-to-$\overline{RXI}$ connections, for Write Expansion Input ($\overline{WXI}$) and Write Expansion Output ($\overline{WXO}$).

DESCRIPTION OF SIGNALS AND OPERATING SEQUENCES (cont'd)

When the last physical location has been read in a FIFO operating in IDT-style cascaded mode, a LOW-going pulse is emitted by that FIFO on its $\overline{RXO}$ output; otherwise, $\overline{RXO}$ remains constantly HIGH. This LOW-going $\overline{RXO}$ pulse serves as a 'token' in the token-passing FIFO-cascading scheme; it is passed on to the next FIFO in the ring via its $\overline{RXI}$ input. When this next FIFO receives the token, it is activated for reading.

After a FIFO emits an $\overline{RXO}$ pulse, its data outputs go into high-Z state, regardless of the assertion or deassertion of its Output Enable ($\overline{OE}$) control input, until it again receives the token.

The foregoing description applies both to the 'first-load' or 'master' FIFO in the ring, and to any and all 'slave' FIFOs in the ring. However, $\overline{RXO}$ has no necessary function for a FIFO which is operating in 'standalone' mode. Consequently, in that mode, $\overline{RXO}$ is never asserted, and remains constantly HIGH. A FIFO is initialized into 'standalone' mode, into 'cascaded master' mode, or into 'cascaded slave' mode according to the state of its $\overline{WXI}/WEN_2$, $\overline{RXI}/REN_2$, and $\overline{FL}/RT$ control inputs during a reset operation. It also may be forced into interlocked paralleled mode by $\overline{EMODE}$. (See Table 2, Table 5, and Table 6.)

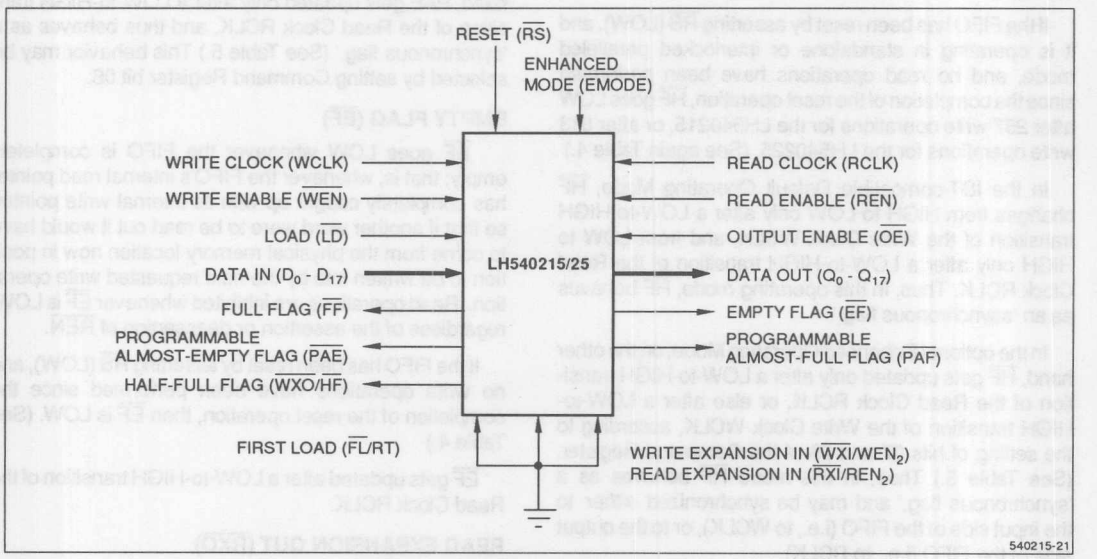


Figure 5. Standalone FIFO (512 × 18/1024 × 18)

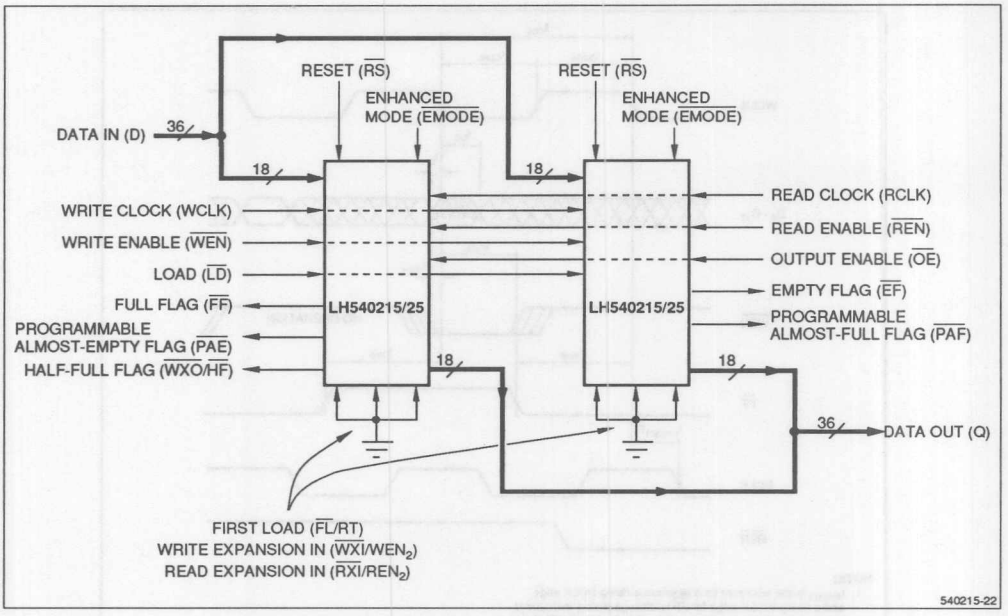


Figure 6. FIFO Word-Width Expansion (512 × 36/1024 × 36)

TIMING DIAGRAMS

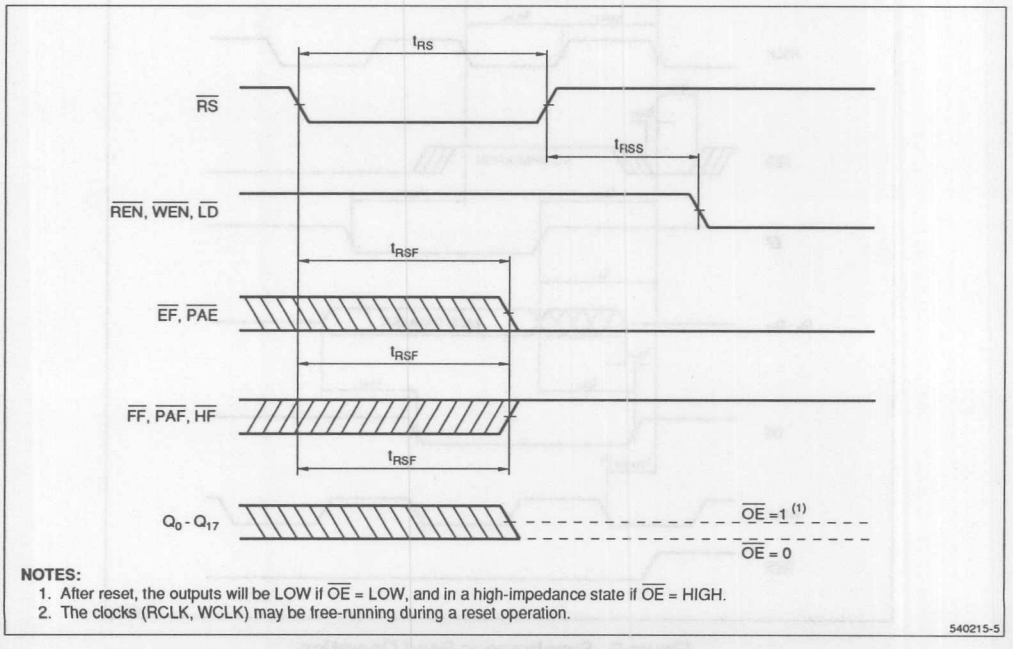


Figure 7. Reset Timing

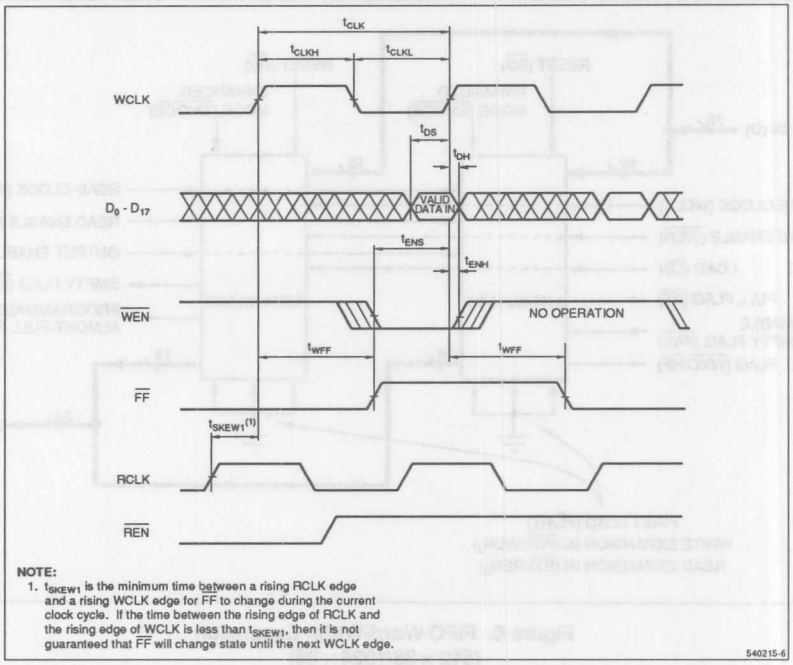


Figure 8. Synchronous Write Operation

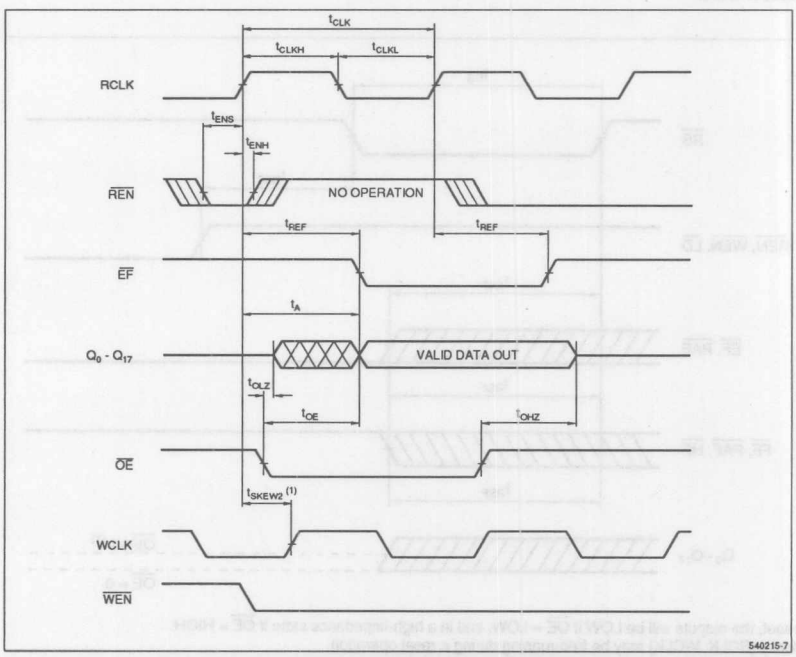


Figure 9. Synchronous Read Operation

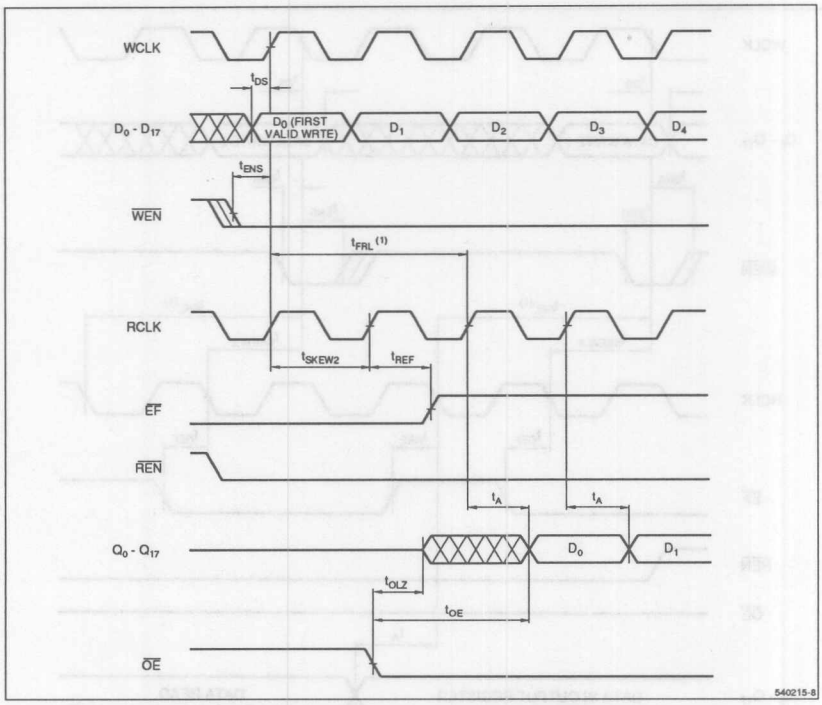


Figure 10. Latency for the First Data Word After a Reset Operation, With Simultaneous Read and Write

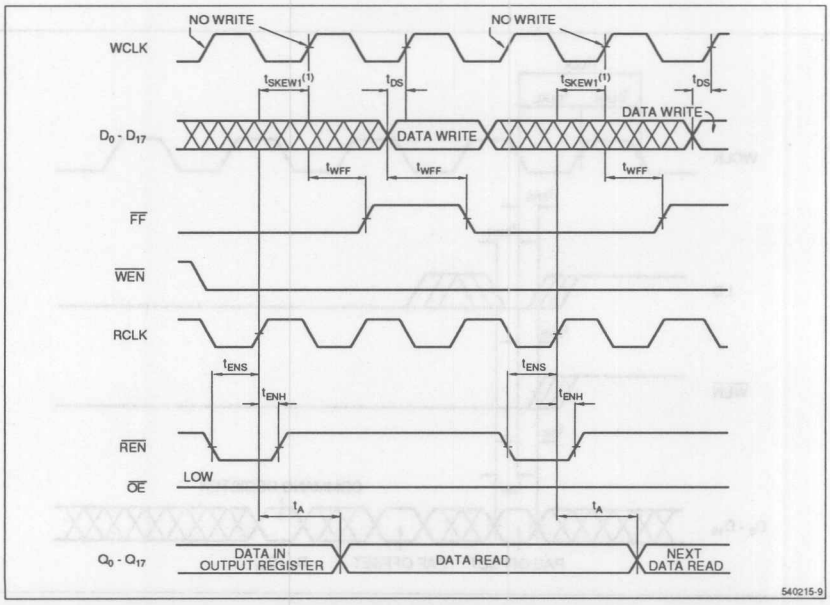


Figure 11. Full-Flag Timing

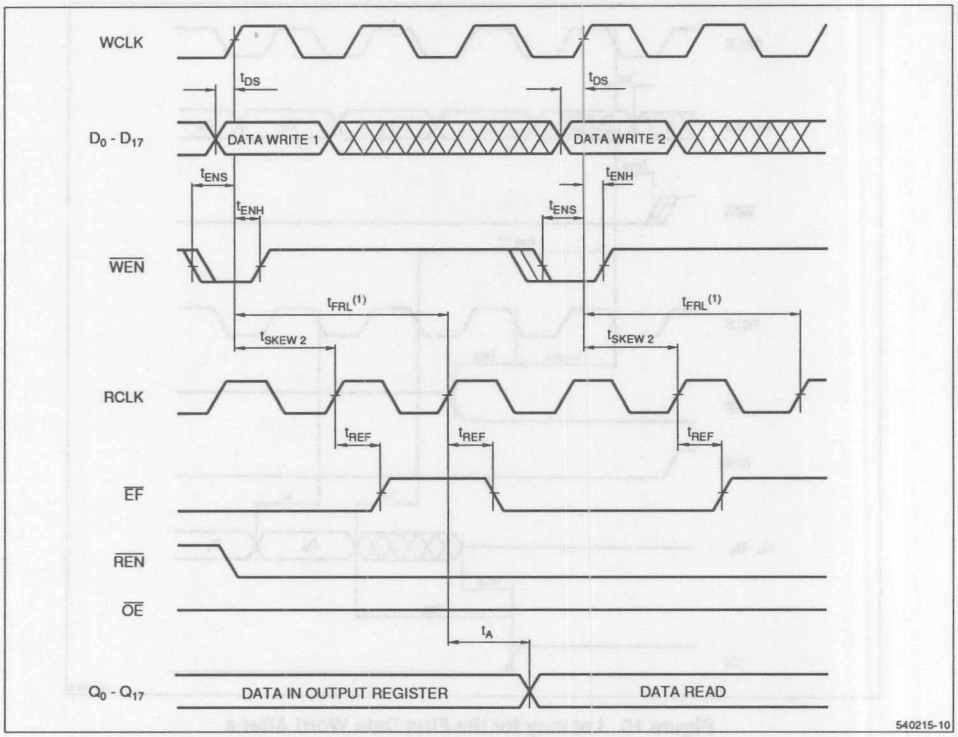


Figure 12. Empty-Flag Timing

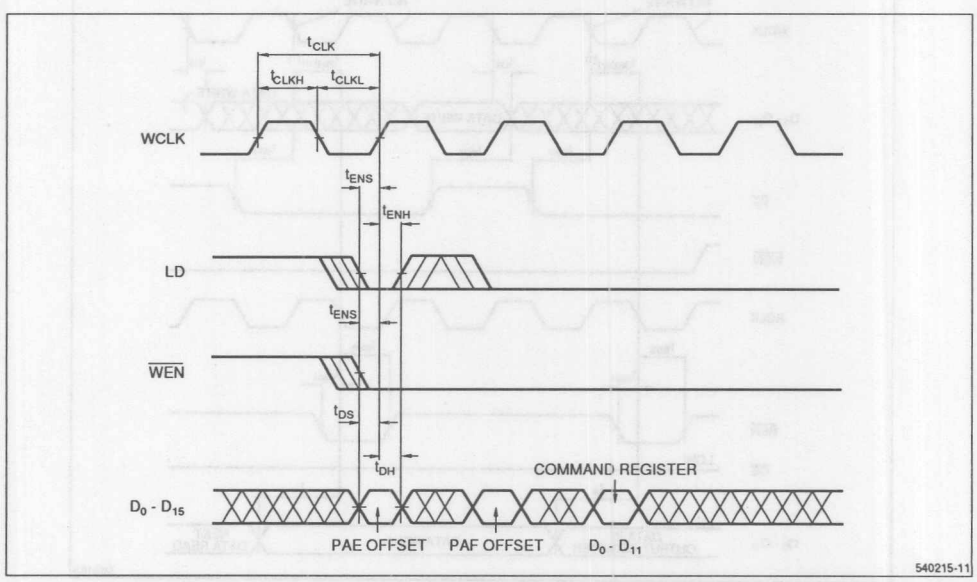


Figure 13. Resource-Register Write Operation

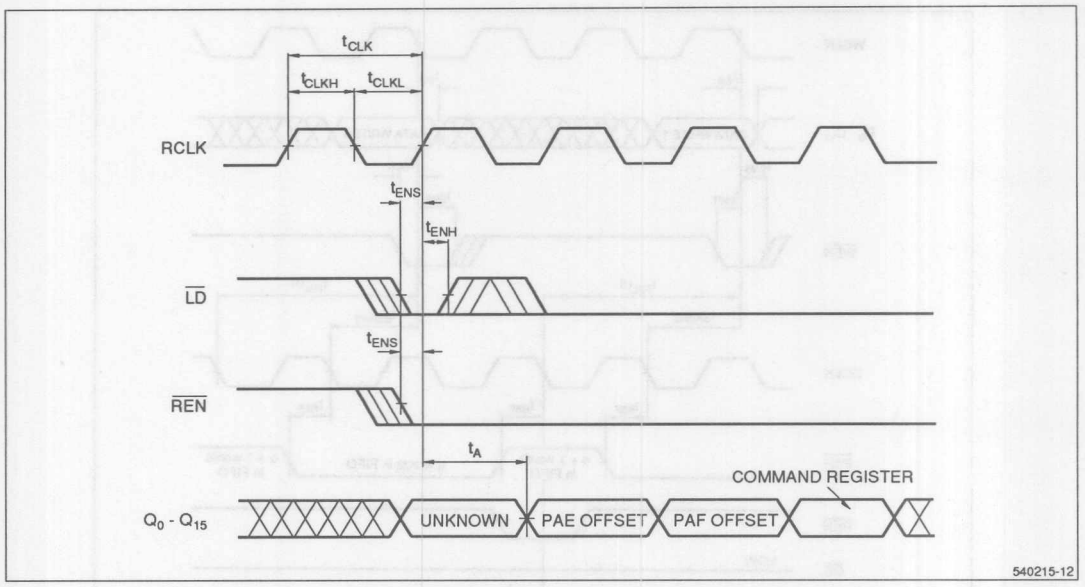


Figure 14. Resource-Register Read Operation

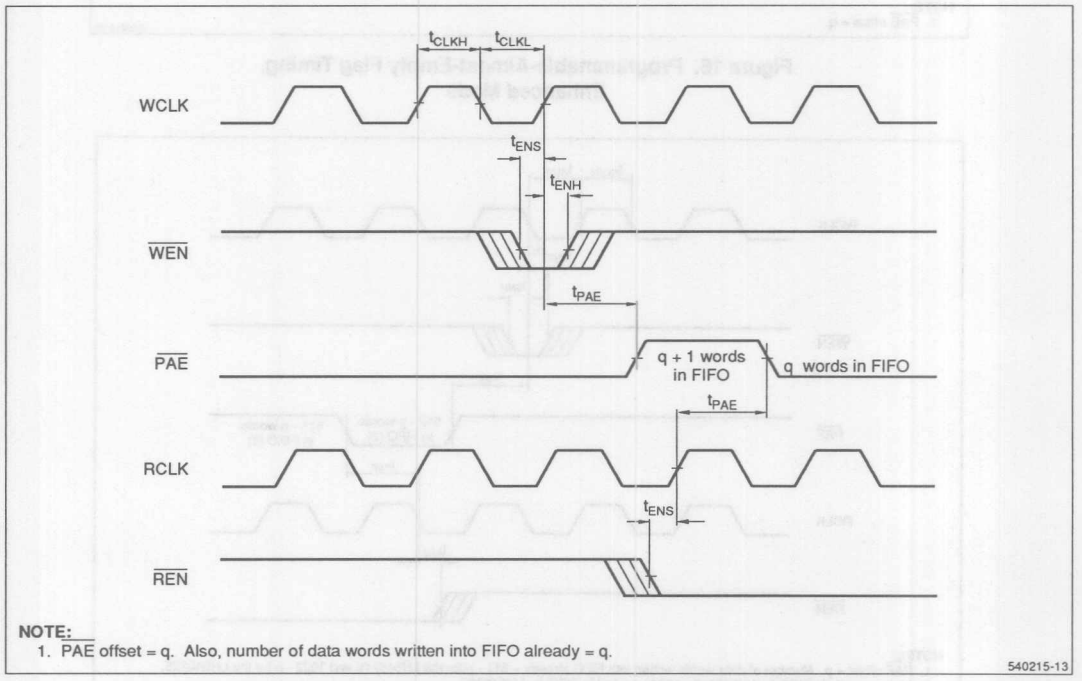


Figure 15. Programmable-Almost-Empty Flag Timing, Default Mode

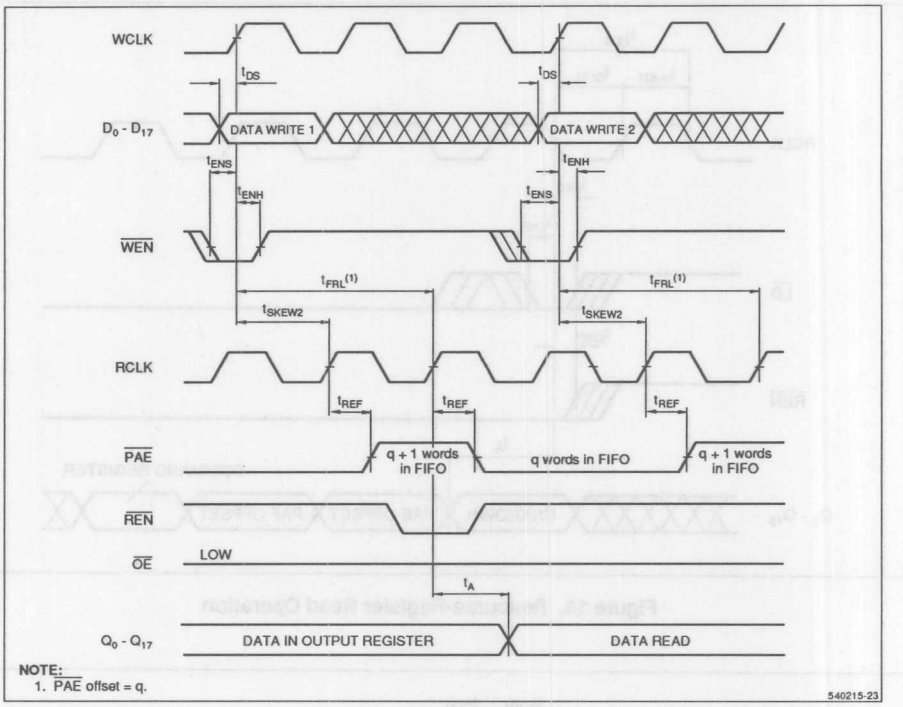


Figure 16. Programmable-Almost-Empty Flag Timing, Enhanced Mode

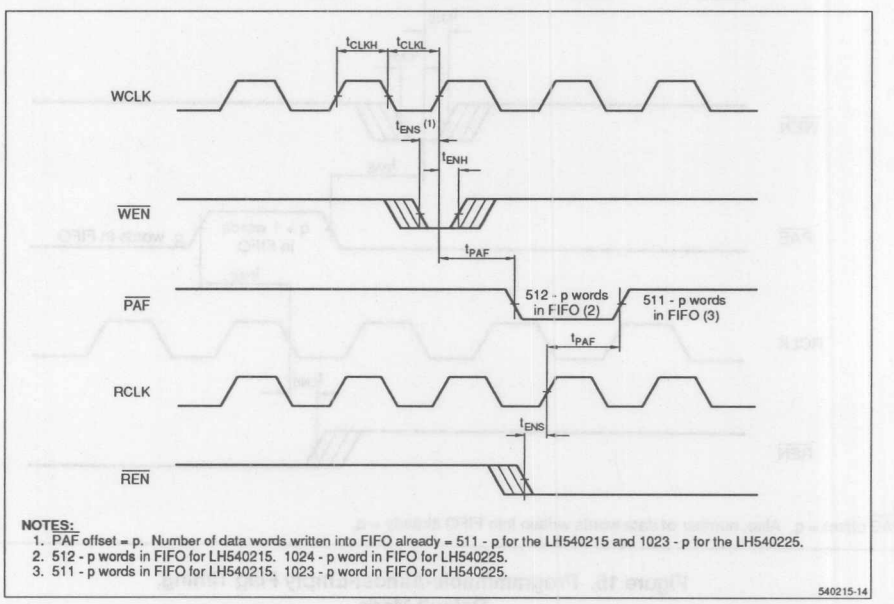


Figure 17. Programmable Almost-Full-Flag Timing, Default Mode

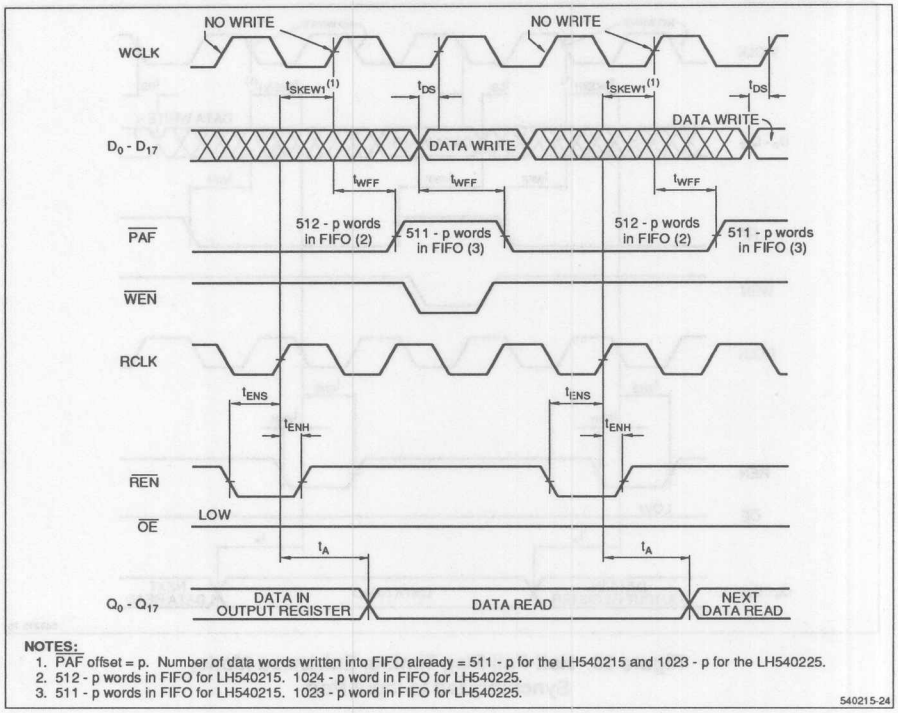


Figure 18. Programmable-Almost-Full-Flag Timing, Enhanced Mode

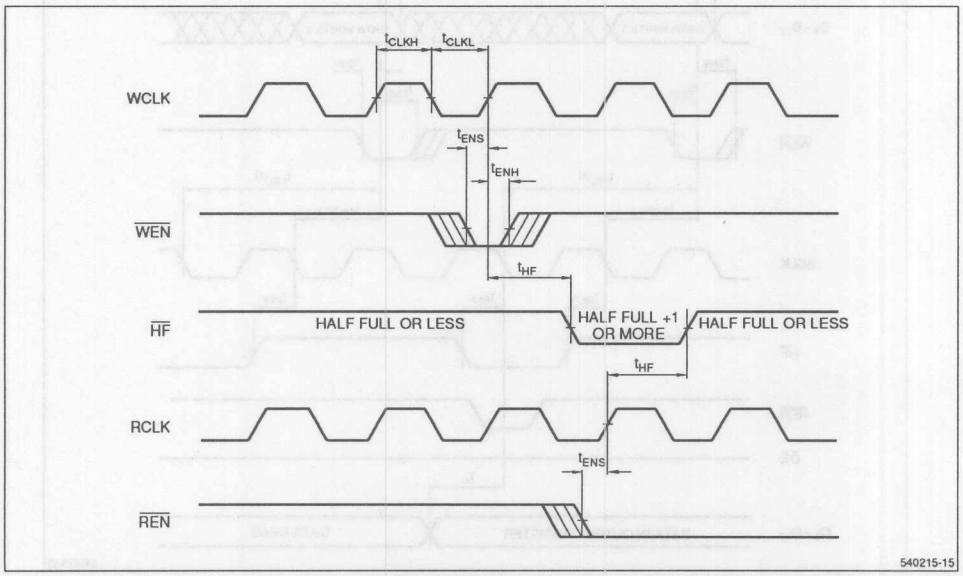


Figure 19. Half-Full-Flag Timing, Default Mode

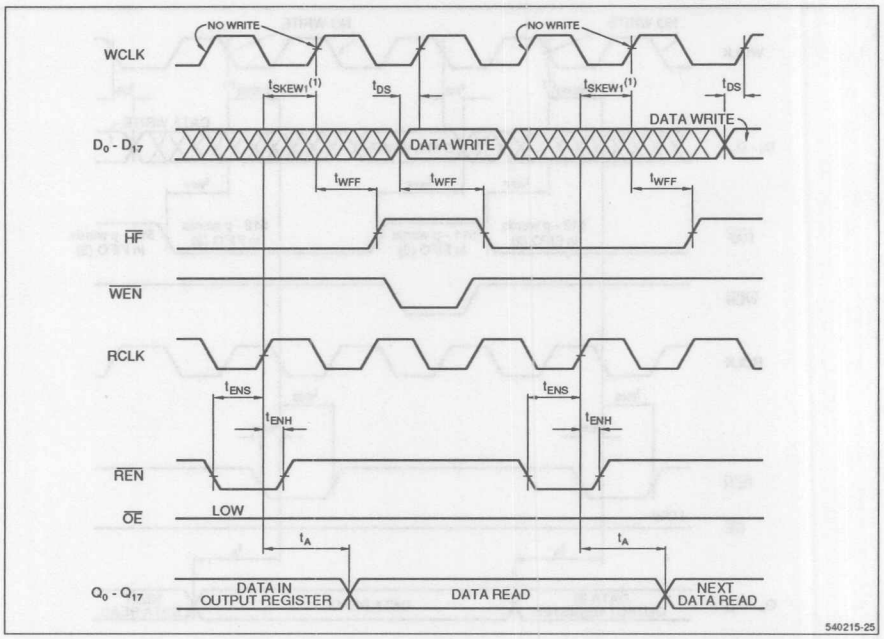


Figure 20. Half-Full-Flag Timing, Enhanced Mode, Synchronized to Input Port

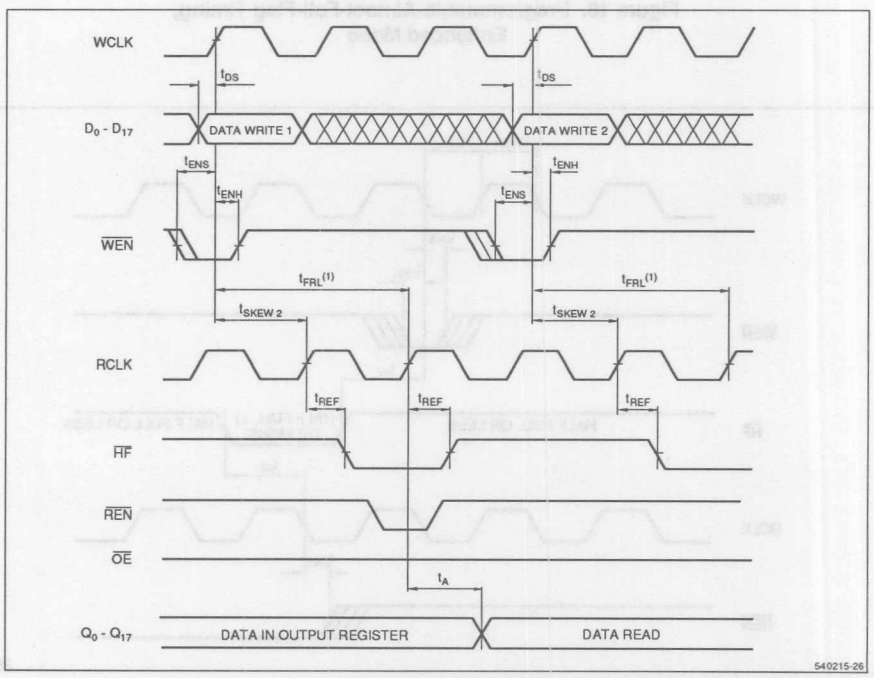


Figure 21. Half-Full-Flag Timing, Enhanced Mode, Synchronized to Output Port

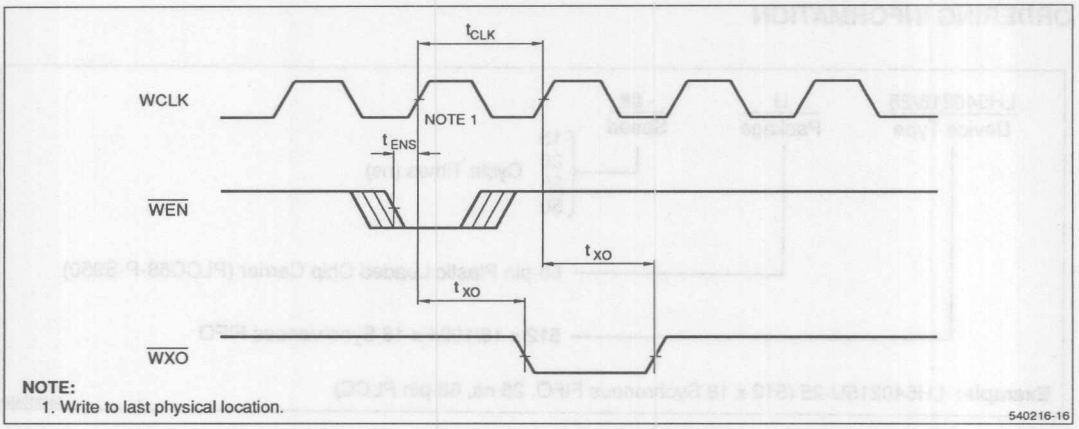


Figure 22. Write-Expansion-Out Timing, Default Mode

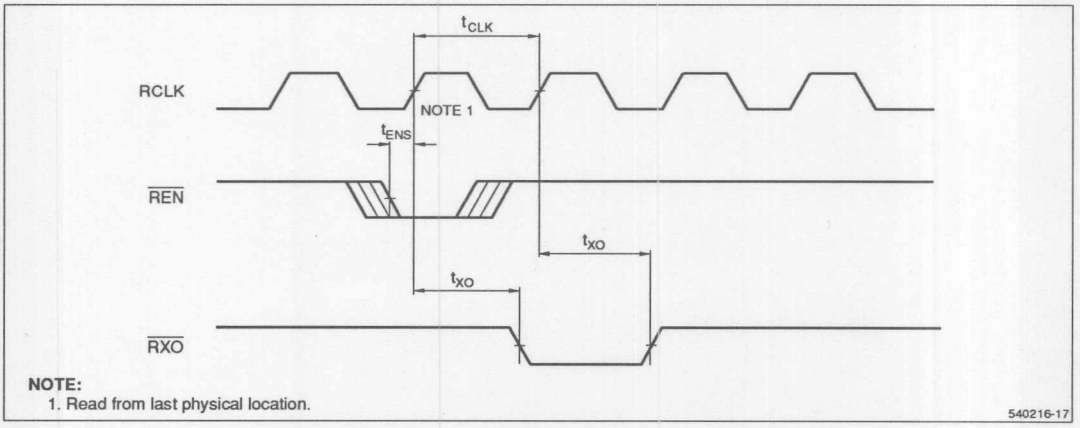


Figure 23. Read-Expansion-Out Timing, Default Mode

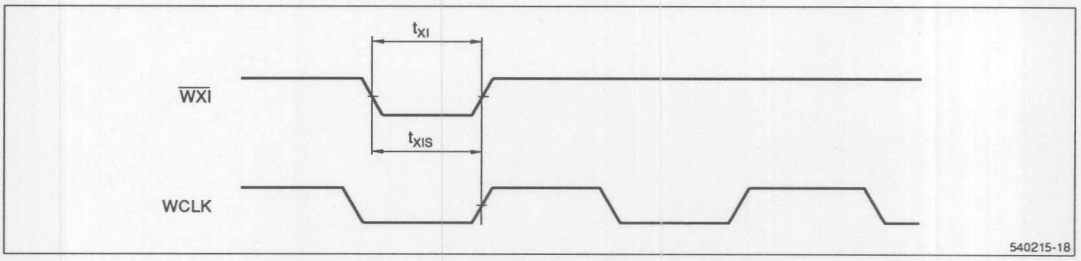
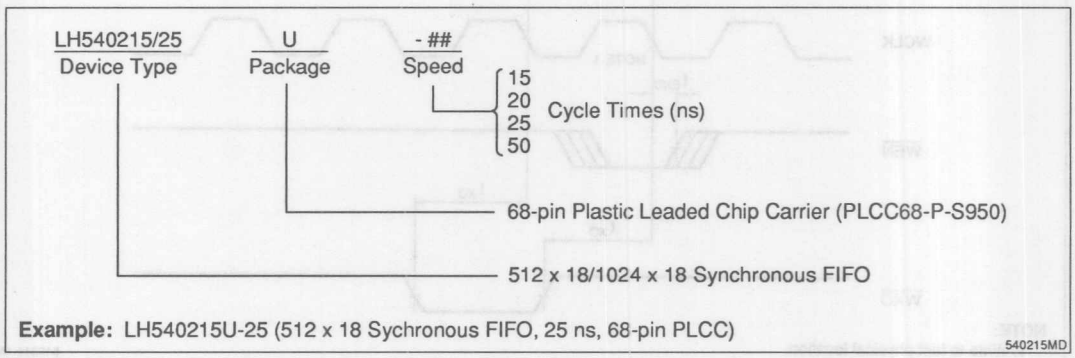


Figure 24. Write-Expansion-In Timing, Default Mode

ORDERING INFORMATION



LH543620

PRODUCT PREVIEW

1024 × 36 Synchronous FIFO

FEATURES

- Fast Cycle Times: 20/25/30 ns
- Selectable 36/18/9-Bit Word Width on *Both* Input Port and Output Port
- 'Synchronous' Enable-Plus-Clock Control at Both Ports
- Independently-Synchronized Operation of Input Port and Output Port
- Pinout Similar to LH5420 256 × 36 × 2 Bidirectional FIFO
- Most Control Input Signals are Synchronous, and are Assertive-LOW for Noise Immunity
- High-Drive Three-State Outputs
- Device Comes Up Into Known Default State at Reset; Programming is Allowed, but is not Required
- Five Status Flags: Full, Almost-Full, Half-Full, Almost-Empty, and Empty; 'Almost' Flags are Programmable
- All Five Status Flags are Completely Synchronous
- Duplicate Enables for Interlocked Paralleled FIFO Operation, for 72-Bit Data Width
- Data-Bypass Mode, Available at Any Time
- Mailbox Facility
- Automatic Byte Parity Checking; Also Byte Parity Generation, When Enabled
- Byte-Order-Reversal Facility
- 'Smart-Retransmit' Capability
- TTL/CMOS-Compatible I/O
- IEEE1149.1-Compliant (JTAG) Boundary-Scan Test Logic
- Space-Saving PQFP Package

FUNCTIONAL DESCRIPTION

The LH543620 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS RAM technology, capable of containing up to 1024 36-bit words. It can replace four or more byte-wide FIFOs in many applications, for microprocessor-to-microprocessor or microprocessor-to-bus communication. Its architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these 'clocks' also may be aperiodic, asynchronous 'demand' signals. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design.

The input port and the output port operate altogether independently of each other, unless the FIFO becomes either totally full or else totally empty. Data flow is initiated at a port by the rising edge of its corresponding clock, and is gated by the appropriate edge-sampled enable signals.

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Almost-Full and Almost-Empty flags are programmable over the entire FIFO depth; but they each are initialized to a default offset of eight locations from the respective boundaries during a reset operation. If this default offset is satisfactory, no further programming is required.

Both the input port and the output port may be set, *independently*, to operate at three data-word widths: 36 bits, 18 bits, and 9 bits. This setting may be changed during system operation; however, the word-width-control signals must meet the usual setup-time and hold-time conditions for control inputs.

Nine-bit bytes passing through the FIFO are assumed to be making use of a parity bit, and parity is automatically passively checked. A flag indicates the results of this parity checking; if parity checking is not desired, the value of this flag may be ignored. When the FIFO is reset, the parity-checking logic is initialized to use odd data parity; but the FIFO may be programmed to use either even parity or odd parity during subsequent operations. Also, the FIFO may be programmed to actively generate, and *record*, a parity bit into the most-significant bit of each 9-bit byte of data passing through the internal memory array, overwriting the previous contents of those bits.

Coordinated operation of two paralleled LH543620 FIFOs, as one 1K × 72 FIFO, may be ensured by 'interlocked' crosscoupling of the $\overline{FF}$ and $\overline{EF}$ outputs from each FIFO to one of the assertive-HIGH enable inputs of the other one; for instance, $\overline{FF}$ to ENI_2, and $\overline{EF}$ to ENO_2, in *both* directions between two paralleled LH543620s. (Note: $\overline{FF}$ may be interpreted as assertive-HIGH 'Input Ready,' and $\overline{EF}$ likewise may be interpreted as assertive-HIGH 'Output Ready.')

The LH543620 has a data-bypass mode, which directly connects the output port to the input port so that the LH543620 behaves like a 36-bit three-state-output buffer. Also, a mailbox facility is provided from the input port to the output port, to support using two LH543620s connected 'back-to-back' as a 1024 × 36 × 2 bidirectional FIFO.

The LH543620 can reverse the order of the four nine-bit bytes of each 36-bit data word passing through it, thus accomplishing 'Big Endian' ↔ 'Little-Endian' conversion.

The LH543620's 'smart-retransmit' capability supports use of the FIFO in data-communications applications, and also as a working memory in digital-signal-processing systems. The LH543620's internal-memory read pointer can be reset to point to *any* arbitrary location in the memory, not just to physical location zero.

PRODUCT PREVIEW

LH54B520

1024 x 36 Synchronous FIFO

FEATURES

- Fast Cycle Times: 20/25/30 ns
- Selectable 36/18-Bit Word Width on Both Input and Output Port
- Synchronous Enable-Plus-Clock Control at Both Ports
- Independently-programmed Detection of Input and Output Full
- Preset Size for LH5420 256 x 36 x 2 Bidirectional FIFO
- Input Control and Flag Signals are Synchronous, and are Active-LOW for Noise Immunity
- High-Drive Three-State Outputs
- Device Comes Up into Known Default State at Power Up; Programming is Allowed, but is not Required
- Five Status Flags: Full, Almost-Full, Half-Full, Almost-Empty, and Empty; Almost-Full logic has Programmable
- All Five Status Flags are Completely Synchronous
- Duplicate Enables for Interfaced Parallelled FIFO Operation, for 72-Bit Data Width
- Data Bypass Mode, Available at Any Time
- Mailbox Facility
- Automatic Byte Parity Checking, Also Byte Parity Generation, When Enabled
- Byte Order-Reversal Facility
- Small Package: Capability
- TTL/CMOS Compatibles I/O
- IEEE 1149.1-Compliant (JTAG) Boundary-Scan Test Logic
- Space-Saving PQFP Package

FUNCTIONAL DESCRIPTION

The LH54B520 is a FIFO (First-In, First-Out) memory device, based on fully-static CMOS RAM technology, capable of operating up to 1024 36-bit words. It can replace four or more byte-wide FIFOs in many applications, for microprocessor-to-microprocessor or microprocessor-to-bus communication. Its architecture supports synchronous operation, tied to two independent free-running clocks at the input and output ports respectively. However, these clocks also may be operated asynchronously whenever appropriate. Almost all control input signals and status output signals are synchronized to these clocks, to simplify system design.

The input port and the output port operate absolutely independently of each other, unless the FIFO becomes either totally full or else totally empty. Data flow is initiated at a port by the rising edge of its corresponding clock, and is gated by the appropriate edge-sampled enable signals.

The following FIFO status flags monitor the extent to which the internal memory has been filled: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Almost-Full and Almost-Empty flags are programmable over the entire FIFO depth but they each are initialized to a default offset of eight locations from the respective boundaries during a reset operation. If this default offset is satisfactory, no further programming is required.

Both the input port and the output port may be addressed to be reading or writing data-word widths of 36 bits, and 9 bits. This setting may be changed during system operation, however the word-width control signals must meet the usual setup-time and hold-time conditions for control inputs.

Byte-by-byte passing through the FIFO can be assumed to be meaningful use of a parity bit, and parity is automatically generated and checked. A flag indicates the results of this parity checking. Parity checking is not obligatory, the value of this flag may be ignored. When the FIFO is reset, the parity-checking logic is initialized to use odd data parity but the FIFO may be programmed to use either even parity or odd parity during subsequent operations. Also, the FIFO may be programmed to actively generate, and record, a parity bit into the most-significant bit of each 9-bit byte of data passing through the internal memory array, overwriting the previous contents of those bits.

Coordinated operation of two paralleled LH54B520 FIFOs, as one 1K x 72 FIFO, may be ensured by interlocked cross-coupling of the $\overline{FF}$ and $\overline{EF}$ outputs from each FIFO to one of the assertive-HIGH enable inputs of the other one, for instance, $\overline{FF}$ to $\overline{ENi}$, and $\overline{EF}$ to $\overline{ENO}$. In both directions between two paralleled LH54B520s, (Note: $\overline{FF}$ may be interpreted as assertive-HIGH "Input Ready" and $\overline{EF}$ likewise may be interpreted as assertive-HIGH "Output Ready".)

The LH54B520 has a data-bypass mode, which directly connects the output port to the input port as does the LH52B520 it shares the 36-bit three-state-output bypass bus. Also, a mailbox facility is provided from the input port to the output port, to support using two LH54B520s connected back-to-back as a 1024 x 36 x 2 bidirectional FIFO.

The LH54B520 can reverse the order of the four nine-bit bytes of each 36-bit data word passing through it, thus accomplishing "Big Endian" ↔ "Little-Endian" conversion.

The LH54B520 is a "smart-returnent" or locally-smarts use of the FIFO in data-communications applications, and also as a working memory in digital-signal-processing systems. The LH54B520's internal-memory read pointer can be reset to point to any arbitrary location in the memory, not just to physical location zero.

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APPLICATION NOTES AND CONFERENCE PAPERS

Databus Funneling Made Easy	6-1
A One-Chip Two-Way Street for Microprocessor Communications: the Sharp LH5420 36-Bit Bidirectional FIFO	6-7
FIFO Memories: Effective, Compact, and Easy to Use	6-12

LH5420

Synchronous Bidirectional FIFO

DATABUS FUNNELING MADE EASY

Mike Yee, Senior Applications Engineer

INTRODUCTION

The Sharp LH5420 256 × 36 × 2 CMOS Bidirectional FIFO is an innovative device which turns the difficult task of funneling and defunneling different-size databuses into an easy one-component solution. Funneling refers to a situation where data from a larger databus (eg. 32-bits wide, 36-bits with parity) must be segmented (usually in increments of 8-bits, 9-bits with parity) and transferred to a smaller databus (eg. 8-bits wide, 9-bits with parity). The funneling options available on the LH5420 are '36-bits to 9-bits' and '36-bits to 18-bits.' Defunneling refers to just the opposite of funneling. To defunnel, data from a smaller databus (eg. 8-bits wide, 9-bits with parity) is combined together sequentially with other data from that databus, and transferred in parallel to a larger databus (eg. 32-bit wide, 36-bit with parity).

The defunneling options available are '9-bits to 36-bits' and '18-bits to 36-bits.' For wide word applications on both ports, '36-bit to 36-bit' buffering is also available.

A very important feature of the LH5420 is the ability to operate bidirectionally. The term Bidirectional refers to the LH5420s ability to funnel and defunnel between different sized databuses, allowing data to travel in both directions. Bidirectional operation is also available when the full width of both ports are used (eg. 36-bit to 36-bit buffering).

The advantages of the LH5420 bidirectional FIFO to the system designer are: elimination of several conventional FIFOs and glue logic; significant reduction of board space; elimination of the complexities of handling bus contention; and improved system performance. But, most importantly, it makes databus funneling easy.

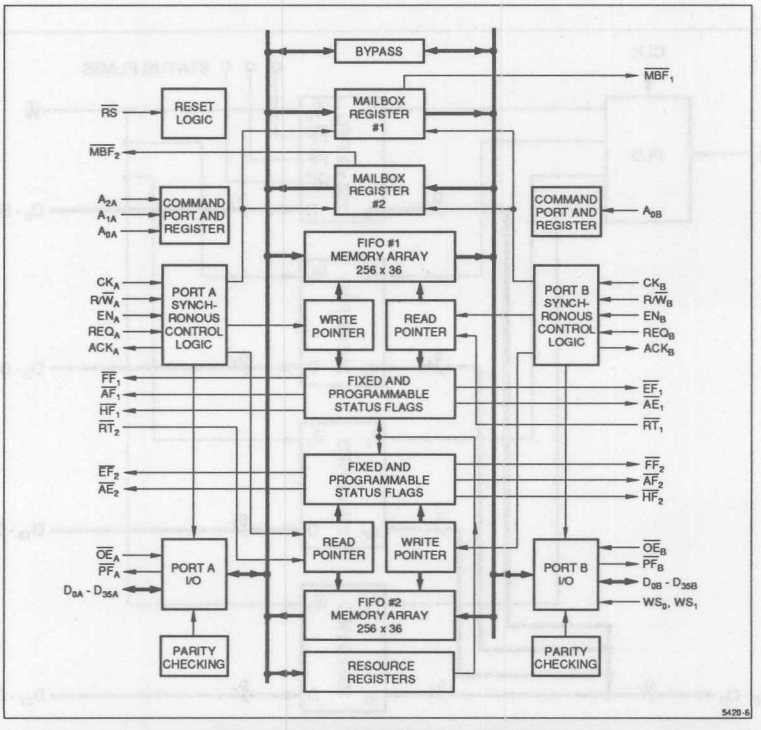

Figure 1. LH5420 Block Diagram

CONVENTIONAL DATABUS FUNNELING SOLUTIONS CAN BE AWKWARD

The rapid transfer of information between a databus of one size to a databus of a different size (funneling or defunneling) seems like a simple enough operation, when viewed on paper in block diagram form; but the block diagram must be transformed into a high-speed circuit design. Conventional solutions require many components, and considerable board area. Further, the timing required for reading, writing, and flag detection for multiple parts in parallel, places a heavy burden on reliable high speed operation.

CONVENTIONAL FUNNELING CIRCUIT DESIGN

Figure 2 shows a bus-funneling circuit designed using conventional components. Figure 2a is an example of the timing required to use the circuit in Figure 2. Figure 3 shows the circuit which must accompany Figure 2 if the circuit were expected to operate bidirectionally (funnel and defunnel). Figure 3a is an example of the timing required to use the circuit in Figure 3. An obvious disadvantage of this conventional funneling circuit is the number of components required. One "Programmable Logic Device" (PLD) and four standard 256 × 9 FIFOs are required for one-way funneling. If bidirectional operation (funneling and defunneling) is important, two PLD's and eight 256 × 9 FIFOs are required. The combination of all these components results in very restrictive data setup (t_{DS}) and hold (t_{DH}) timings during a Write cycle, and restrictive access timings (t_A) due to the risk of databus contention during a Read cycle. In many cases, high speed operation would be out of the question. Tight controls on signal noise and signal skew might also be required to keep the four FIFOs synchronized. After all this, the circuit designer would do just about anything for a single-chip solution. Setup and Hold times for a single asynchronous 256 × 9 FIFO are typically 10 ns and 0 ns respectively for access times of 20 ns. Because this defunneling circuit is a combination of separate components (see Figure 3), setup and hold times would have to be increased significantly to ensure correct synchronization due to signal propagation delays of the control signals and data. In a conventional defunneling circuit, there could be as many as four 9-bit words waiting to be written sequentially into four different FIFOs. Each of the four 9-bit words requires its own setup (t_{DS}) and hold (t_{DH}) time (see Figure 3a). These restrictions will limit the maximum defunneling frequency of this circuit.

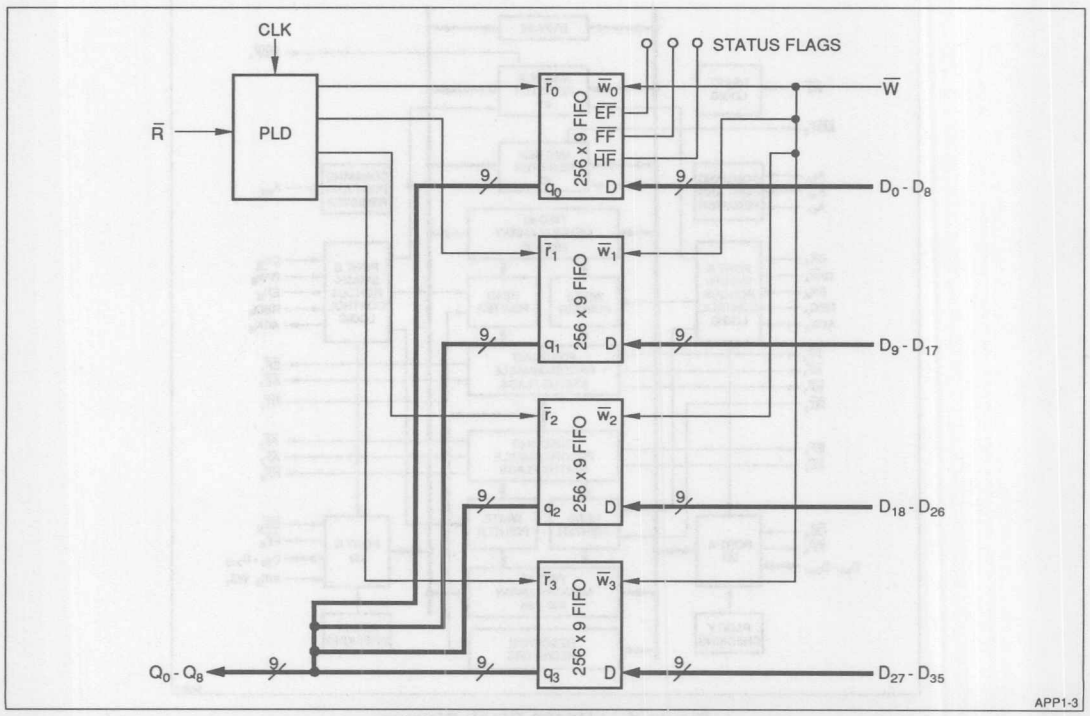

Figure 2. 36-Bit to 9-Bit Conventional Funneling FIFO Circuit

Databus contention is a common problem experienced when combining two or more output pins from different devices in parallel, on the same databus (see Figure 2). If during a Read cycle, at least two of the output pins happen to be momentarily on at the same time, the two output drivers potentially could fight against each other driving the data bus to opposite logic states (one driver pulling the bus to 0V, while the other driver is simultaneously pulling the bus to 5 V). Databus contention degrades system performance and increases the system operating current.

Another significant disadvantage with using the conventional component solution is handling the flags. Each 256 × 9 FIFO has 3 types of flags which can be used in the application to indicate the current FIFO status (Empty, Full, or Half Full). Most designers use a flag from only one of the four FIFOs. This flag-handling technique has a significant disadvantage. When a flag from only one of the four 9-bit wide FIFOs is used to represent the entire 36-bit word, there is no way to insure that the other three FIFO flags are synchronized (empty, full, or half full at the same time) with the first. There is the possibility that one, two, or all three of the other FIFOs may have become unsynchronized (due to signal noise, excessive signal skew, etc.) and are now contributing incorrect data to the 36-bit word.

SHARP's Single Chip Solution to the Complexities of Funneling

The LH5420 CMOS Bidirectional FIFO was designed specifically to simplify the handling of wide-word (up to 36-bits) data buffering. The notable features of this device relating to data bus funneling are:

- Selectable 36/18/9-bit Word Width on Port B
- Two 256 × 36-bit FIFO Buffers for Bidirectional Operation
- Synchronous operation on both Ports A and B
- Fully Asynchronous Communications between Port A and Port B
- Only One Set of Flags for the Entire 36-bit Wide Word
- Capable of 40 MHz operation

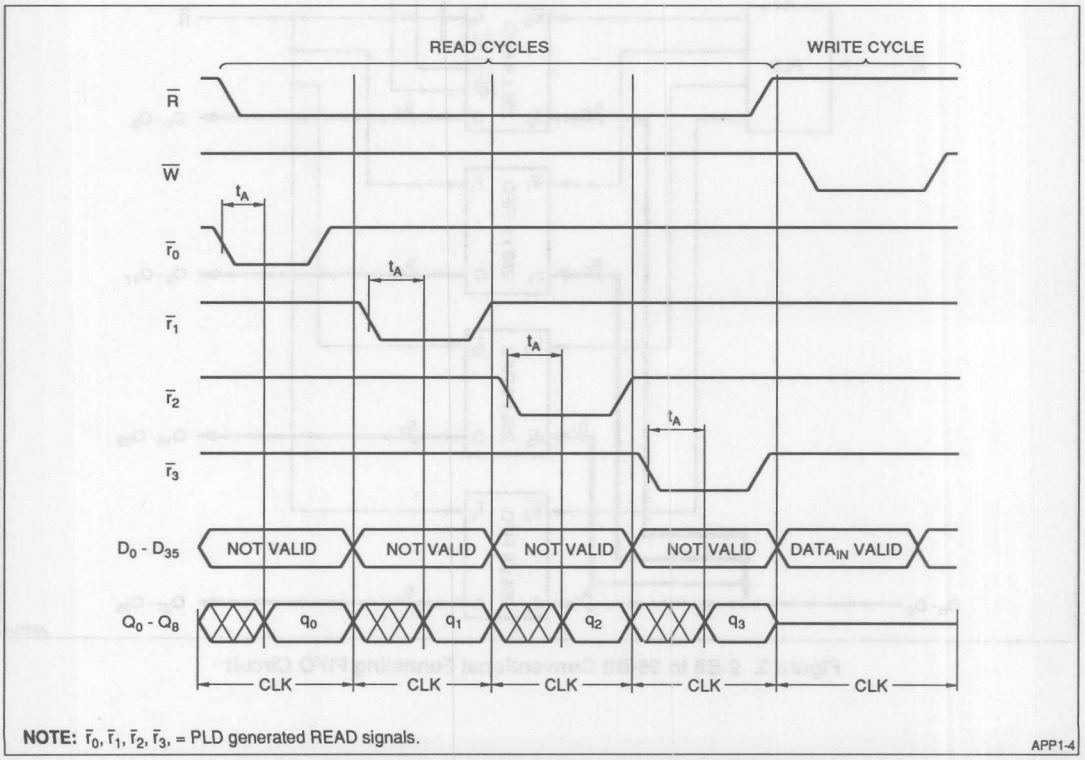

Figure 2a. 36-Bit to 9-Bit Conventional Funneling Write and Read Timing Diagram

The LH5420 provides an easy one chip solution to the problems associated with funneling one size databus to a different size databus (see Figure 3). The LH5420 also provides a simple method of buffering wide word databusses up to 36 bits wide on each port. There are two ports on the LH5420, Port A and Port B. A Port is defined as an interface between the outside databus and the internal FIFO memory. Each port can be used as an input or an output depending on which direction the data will travel. The LH5420 allows Port B to be selectable in word widths from 36, 18 or 9 bits wide, while Port A is fixed at 36-bits wide.

Two separate 256 × 36-bit FIFO buffers work side-by-side to move data in opposite directions. This is what enables the LH5420 to operate bidirectionally. As an example, a 36-bit databus and a 9-bit databus can send and receive data back and forth, giving unrestricted communication privileges between an 8-bit microcontroller and a 32-bit microprocessor. Clock-frequency differences between the two busses are not an issue. Even though the individual ports are synchronous in nature, each port is controlled from separate system clocks (CKA and CKB). Each port operates independently from the other, so that port-to-port communication occurs asynchronously.

The LH5420 has five different types of flags available: Full Flag (FF), Empty Flag (EF), Half Full Flag (HF), Almost Full Flag (AF), and Almost Empty Flag (AE). The Almost Empty and Almost Full Flags are programmable. One set of these flags are available for each 256 × 36 FIFO buffer, to cover the status of data going in either direction. The low skew inherent in a single monolithic solution eliminates the risk that desynchronization will occur within the 36-bit wide word in the FIFO. Further protection is afforded because the flags cover the full 36-bit word width and not just the 9 bits that were used in the conventional funneling design mentioned above. The problems of designing a system around restrictive read and write timing constraints are no longer an issue, because the complexities of funneling timing synchronization are handled automatically within the LH5420 bidirectional FIFO.

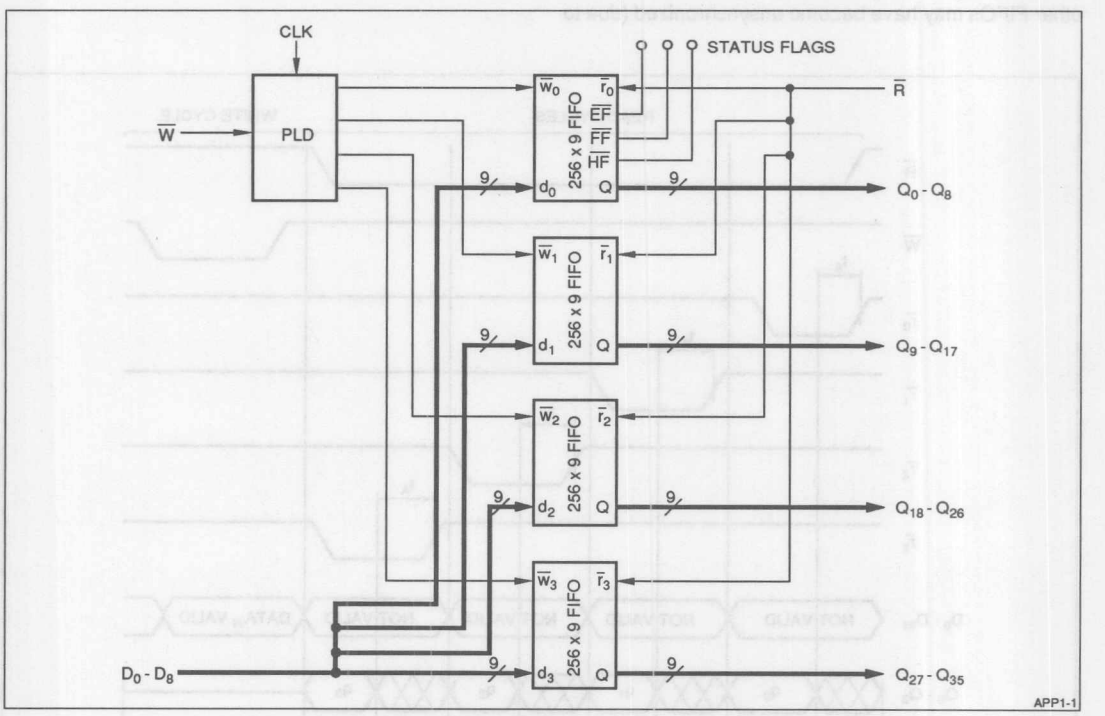

Figure 3. 9-Bit to 36-Bit Conventional Funneling FIFO Circuit

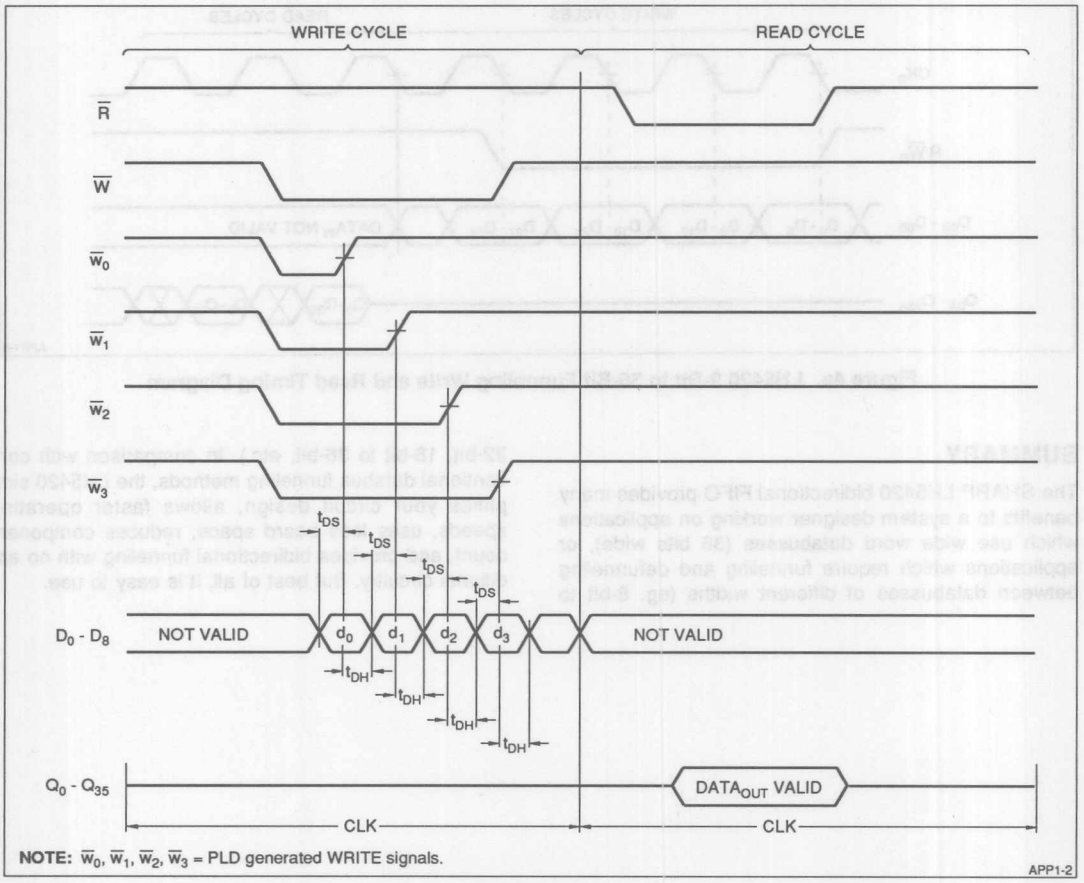

Figure 3a. 9-Bit to 36-Bit Conventional Defunneling Read and Write Timing Diagram

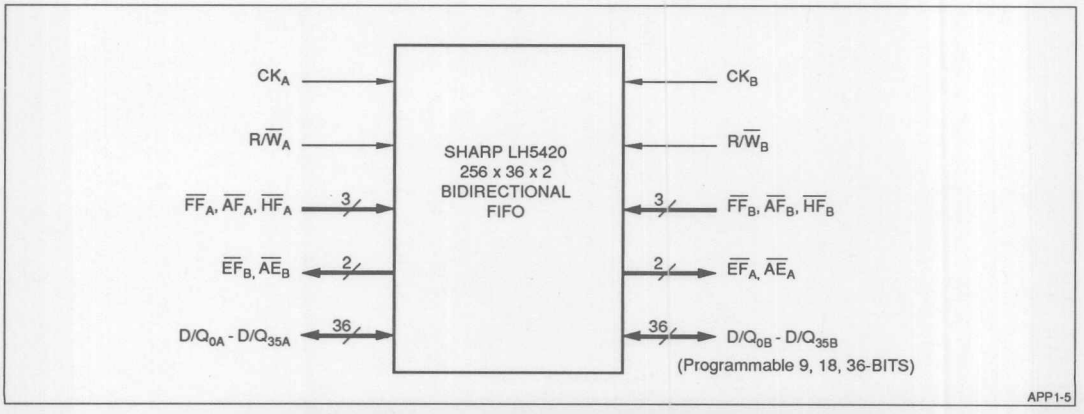

Figure 4. LH5420, the Single Chip Solution for Databus Funneling

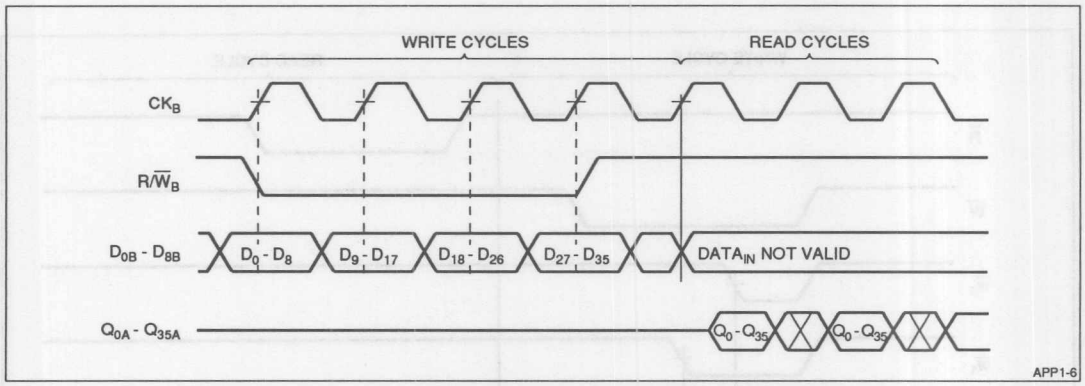

Figure 4a. LH5420 9-Bit to 36-Bit Funneling Write and Read Timing Diagram

SUMMARY

The SHARP LH5420 bidirectional FIFO provides many benefits to a system designer working on applications which use wide word databusses (36 bits wide), or applications which require funneling and defunneling between databusses of different widths (eg. 8-bit to 32-bit, 18-bit to 36-bit, etc.). In comparison with conventional databus funneling methods, the LH5420 simplifies your circuit design, allows faster operating speeds, uses less board space, reduces component count, and provides bidirectional funneling with no additional circuitry. But best of all, it is easy to use.

A ONE-CHIP TWO-WAY STREET FOR MICROPROCESSOR COMMUNICATIONS: THE SHARP LH5420 36-BIT BIDIRECTIONAL FIFO *

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INTRODUCTION

New integrated circuits often evolve as single-chip embodiments of groups of lower-complexity parts. When the same multiple-device configuration starts turning up in many new designs, a semiconductor manufacturer may get inspired to develop a one-chip-does-all replacement just by listening to its customers. Bidirectional FIFOs, wide enough to hold an entire word of data, are one such frequently-occurring combination. Perhaps one out of every five system applications for FIFOs fits this description. Usually, the role of a bidirectional FIFO is to provide convenient two-way communication between two processors or microprocessors.

In the past, an effective bidirectional FIFO for communication back and forth between two 32-bit-processors has needed to consist of at least *eight* industry-standard byte-wide unidirectional FIFO devices, arranged into two 'back-to-back' ranks of four paralleled FIFOs each. When parity checking is implemented, the data path between processors becomes 36-bit. Sometimes only one of the two processors is 32-bit, and the other one is 16-bit or 8-bit. In this event, even more devices must be added, to implement multiplexing, demultiplexing, and control functions at the narrower end of the bidirectional data path.

The LH5420 256 × 36 × 2 bidirectional FIFO, now available from Sharp, is a 'one-chip-does-all' solution to such system requirements for two-way interprocessor communication. One LH5420 can provide either a convenient fully-parallel two-way connection from one 36-bit bus to another such bus, or it can provide a two-way 'funneling/defunneling' connection from a 36-bit bus to an 18-bit bus, or to a 9-bit bus. Thus, the LH5420 supports all of the usual microprocessor word widths, and accommodates the extra bit per byte for parity or marker-bit usage. It operates at up to 40 MHz, and is available either in a 120-pin PGA package or in a 132-pin PQFP package.

LH5420 ARCHITECTURE AND OPERATION

The LH5420 includes several enhancements, aimed at making a system designer's life easier. The LH5420 itself can check the parity of all bytes passing through it in either direction. And it features programmable almost-full and almost-empty flags, retransmission capability in either direction, 'mailbox' capability in either direction, a limited form of transceiver-mode oper-ation, and a synchronous request/acknowledge capability which is useful in burst-mode communications.

Conceptually, an LH5420 is organized as two 36-bit-wide bidirectional ports, Port A and Port B. Two full-width 256-word FIFOs, FIFO # 1 and FIFO # 2, are connected between the two ports, one transmitting in each direction. (See Figure 1.) There are also two full-width one-word mailboxes between the two ports, one likewise transmitting in each direction. And there is a

* See copyright information on pages 6-11.

full-width bidirectional data bypass path, which functions during a reset operation. Two asynchronous control inputs set the data width of Port B at 36 bits, at 18 bits, or at 9 bits.

Each port has its own clock input. In typical applications, a port's clock input is connected to a periodic free-running clock signal, which may or may not be derived from the same frequency source as the other port's clock input. Each port also has three control inputs which are sampled at the rising edge (LOW-to-HIGH transition) of its clock: read/write, enable, and request. Each port also has an 'Acknowledge' output which is synchronized to its clock, a parity flag output, and asynchronous control inputs for initiating data re-transmission and for enabling/disabling its data outputs.

FIFO # 1 and FIFO # 2 each have five status flags to indicate relative fullness: Full, Almost-Full, Half-Full, Almost-Empty, and Empty. The Full, Half-Full, and Empty flags are hard-wired to signal exactly what their names indicate. But there are programmable 'offsets' controlling the operation of the Almost-Full and Almost-Empty

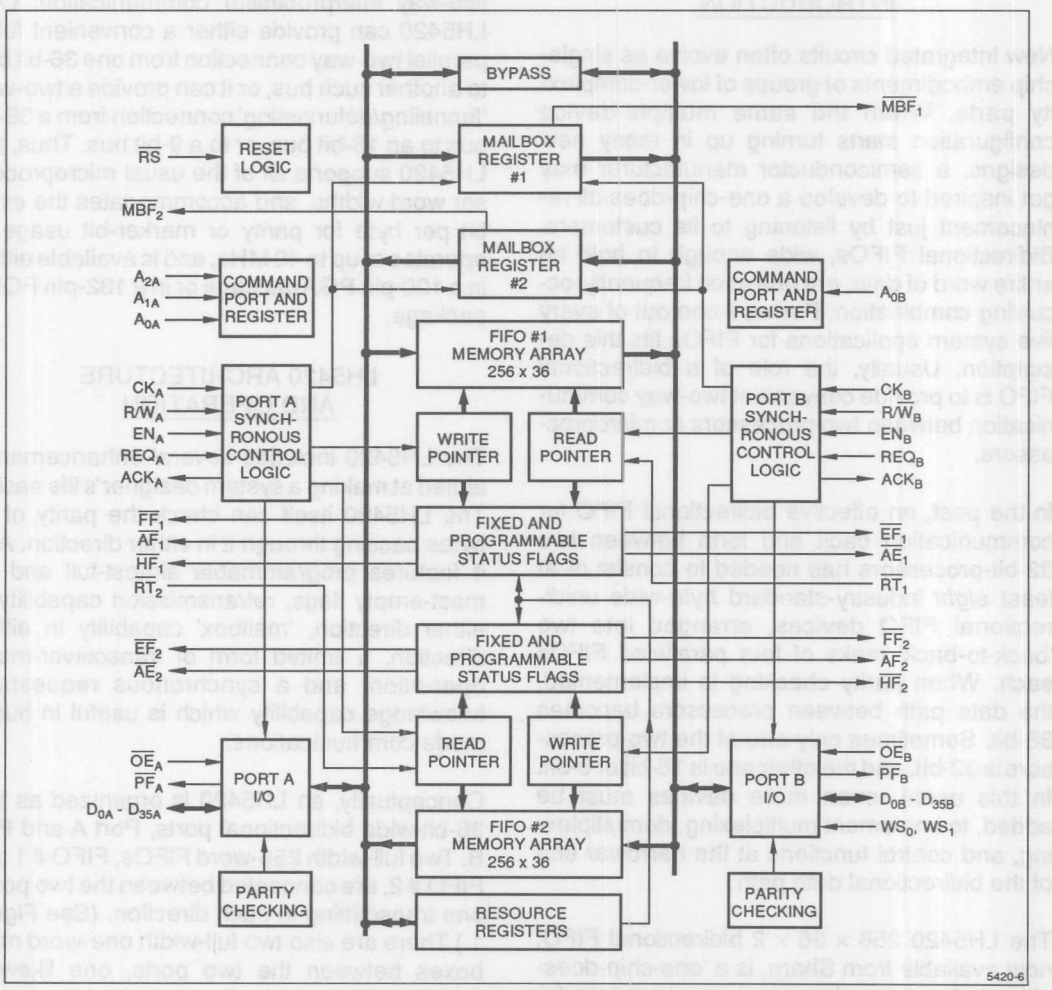

Figure 1. LH5420 Block Diagram

flags, to numerically define the boundaries of the 'Almost-Full' region and the 'Almost-Empty' region. These offset values are both initialized to eight during a reset operation; but either one may be changed under system control, independently of the other one, to any value from zero to 255.

While a data transfer is actually taking place, the port's Acknowledge output repeats the same information as either the Almost-Full flag or the Almost-Empty flag, depending on the current direction of data transfer – Almost-Full when writing, and Almost-Empty when reading.

The five relative-fullness status flags may change state either in response to a write event clocked at one port, or else in response to a read event clocked at the other port. The port's Acknowledge output signal, however, is totally synchronous with the clock input signal at that port; except, that it gets deasserted immediately if at any time the Request input signal is deasserted.

Both the Request control input and the Enable control input of a port must be asserted, in order for that port to carry out a read operation or a write operation. The Read/Write control input determines which type of operation gets performed.

The action of the Request and Enable signals within the LH5420 are generally similar; but their detailed timing is different. The Enable signal is presumed to be originating as a synchronous signal referenced to the same clock signal used by the port. On the other hand, the Request signal may arise asynchronously, elsewhere in the system; the LH5420 contains resynchronizing circuits, which reference the Request signal to the port clock internally within the LH5420.

Either port may place a full 36-bit word in the other port's mailbox register. Doing so sets a mailbox flag, which is synchronized to the receiving port's clock. This flag is reset whenever the receiving port has read the word in the mailbox register. Both ports have the ability to select either their outgoing FIFO or their outgoing mailbox for writing, or either their incoming FIFO or their incoming mailbox for reading.

Although Port A and Port B both have the capability to send and receive 36-bit data words, each port has one major function unique to it. Port A is the master port for purposes of resource-allocation and control functions, such as changing the value of the offsets for the Almost-Full and Almost-Empty flags, or changing the byte parity scheme from odd parity to even parity. Port B, on the other hand, is the port which is capable of setting its effective data width at 36 bits, 18 bits, or 9 bits.

Two asynchronous inputs control the data width of Port B. Changing this data width does not require any reset operation. However, sufficient time must be allowed for the LH5420's internal byte-shifting and demultiplexing circuits to settle; waiting for two full Port B clock cycles is recommended.

'SYNCHRONOUS' FIFOs AND 'ASYNCHRONOUS' FIFOs

The antonyms 'synchronous' and 'asynchronous' each have taken on two very different meanings in FIFO applications literature. The first meaning has to do with the timing of the FIFO's data and control inputs, and of its data and status outputs. The second meaning has to do with the capability of the FIFO to adjust itself to different and unrelated timing requirements at each of its two ends.

According to the first meaning of these terms, a 'synchronous' FIFO operates with a free-running clock input, but performs operations such as writing or reading only when these operations are 'enabled.' Data inputs, and control inputs such as enable signals and mode-control signals, must all meet setup time and hold time requirements with respect to the free-running clock. Data outputs and status outputs are presumed valid after some specified delay time has elapsed, following a transition of the free-running clock.

FIFOs which are 'asynchronous,' according to this meaning of 'asynchronous,' do not use any such free-running clock. Some older-architecture 'asynchronous' FIFOs even use edge-sensitive, rather than level-sensitive, control inputs. 'Synchronous' FIFOs sometimes may be made to behave as 'asynchronous' FIFOs, if desired, by connecting their 'enable' inputs to be permanently asserted, and using their free-running clock inputs as asynchronous edge-sensitive 'demand' control input signals.

According to the second meaning of the terms 'synchronous' and 'asynchronous,' however, a 'synchronous' FIFO would be a FIFO having both its input port and its output port always synchronized to the same 'clock' signal; in other words, a glorified shift register. An 'asynchronous' FIFO, on the other hand, can operate with its input port synchronized to one timing signal, and its output port synchronized to a second timing signal having no necessary relation to the first one; and neither timing signal needs to be regular or periodic.

The LH5420 has a free-running-clock-plus-enable control structure; and so its two internal FIFOs are 'synchronous' FIFOs in the first sense of this term, except that the behavior of the five relative-fullness flags is not entirely 'synchronous.' However, they are completely 'asynchronous' FIFOs in the second sense; there is no necessary synchronization relation between the Port A clock and the Port B clock, nor is either of these clocks required to be strictly periodic. This type of behavior is usually considered to be useful, system-friendly, and what FIFOs are all about.

DESIGNING WITH THE LH5420

In some applications, data bursts get pushed through a FIFO at or close to the FIFO's maximum word rate; but the system must take some immediate action if the FIFO ever becomes completely full or completely empty. The LH5420's Request/Acknowledge feature supports such a mode of operation. The Acknowledge output signal meets the setup time and hold time requirements for the Enable input, and may simply be tied back to it, in order to prevent complete filling or complete emptying of the active FIFO. This mode of operation slightly decreases the maximum data rate.

In essence, the Acknowledge signal is a synchronous 'proxy' or 'predictor' for whichever 'Almost' flag is pertinent to the current data-transfer operation. Because synchronous predictive logic is used to determine the state of this signal, it is actually faster than the corresponding flag.

Assume now that a port's Request input is being continuously asserted, say for writing into the outbound FIFO for that port. As long as the FIFO does not get into the 'Almost-Full' region, that is, the number of vacant FIFO physical words never falls below the 'Almost-Full' offset value, then the Acknowledge output is continuously asserted by the LH5420 control logic, and a word gets written into the FIFO as a result of every write-clock pulse. However, if the FIFO does become 'Almost Full,' then the Acknowledge output gets asserted only on every *third* write-clock pulse, rather than continuously. Thus, if the Acknowledge output has been tied back to the Enable input, the wide-open data rate then gets slowed down immediately, so that the writing of each word can be handled on a full-handshake basis. This operational technique allows achieving the maximum data rate much of the time, and yet protects the system against data loss caused by overrunning the FIFO boundaries.

When the system is operating an LH5420 in block-transfer mode, where a full block gets loaded at one port and then gets unloaded at the other port, the Acknowledge signals may be used to locate the end of a block, in lieu of having to implement an external block-length counter. As a simple example, say that the system block length is 193 words. The sending port loads in one complete block, and 55 words from the next block, in burst mode. At this point, its Acknowledge signal gets deasserted, indicating that the FIFO is 'Almost Full.' The Acknowledge signal does behave exactly in this manner, provided that the corresponding 'Almost-Full' flag offset still remains at its default value of eight. The receiving port then unloads

the block. If its 'Almost-Empty' offset value has been set to 55, its Acknowledge signal will get deasserted exactly at the end of the block. Since this indication occurs within a clock period, it is fast enough to be accurate without any uncertainty.

The LH5420's parity-checking facilities treat all nine bits alike, of each byte passing through one of the two FIFOs; the 'parity bit' may be in any position within a byte. A ten-input parity gate scans each group of nine bits in the output register of each port; the tenth input of each parity gate is from the even/odd-parity control flipflop, which may be programmed from Port A. This flipflop is set for odd parity when the LH5420 is reset; but it may be reprogrammed to even, or back to odd, at any time subsequently. If any of the four parity gates at a port ever detects an odd number of 'ones' in a byte, *including* the control flipflop in the 'ones' count, then the port's parity flag is asserted as long as the word containing the erroneous byte remains in the output register.

SUMMARY

The LH5420 36-bit bidirectional synchronous FIFO, available now from Sharp, is a system-oriented 'one-chip-does-all' part, intended to simplify back-and- forth communications between two microprocessors, microcontrollers, or similar devices.

The LH5420 offers several sophisticated features: on-the-fly parity checking, word-width matching of a 36-bit bus to an 18-bit bus or to a 9-bit bus, two-way mailbox communications, and synchronous Acknowledge signals which can be used to give a quick and accurate end-of-block indication or an advance warning of FIFO fullness or emptiness.

In most bidirectional-FIFO applications, one LH5420 replaces many lower-level and discrete parts, and simplifies system design. It offers high performance for burst operations; it can transfer a 36-bit word in each direction every 25 nanoseconds.

* **COPYRIGHT INFORMATION:** This paper is a slightly modified version of the paper with the same title which appeared in the *Electro92 Conference Record*, paper 58/1; 11-14 May 1992.

FIFO MEMORIES: EFFECTIVE, COMPACT, AND EASY TO USE

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INTRODUCTION

FIFO memories ('FIFOs') are VLSI semiconductor memory devices which store information temporarily.

The word 'FIFO' is an 'acronym' in English. An acronym is a word formed from the first letters of other words, in this case 'First-In, First-Out.' This term was first used in the mathematical field of operations research to describe one particular 'queue discipline,' that is, priority rule for dealing with the members of some 'queue.' The other major possible queue discipline is 'Last-In, First-Out,' or 'LIFO.' The terms 'FIFO' and 'LIFO' also are used in the fields of cost accounting and inventory control, for the two major methods of assigning a current cost to an item which has been withdrawn from an inventory stock of items bought at varying times and at varying prices.

Data words may be pushed into a FIFO memory in sequence, one word at a time, without ever having to give the FIFO any 'address' to tell it exactly where to store a given word. Later on, the same sequence of data words may be pulled out of the FIFO at its other end, one word at a time, in the same order in which they entered the FIFO. Because the position of each word remains the same within the block of words, there is no need to 'address' the FIFO to tell it where a particular word is to be found.

Single-chip FIFO devices of several different word widths are available. The most common word width today is 9 bits. But there still are older FIFOs being sold with word widths of 4 or 5 or 8 bits, and newer FIFOs with word widths of 18 or even 36 bits. Sharp has been the first FIFO manufacturer to have brought 36-bit FIFOs to market.

FIFO memories are used for several diverse purposes in digital systems:

- Matching different data rates.
- Holding data temporarily, away from any main memory.
- Eliminating 'skew' between parallel data streams.
- Acquiring a time-sequential record of successive events.
- Reading out the same data over and over again repetitively.

Some uses of FIFOs perhaps may serve more than one of these purposes.

MATCHING DIFFERENT DATA RATES

Data-rate matching probably is the most common type of FIFO application. There are three common patterns for the timing of a stream of data words. The data words may arrive and/or depart

- at RANDOM times, individually.
- in BURSTS, that is, in blocks of some given number of words.
- at a CONSTANT rate.

A FIFO may be used to hold input-data-stream words, which are arriving according to any of the above timing patterns, for a variable and controllable duration, so that they depart according to the timing pattern needed for output-data-stream words. On the average and over the long term, however, exactly as many words must depart from the FIFO as previously arrived – no more, and no less. Otherwise, either the FIFO memory would become permanently full, or else it would become permanently empty.

Since there are three timing patterns for the arrival of data words, and also the same three timing patterns for their departure, there are nine possible timing patterns in all for a FIFO's complete data-transfer task. Probably the four most important of these are 'random-to-random,' 'burst-to-burst,' 'burst-to-constant,' and 'constant-to-burst.'

The 'random-to-random' case is referred to as the 'single-server-problem' in operations-research mathematics, where it is often described using the illustration of hungry customers arriving at a hamburger stand at random intervals, and departing with their hamburgers at different random intervals.

Often some electromechanical peripheral device is connected to one end of a FIFO, while a purely electronic device is connected to the other end. Electromechanical devices usually must acquire or emit data at fixed times, which are a function of their own design; their timing can't be rearranged on command by an electronic system. On the other hand, most all-electronic devices are much

more able to adjust their data-transfer timing to the needs of other devices with which they are communicating, although there are some major exceptions.

Even all-electronic devices may have their operating efficiency badly degraded, if they are subjected to constant 'overhead' interruptions by electromechanical devices. Thus, FIFOs often perform in the useful role of isolating all-electronic devices such as microprocessors from common electromechanical devices such as disk memories, laser and ink-jet printers, and bar-code readers.

As mentioned, there are some important all-electronic devices, without any moving parts, with timing characteristics just as inflexible as those of electromechanical devices. Many kinds of computer-graphic displays must be refreshed or changed at some predetermined rate. A telephone-line network or a local-area network likewise has an established data-transfer frequency, to which any external device connected to the network must adapt itself, often via a FIFO.

Also, industry-standard databus specifications restrict the timing allowed for many signals, so as to ensure reliable communications interfacing between hardware modules designed independently by different groups of people.

Most newer FIFO memory devices provide built-in status outputs, called 'flags,' which help the system's controlling logic implement efficient FIFO-memory operating strategies. Typically, there are five of these flags: 'Full,' 'Almost-Full,' 'Half-Full,' 'Almost-Empty,' and 'Empty.' The 'Almost' flags may be used as advance warnings to the system that some action must be taken soon. For, once the FIFO memory has reached the 'Full' condition or the 'Empty' condition, it may already be too late to avoid losing or scrambling data.

One simple but effective control strategy, for 'burst-to-burst' FIFO operation, is to select a FIFO memory having a depth of twice as many words as the usual system datablock size. A new block of data is brought in whenever the 'Half-Full' flag indicates that the memory is now less than half full, thus making efficient use of the FIFO's memory capacity.

There also are some more sophisticated strategies, which use the 'Almost' flags as well. In many FIFO devices, the 'offset' values for these 'Almost' flags are 'programmable.' This 'offset' value is a specification by the system of the number of FIFO-memory words by which 'Almost-Full' is to differ from 'Full,' and may be changed by the system during operation; likewise for 'Almost-Empty' and 'Empty.'

Occasionally there is a 'constant-to-constant' FIFO application. Here, the FIFO has to serve as a pure time-delay element, and the data rates at both ends of the FIFO must be exactly the same.

HOLDING DATA TEMPORARILY, AWAY FROM ANY MAIN MEMORY

The information-storage capacity of FIFO memories usually is smaller than that of random-access memories ('RAMs'). Nevertheless, today's FIFO memories are large enough to fulfill many needs for 'local' storage at various points in a system remote from any 'main memory.'

FIFOs don't require that the system create or monitor any 'addresses' for the information stored within them. Whatever goes in one end simply comes out the other end, in the same order. Thus, FIFOs provide a convenient form of 'data storage at a point.' In some cases, what is being stored is control information, such as commands or instructions; it is not necessarily always 'data.'

One other unique and valuable property of FIFOs is that, within one given 'family' of architecturally-compatible FIFO parts, FIFOs having different sizes of internal memory are DIRECTLY 'drop-in-compatible' with each other without ANY system redesign. Thus, a 'deeper' FIFO, having more memory-word capacity, often is used to replace a smaller or 'shallower' FIFO, which may have turned out not to have enough memory-word capacity for the application.

Sometimes, the need to replace smaller FIFOs with larger FIFOs may come about because of a deliberate system-engineering strategy, of upgrading the performance of a microprocessor-based system design by increasing the system datablock size. With larger datablocks, the microprocessor does not need to be interrupted as often in order to deal with FIFO data, and can be focused more efficiently on its main tasks.

ELIMINATING SKEW BETWEEN PARALLEL DATA STREAMS

Parallel data streams which are supposed to be mutually synchronized, but which get out of synchronization by varying amounts, are said to be 'skewed' with respect to one another. An interesting specialized FIFO application is that of 'deskewing' the individual bits read from the parallel bit-recording longitudinal data 'tracks' of a multiple-channel magnetic tape. The magnetic-tape skew problem arises primarily because a particular tape may first have been recorded on one physical tape drive, and later on moved to a different physical tape drive for reading. Similar applications arise when dealing with other not-too-precise synchronous devices.

The solution to this design problem, in its usual form, requires one FIFO memory device per magnetic-tape longitudinal data track. The FIFO devices are operated at a repetition rate which is much higher than the databits-per-unit-time rate for each magnetic-tape track. Using an algorithm which depends on the magnetic recording format in use, the system must continuously determine the current phase timing for each track, and then must advance or hold back the unloading of each FIFO to keep all of the FIFO outputs in phase together.

ACQUIRING A TIME-SEQUENTIAL RECORD OF SUCCESSIVE EVENTS

A FIFO, with its data inputs connected to some 'interesting' system point, can serve as an 'event recorder.' In such applications, the FIFO's 'Write Clock' or 'Shift-In Strobe' (or other signal which tells the FIFO when it is to write in a new data word) is controlled by system logic, which decides WHEN the information at that system point is 'interesting' and hence should be captured by writing it into the FIFO.

One 'event-recording' application for FIFOs is that of serving as the data-capture memory within a logic analyzer or a medical ultrasound scanner. A characteristic feature of such instrumentation applications for FIFOs is that the very same data, once captured, must be read out over and over again. Many FIFO devices have a 'Retransmit' facility which allows doing so.

A similar application, within a processor, is that of a 'jump-trace memory.' The FIFO's data inputs are connected to the processor's 'program counter' or 'microprogram counter' (or other control-sequencing register), and a FIFO input word is recorded every time that a jump out of the normal incremental program-step-addressing sequence occurs. Such a 'jump-trace memory' feature can be very helpful when debugging real-time operating systems; if the system crashes, having a 'trace' record of the last few dozen jump addresses can be very valuable in analyzing the cause of the crash, since in real-time applications there usually isn't any way to repeat the exact sequence of events which led up to the crash.

Another processor application for FIFOs is the queueing of 'interrupts,' which are high-speed requests for the processor's attention. In certain types of systems, such as digital-telephony processors, the number of real-time interrupts is extremely high; but a delay of a few milliseconds is permissible when responding to each of them. A useful technical approach in such cases is to form an encoded interrupt-information word by hardware means, for each interrupt as it is received, and store these interrupt-information words in time-sequenced order within a FIFO, to be unloaded and dealt with whenever the processor has the free time to do so.

READING OUT THE SAME DATA OVER AND OVER AGAIN REPETITIVELY

When implementing reliable data-communications hardware which must use an unreliable communications channel, it is customary for the receiving device to transmit an 'acknowledge' signal back to the sending device to indicate that the last datablock was received, and that it appeared to be correct. If no such 'acknowledge' signal gets received by the sending device, or if – worse yet! – a 'negative-acknowledge' signal gets received instead, then the sending device must transmit the erroneously-received datablock another time. A FIFO with a 'Retransmit' facility, as described above, is a convenient means of implementing this capability within the sending device.

A waveform generator is a laboratory instrument which can produce a repetitive waveform of any desired shape or frequency, up to its performance limits. Some waveform generators use digital electronics; the heart of one of these may be a large-but-slow read-only memory, which holds an extensive library of waveforms expressed as successive digital sample values, plus a FIFO. The FIFO loads up the desired waveform once, at the read-only memory's slow speed; then it reads out the waveform over and over again, using its 'Retransmit' facility, often at a much higher speed.

IN CONCLUSION

Once, FIFOs were rather high-priced as compared to other digital semiconductor components. Now, competition and manufacturing improvements have reduced the price of FIFOs substantially. Today, more than ever, FIFOs should be considered for many applications for which they have always offered a superior design approach, but for which they have been considered too expensive. If your application can be described as 'data-rate matching,' 'local memory,' 'skew elimination,' 'sequential event recording,' or 'repetitive readout,' a FIFO is your best answer.

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PACKAGE SELECTIONS: STATIC RAMs

PRODUCT	PIN COUNT (NOMINAL DIMENSIONS)																		
	DIP						SDIP		SOJ				SOP			TSOP			PLCC
	24 (300)	24 (600)	28 (300)	28 (600)	32 (400)	32 (600)	24 (300)	28 (300)	24 (300)	28 (300)	28 (400)	32 (400)	24 (450)	28 (450)	32 (525)	28[1] (0813)	32[2] (400)	32[1] (820)	52 (750)
PSEUDO STATIC RAMs																			
LH5P832				X				X						X					
LH5P8129						X									X			X	
LH5P8128						X									X			X	
LH5P8512						X									X		X		
STATIC RAMs																			
LH5116/H		X					X						X						
LH5116S													X						
LH5118/H		X					X						X						
LH5168/H				X				X						X		X			
LH5168SH														X					
LH51256L				X										X					
LH511000UL						X									X			X	
LH52250AL			X	X										X					
LH52256LL				X										X					
LH52252A	X								X										
LH52252B	X								X										
LH52253			X							X									
LH52258			X							X									
LH52258A			X							X									
LH52258B			X							X									
LH521002											X								
LH521007					X							X							
LH521008					X							X							
LH521028																			X

1. TSOP(I)
2. TSOP(II) – Consult factory for availability.

PACKAGE SELECTIONS: MASK-PROGRAMMABLE ROMs

PRODUCT	PIN COUNT (NOMINAL DIMENSIONS)												
	DIP				SDIP	SOP				QFP			TSOP
	28 (600)	32 (600)	40 (600)	42 (600)	64 (750)	28 (450)	32 (525)	40 (525)	44 (600)	44 (1010)	44 (1414)	64 (1420)	48[1] (1218)
MASK-PROGRAMMABLE ROMs													
LH53259	X					X				X			
LH53515	X					X	X			X			
LH53H1000			X					X					
LH53H0900		X					X						
LH530800A		X					X			X			
LH531000B	X					X							
LH532000B			X					X		X	X		X
LH532100B		X					X						
LH534000B			X					X		X	X		X
LH534100B		X					X						
LH534500A			X					X			X		X
LH534600			X					X			X		
LH538000				X					X			X	X
LH538100		X					X						
LH538500A				X					X			X	X
LH5316000					X							X	
LH5316500				X					X			X	X
LH5332000									X			X	

1. TSOP(I)

PACKAGE SELECTIONS: FIFO MEMORIES

PRODUCT	PIN COUNT (NOMINAL DIMENSIONS)							
	DIP		SOJ	PLCC			PQFP	PGA
	28 (300)	28 (600)	28 (300)	28 (450)	32 (450)	68 (950)	132 (950)	120 (1360)
FIFO MEMORIES								
LH5481/91	X			X				
LH5496	X	X			X			
LH5497	X	X			X			
LH5498	X	X			X			
LH5499		X			X			
LH5492					X			
LH5493					X			
LH5494					X			
LH5420							X	X
LH540201/02	X [1]	X	X		X			
LH540203	X [1]	X	X		X			
LH540204	X [1]	X	X		X			
LH540205	X [1]	X						
LH540206	X	X						
LH540215/25						X		
LH543620							X	X

1. Wide Body

PACKAGING NOMENCLATURE

DIP – Dual-In-line-Package

- SKDIP – Skinny DIP (.300 inch body width)
- SDIP – Shrink DIP (.070 inch lead pitch)
- CERDIP – Ceramic DIP

SOP – Small Outline Package

- TSOP – Thin SOP

SOJ – Small Outline J-Leaded Package

ZIP – Zigzag In-line Package

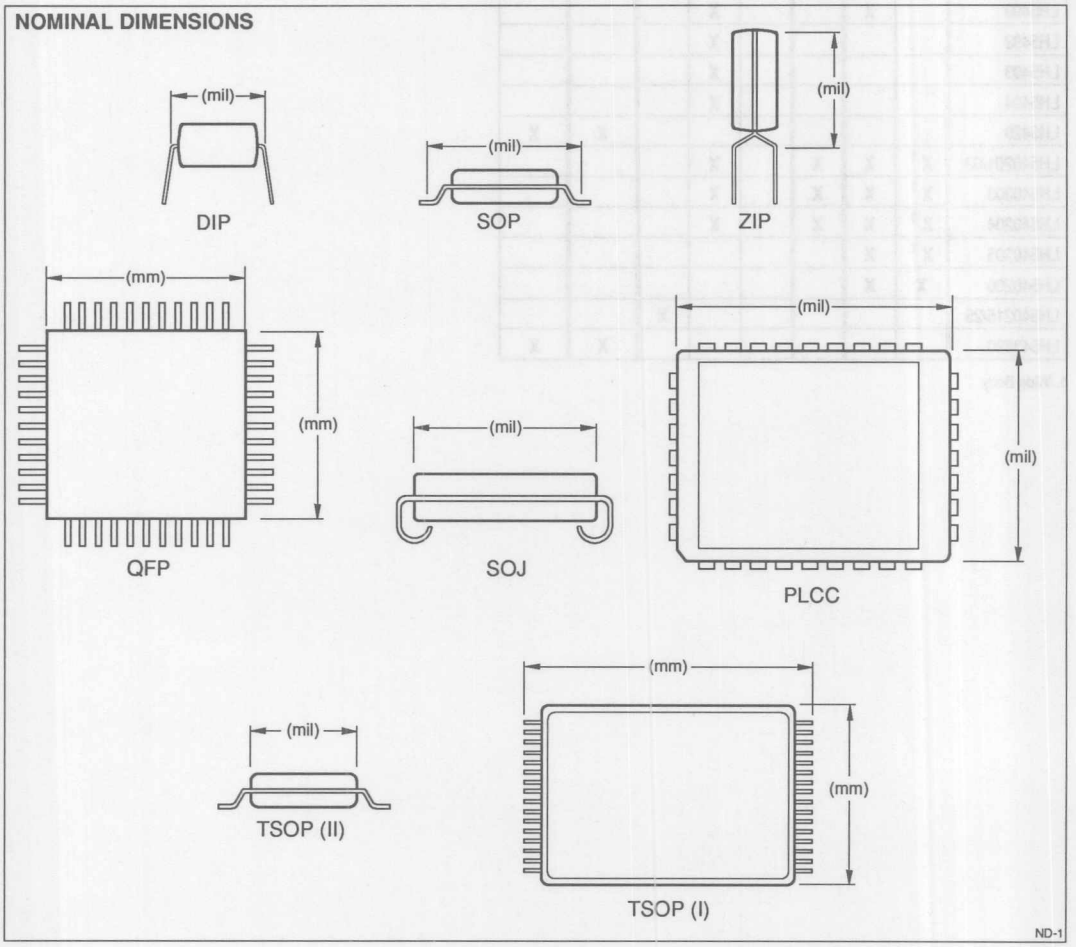
QFP – Quad Flat Package (Metric Standard)

- PQFP – Plastic QFP (JEDEC Bumpered Standard)

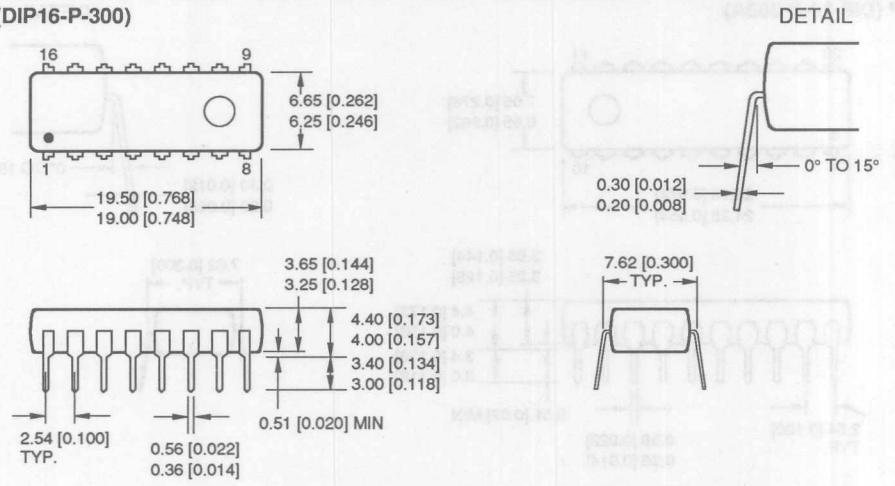
PLCC – Plastic Leaded Chip Carrier

PGA – Pin Grid Array

NOMINAL DIMENSIONS



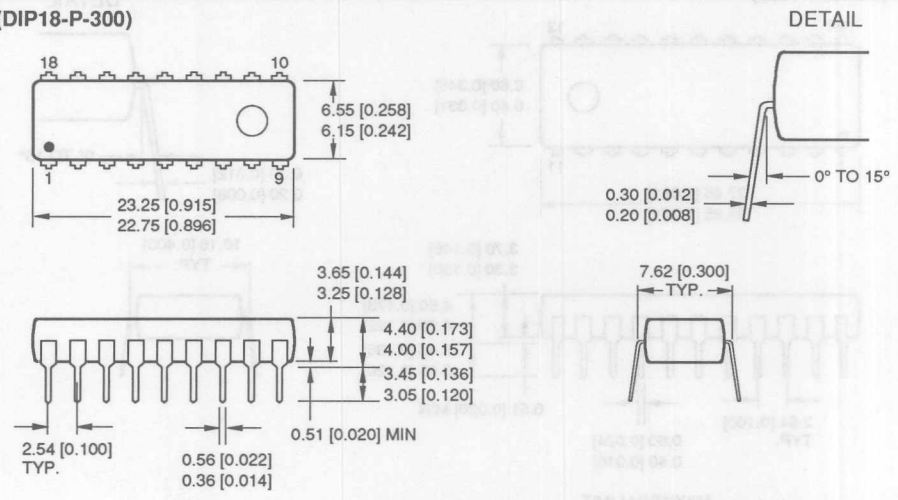
16DIP (DIP16-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

16DIP

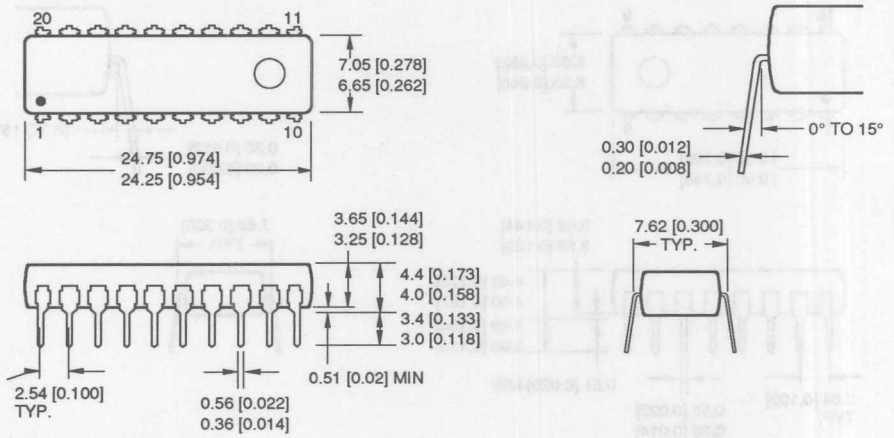
18DIP (DIP18-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

18DIP

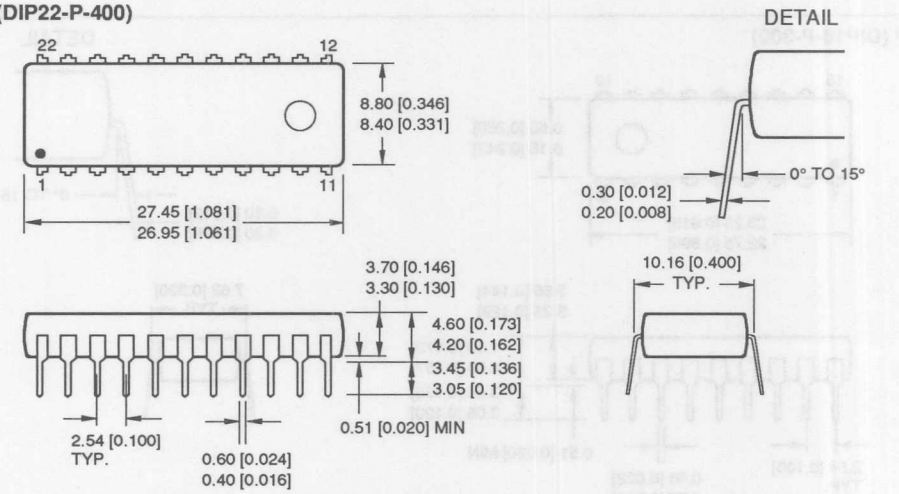
20DIP (DIP-20-P-300A)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

20DIP-2

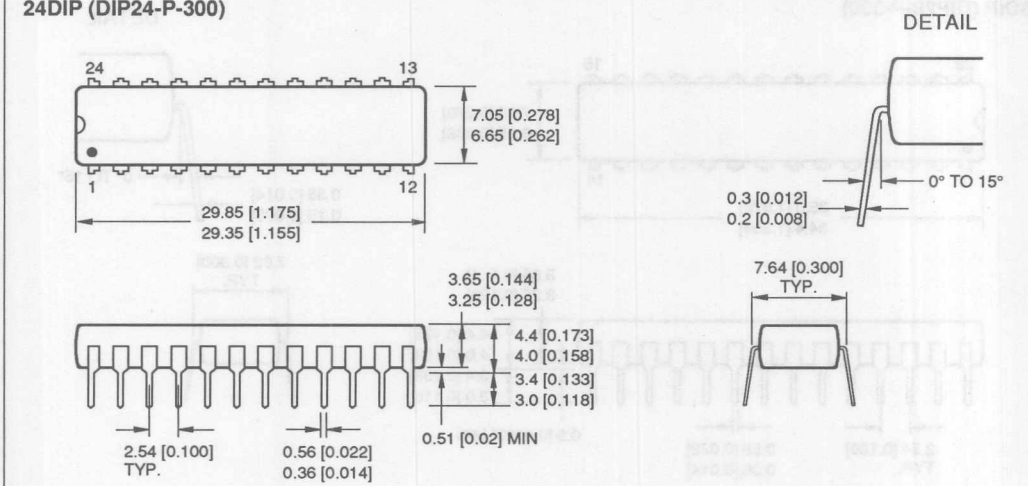
22DIP (DIP22-P-400)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

22DIP-2

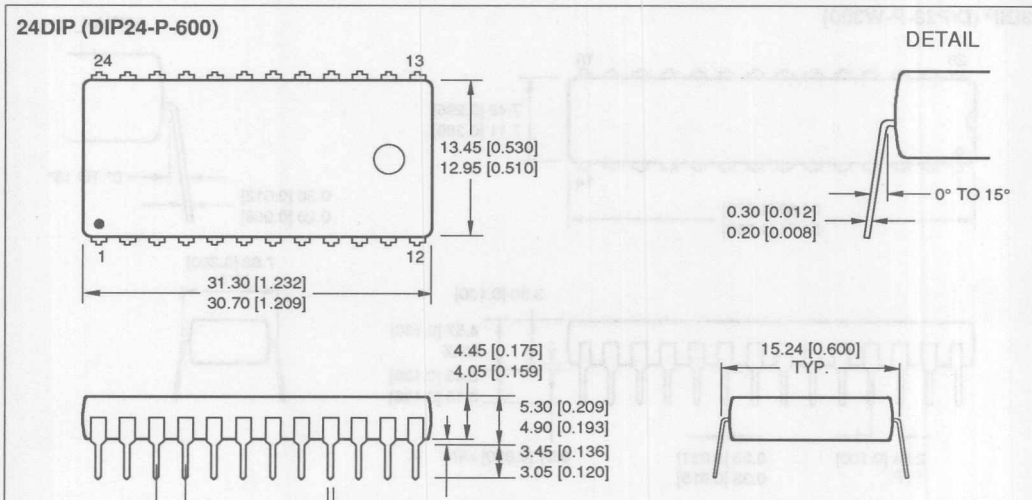
24DIP (DIP24-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24DIP-1

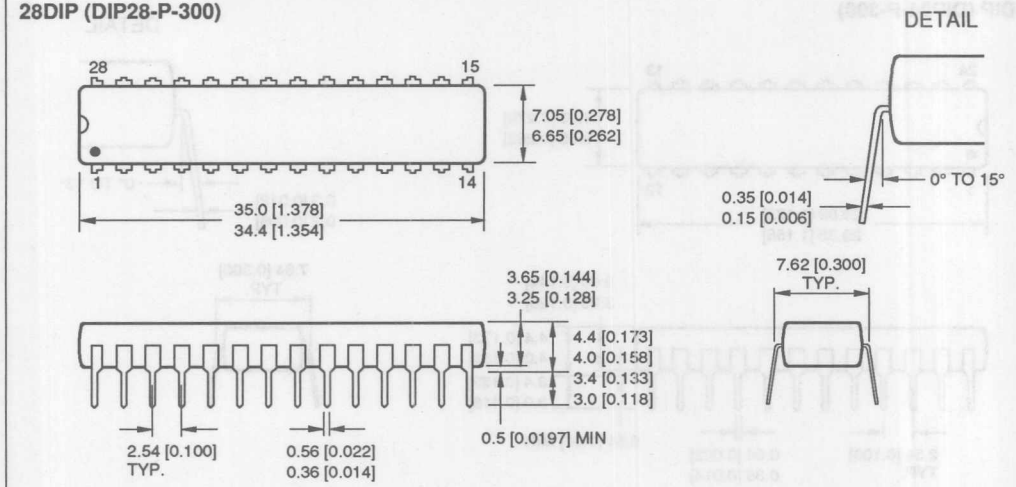
24DIP (DIP24-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24DIP-2

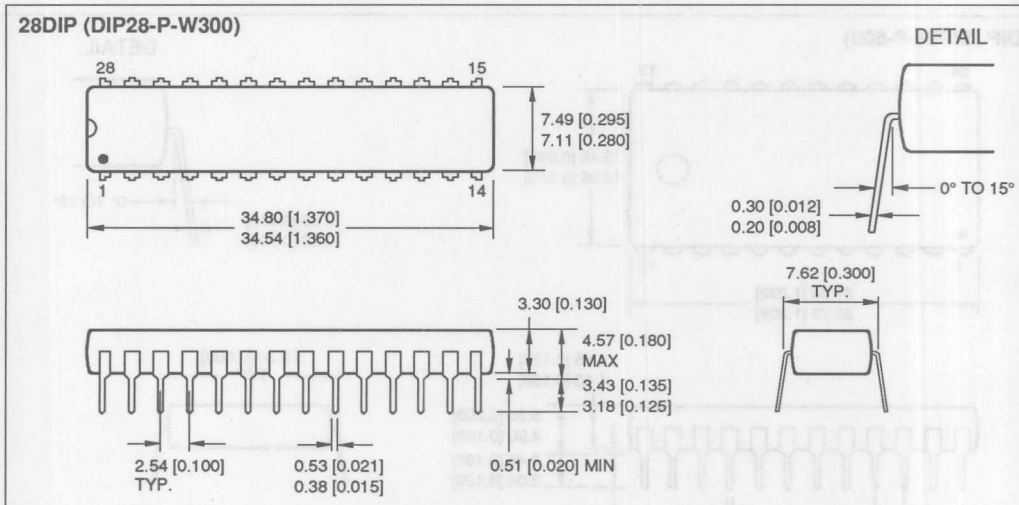
28DIP (DIP28-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-1

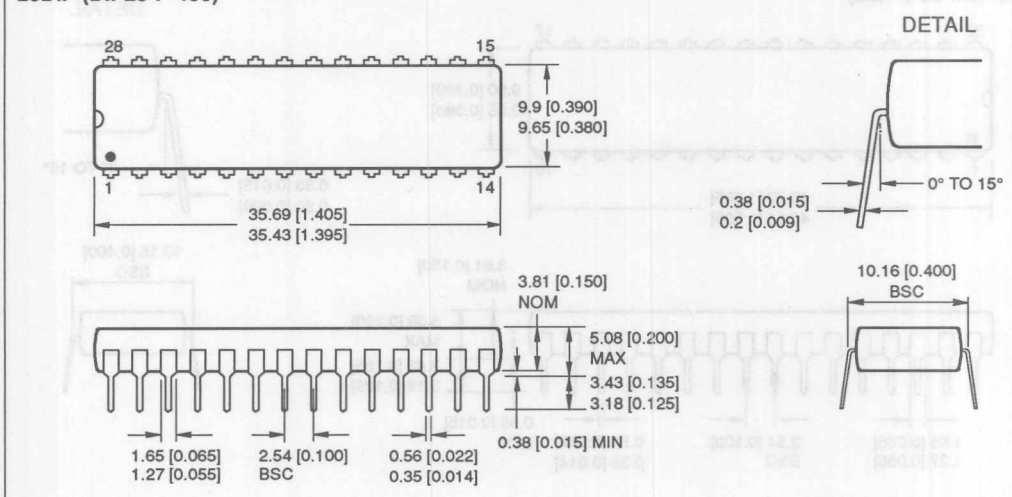
28DIP (DIP28-P-W300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-5

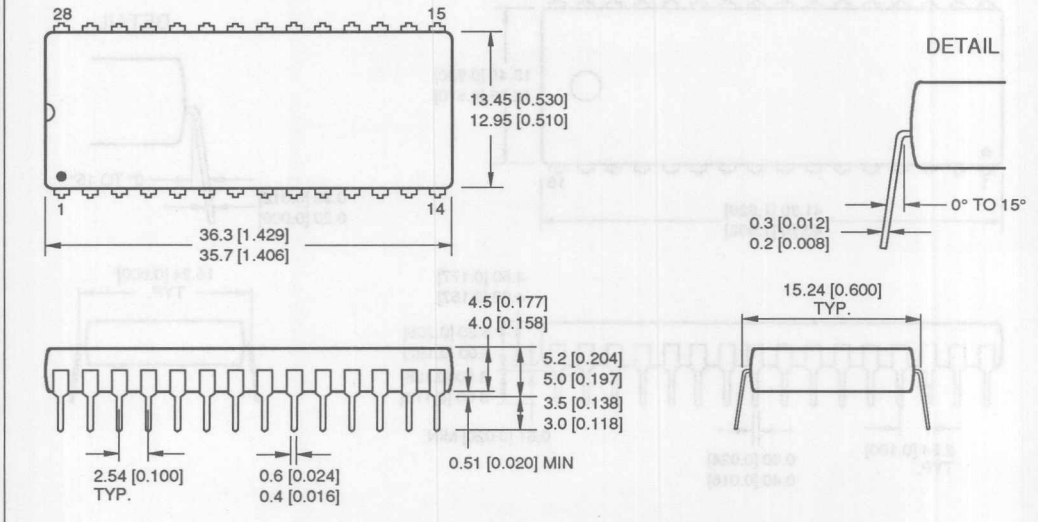
28DIP (DIP28-P-400)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-4

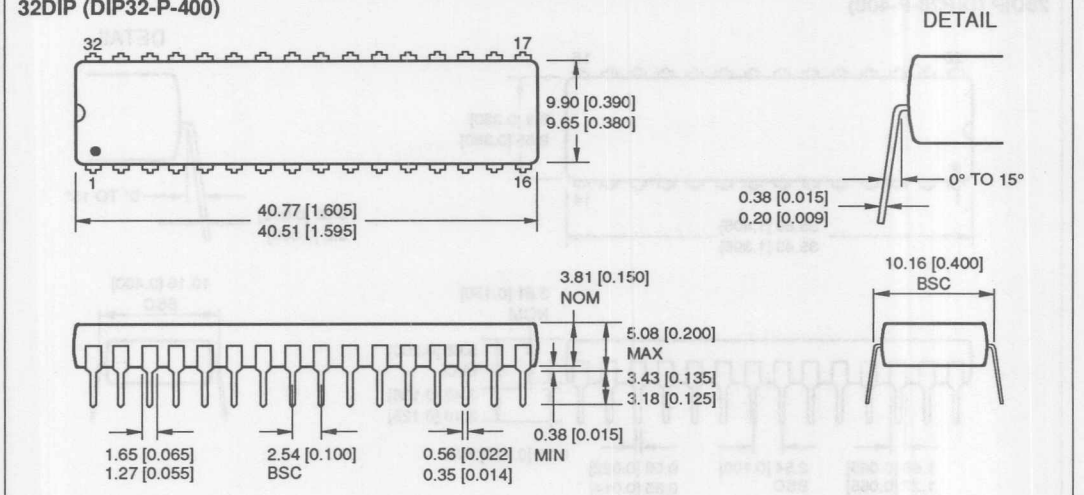
28DIP (DIP28-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28DIP-2

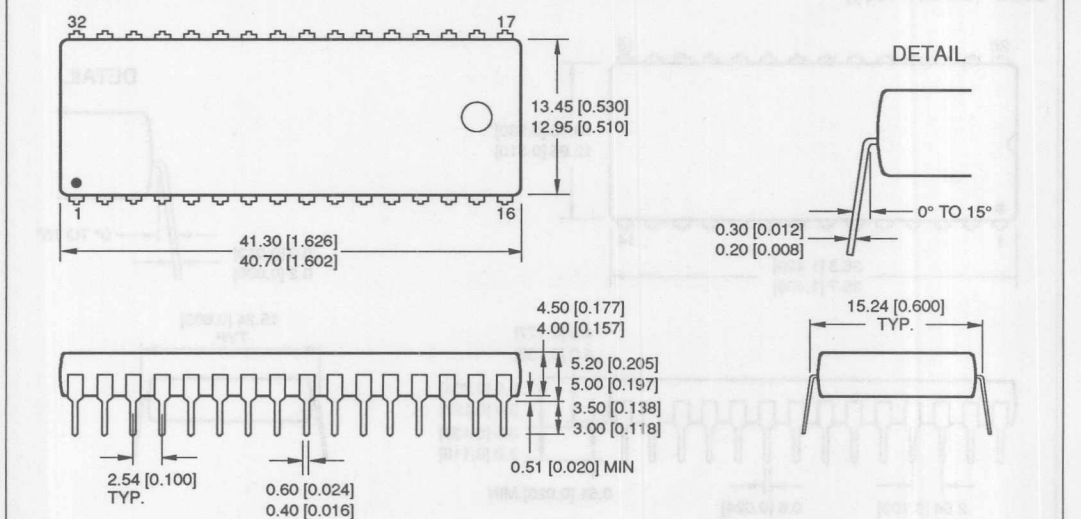
32DIP (DIP32-P-400)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32DIP-1

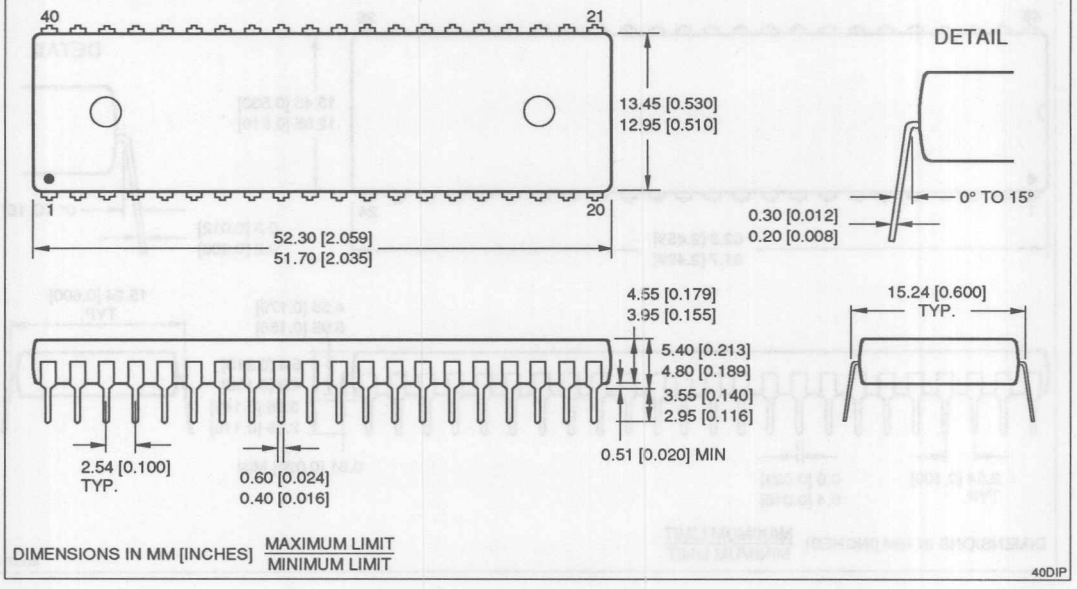
32DIP (DIP32-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32DIP

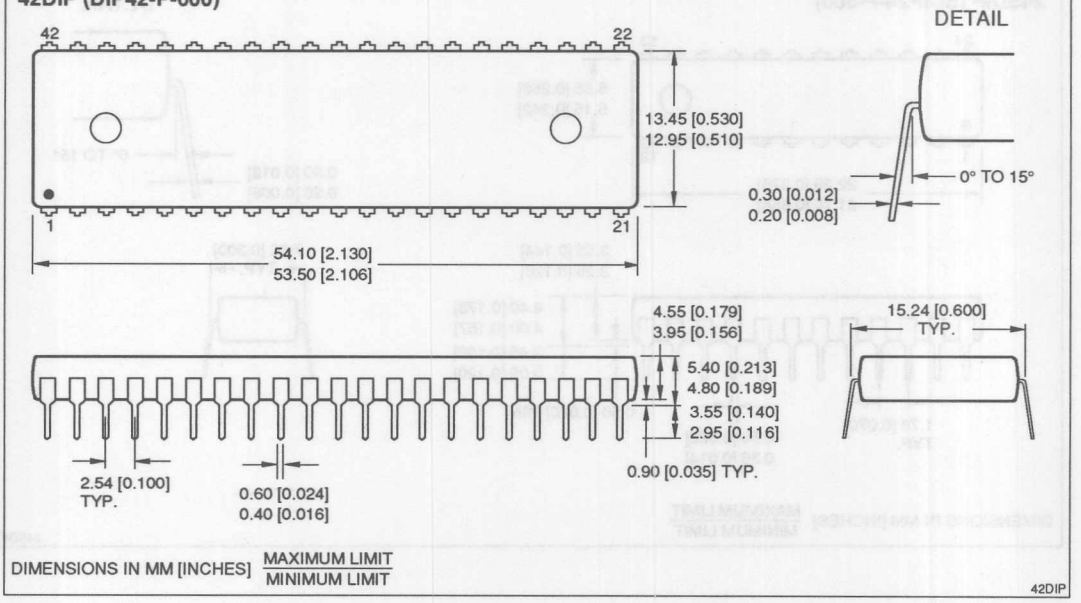
40DIP (DIP40-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

40DIP

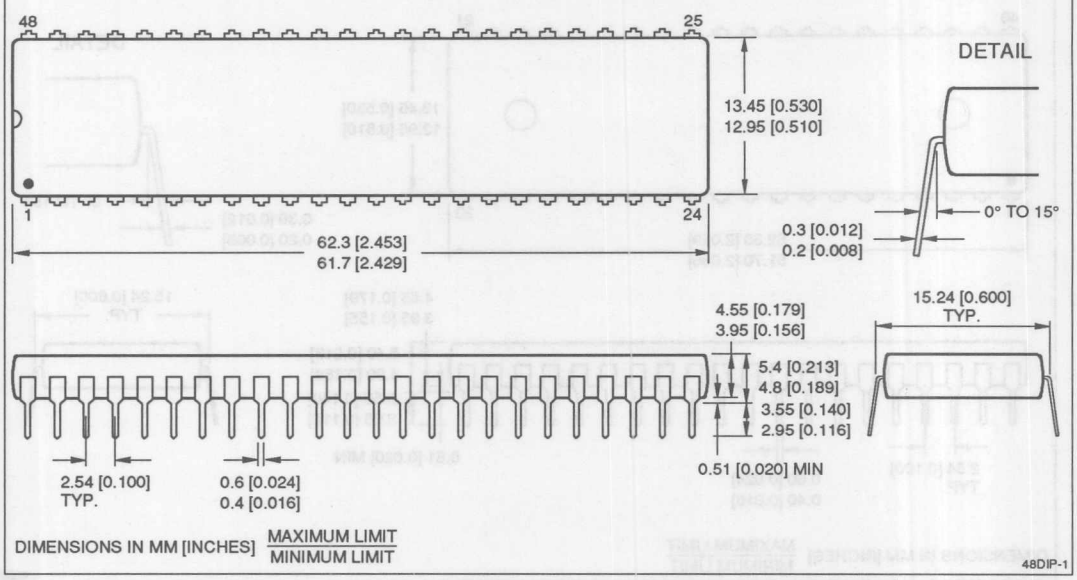
42DIP (DIP42-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

42DIP

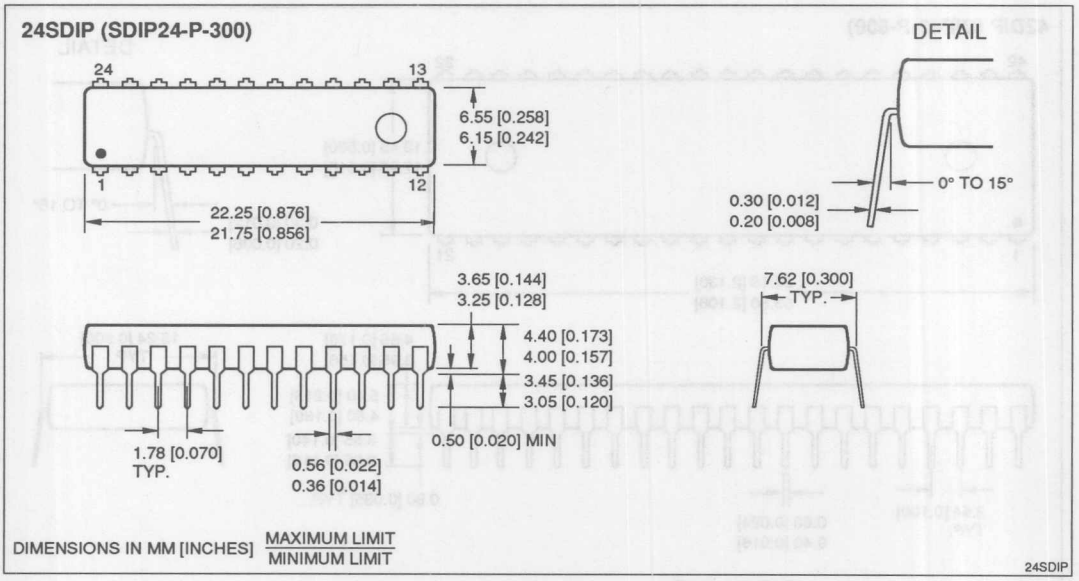
48DIP (DIP16-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

48DIP-1

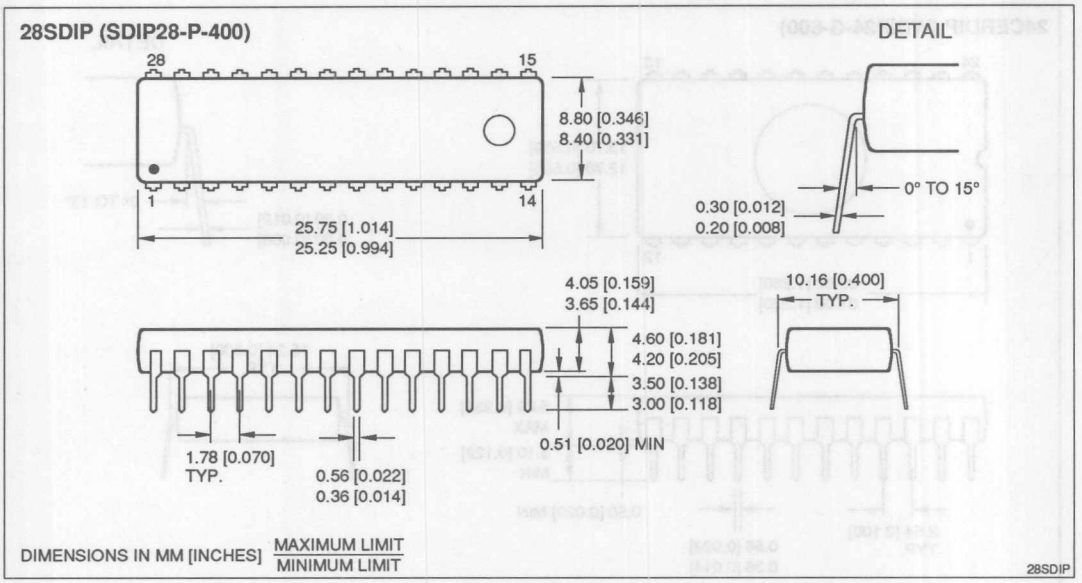
24SDIP (SDIP24-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24SDIP

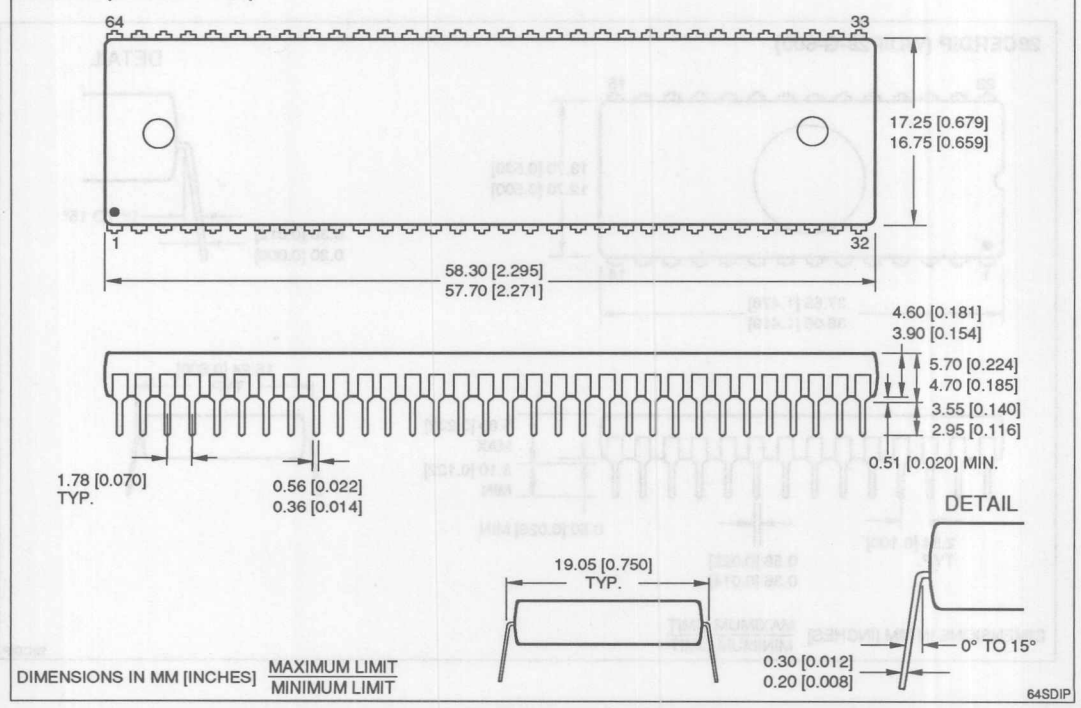
28SDIP (SDIP28-P-400)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SDIP

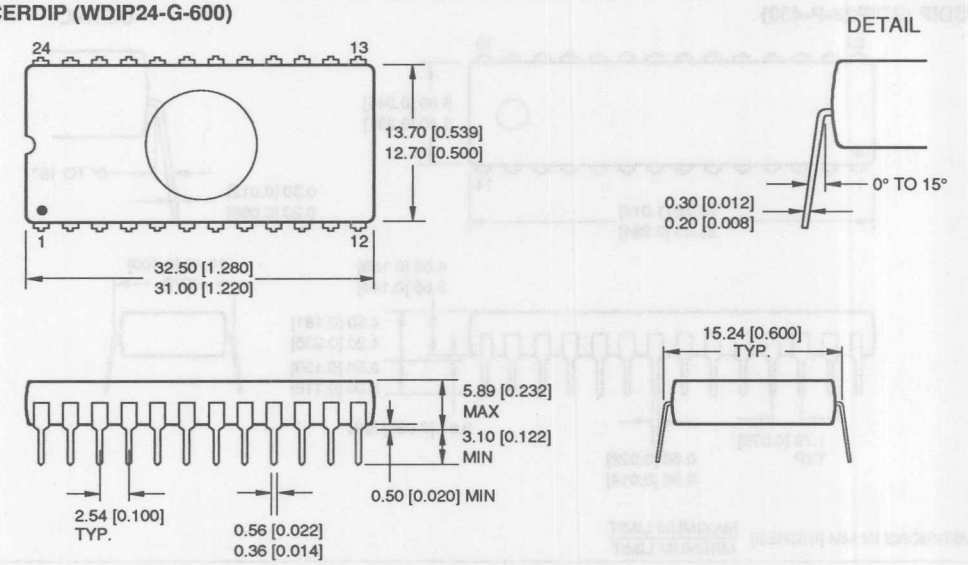
64SDIP (SDIP64-P-750)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

64SDIP

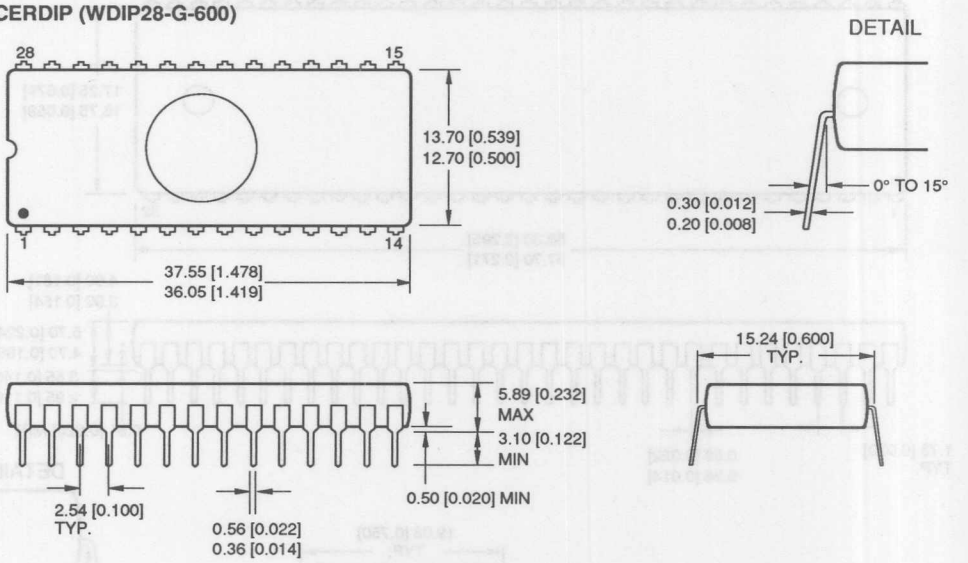
24CERDIP (WDIP24-G-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24CDIP

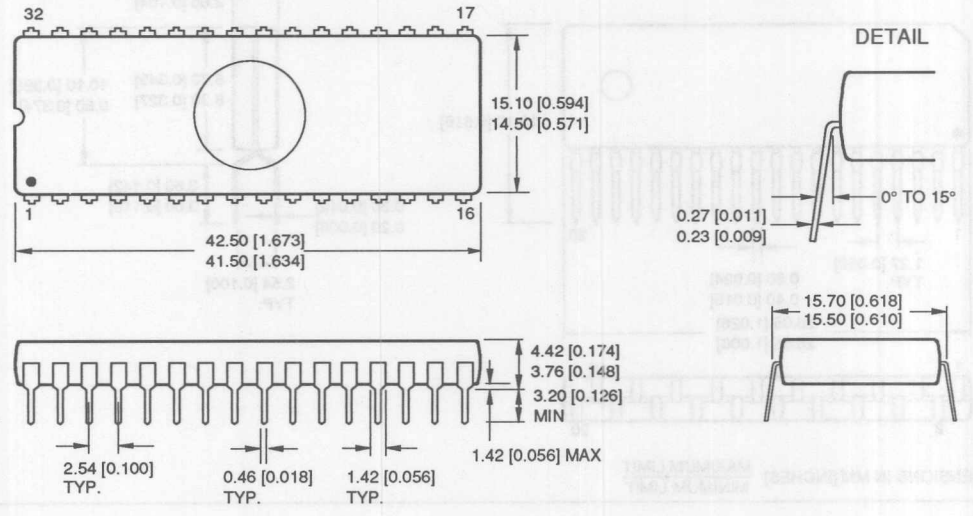
28CERDIP (WDIP28-G-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28CDIP

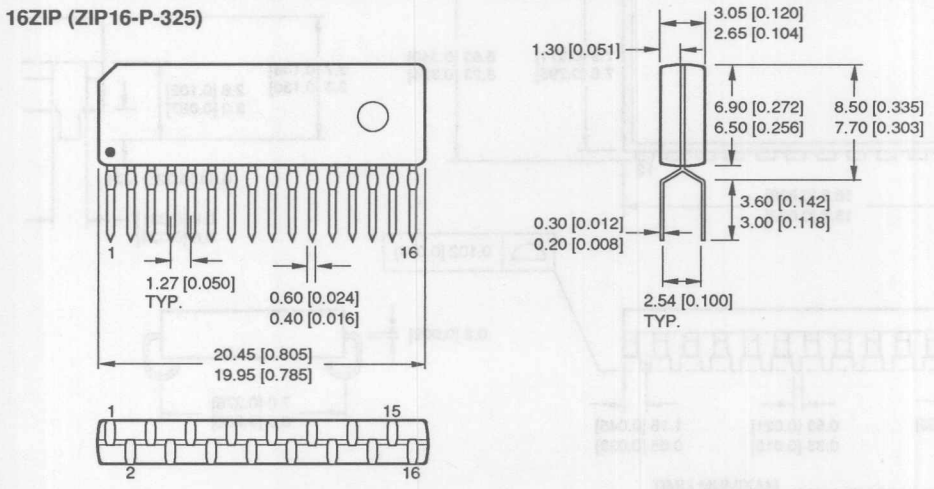
32CERDIP (WDIP32-G-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32CDIP

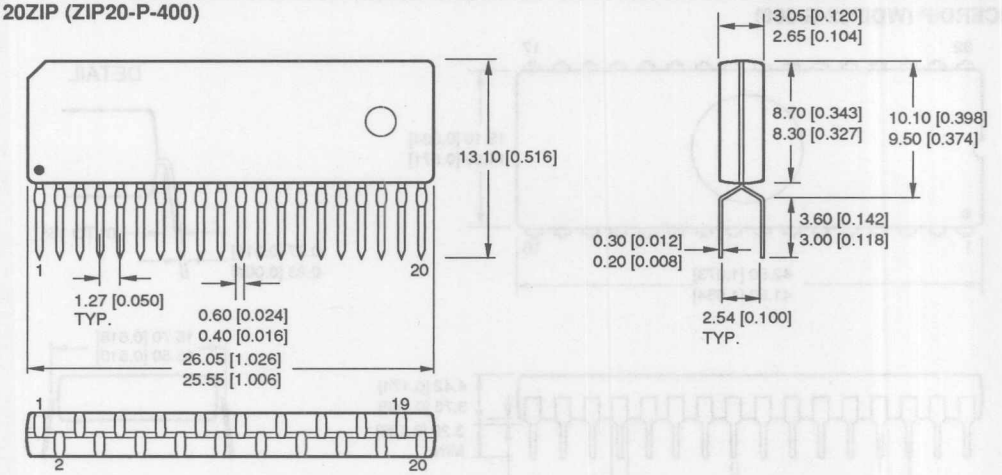
16ZIP (ZIP16-P-325)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

16ZIP

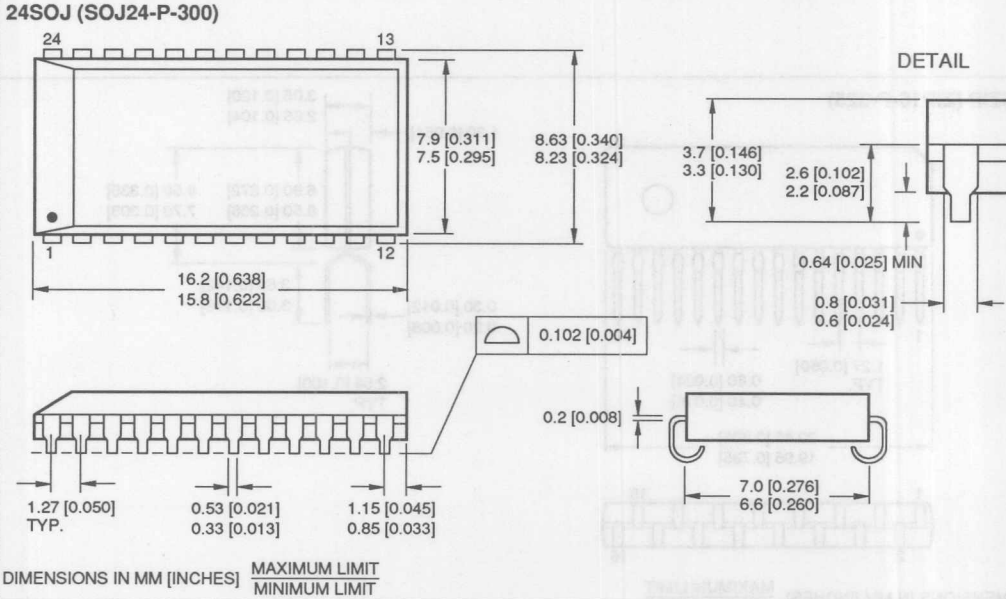
20ZIP (ZIP20-P-400)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

20ZIP

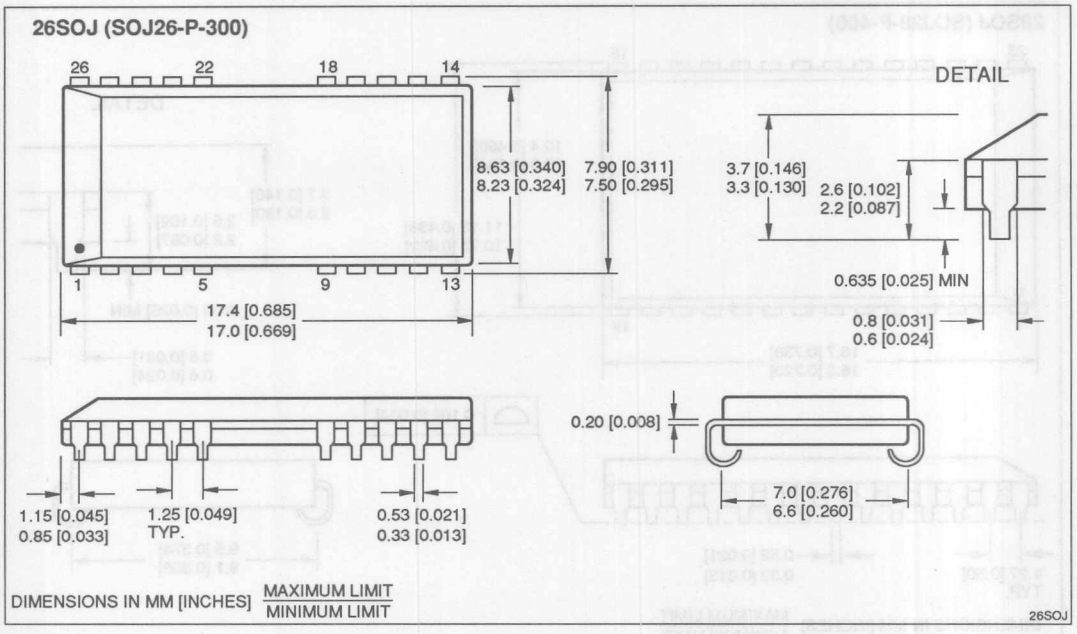
24SOJ (SOJ24-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24SOJ

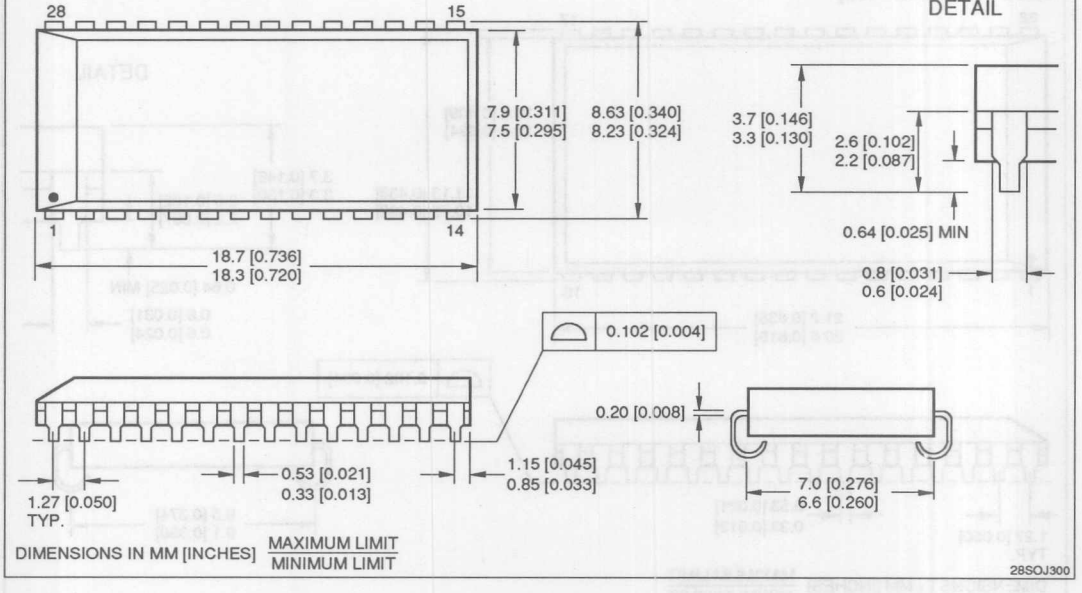
26SOJ (SOJ26-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

26SOJ

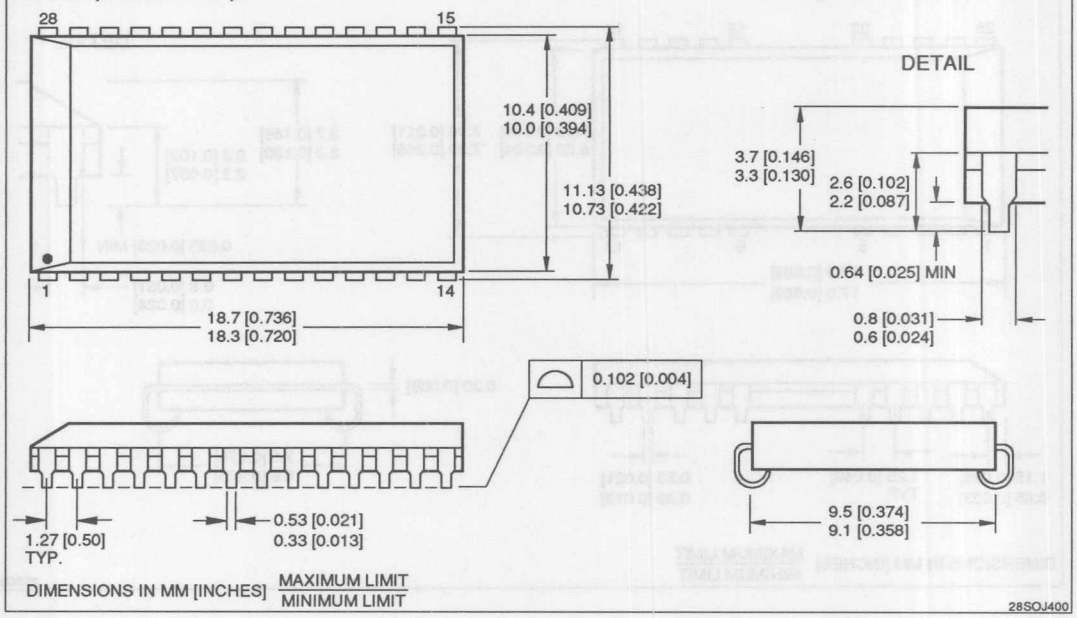
28SOJ (SOJ28-P-300)



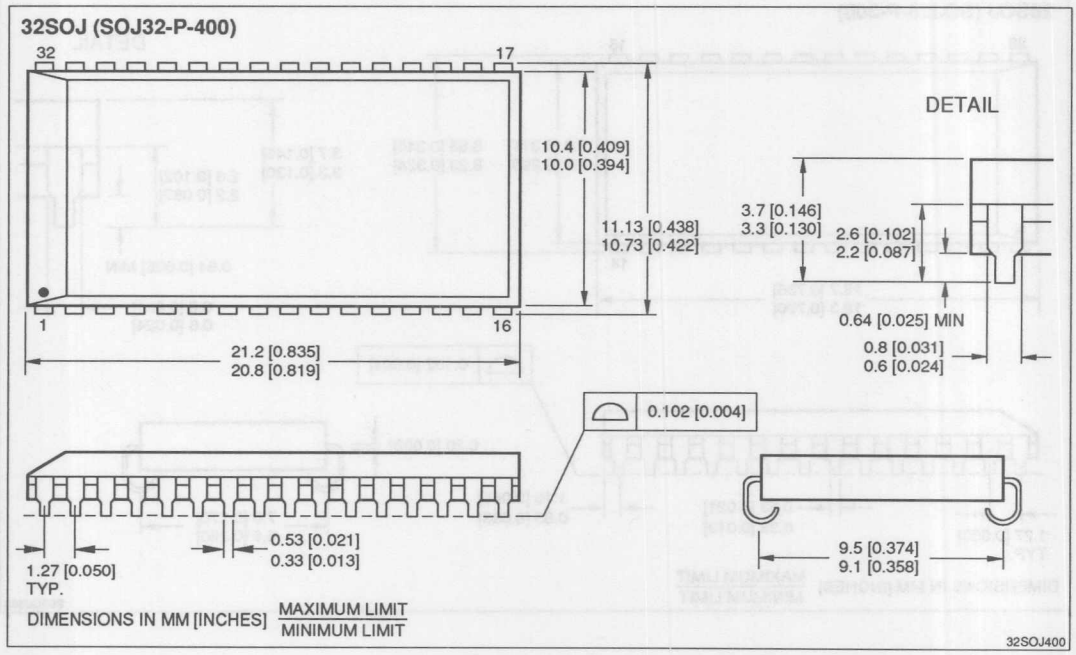
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SOJ300

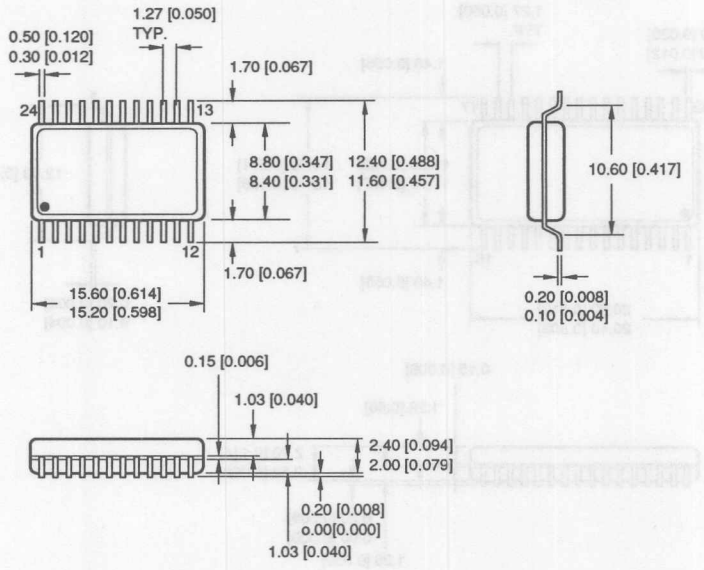
28SOJ (SOJ28-P-400)



32SOJ (SOJ32-P-400)



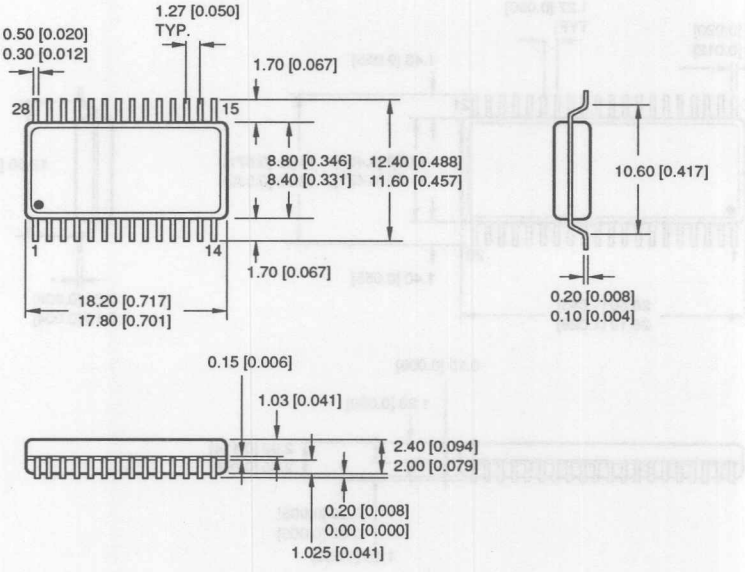
24SOP (SOP24-P-450)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

24SOP

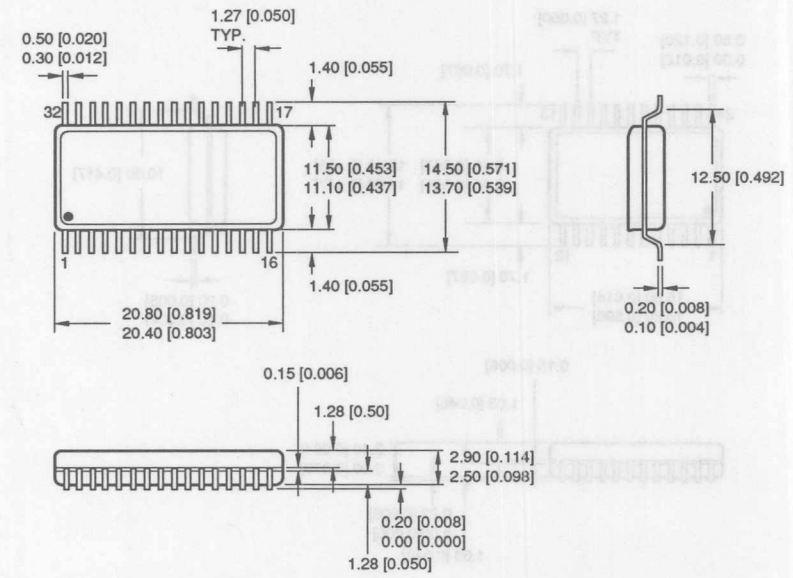
28SOP (SOP28-P-450)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28SOP

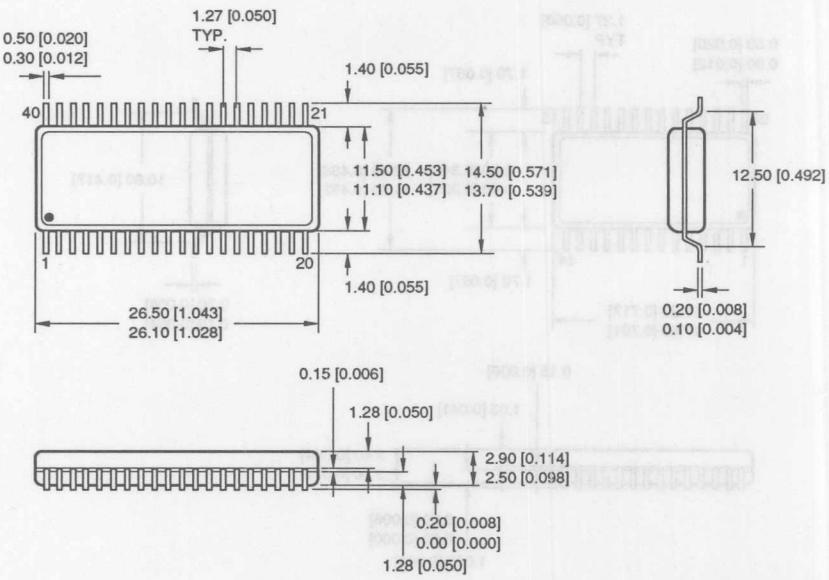
32SOP (SOP32-P-525)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32SOP

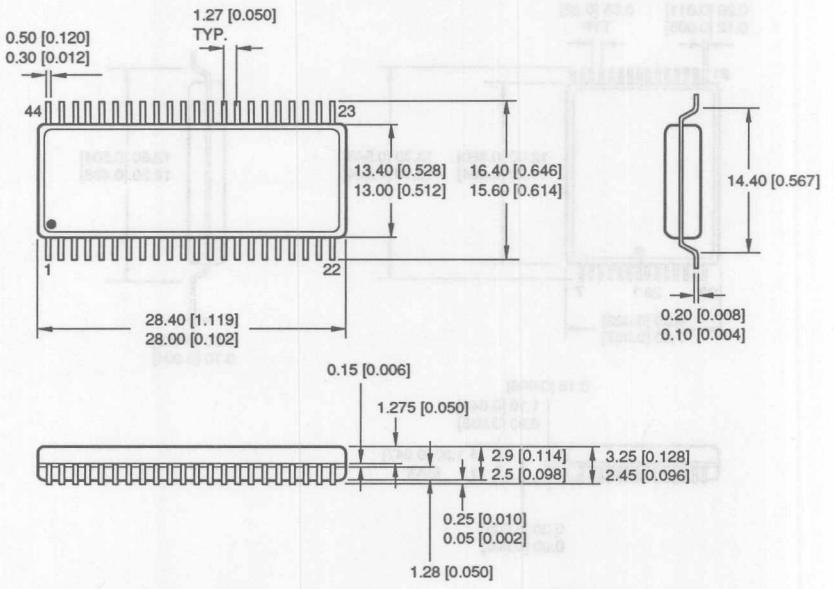
40SOP (SOP40-P-525)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

40SOP

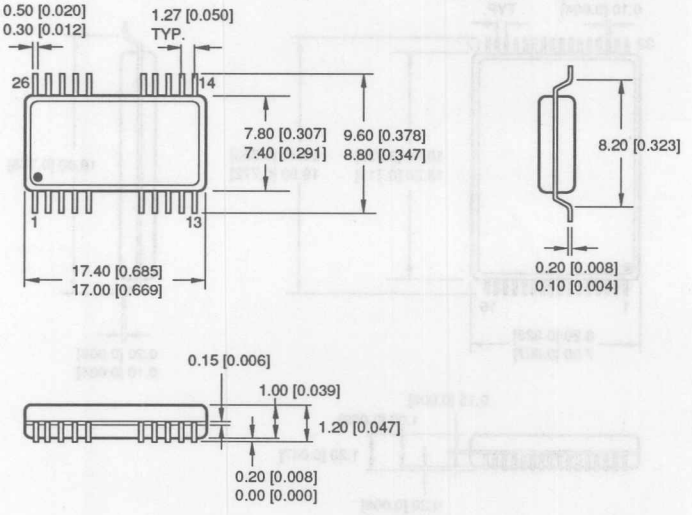
44SOP (SOP44-P-600)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

44SOP

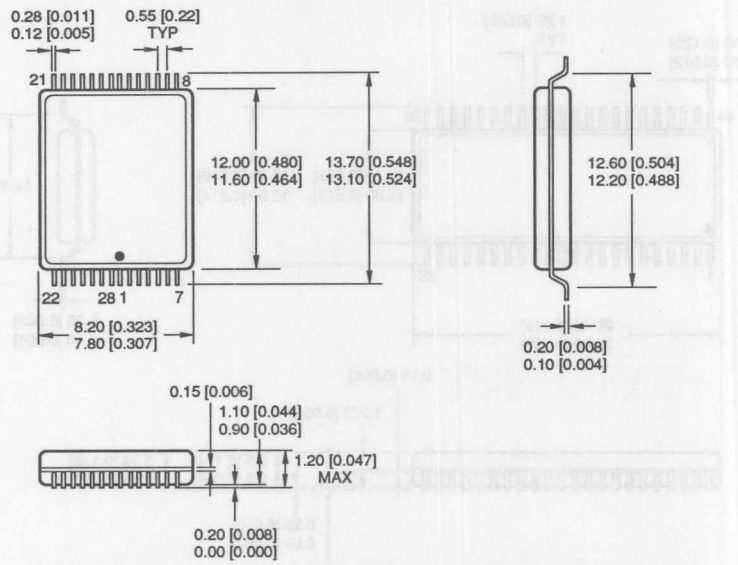
26TSOP (TSOP26-P-300)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

26TSOP

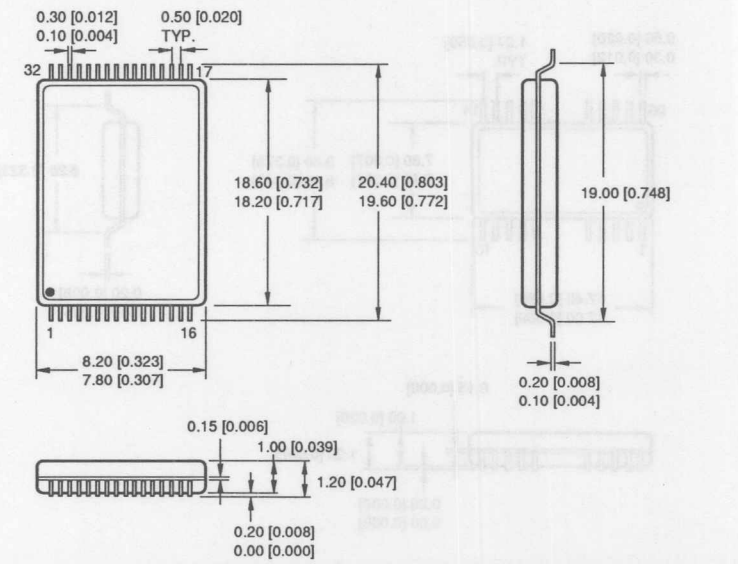
28TSOP (TSOP28-P-0813)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

28TSOP

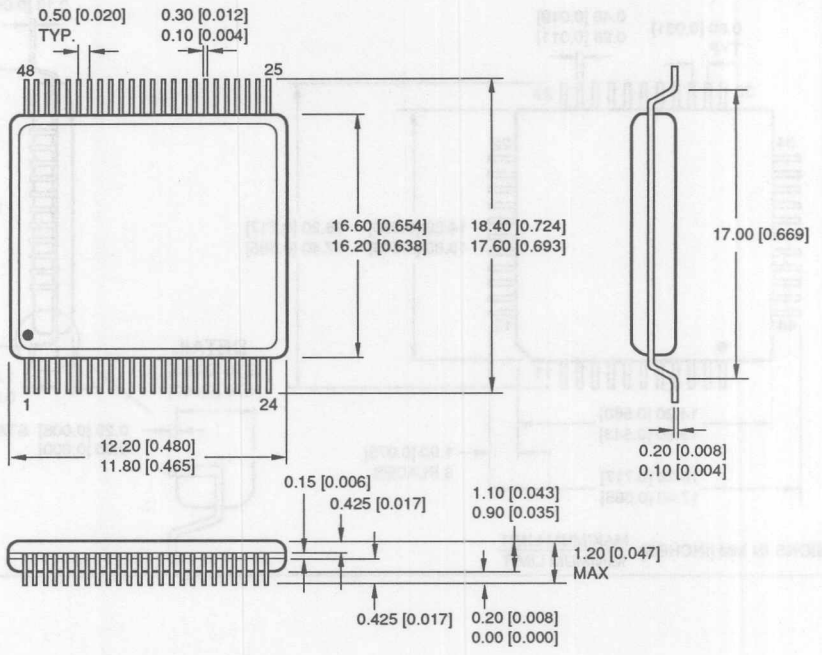
32TSOP (TSOP32-P-0820)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

32TSOP

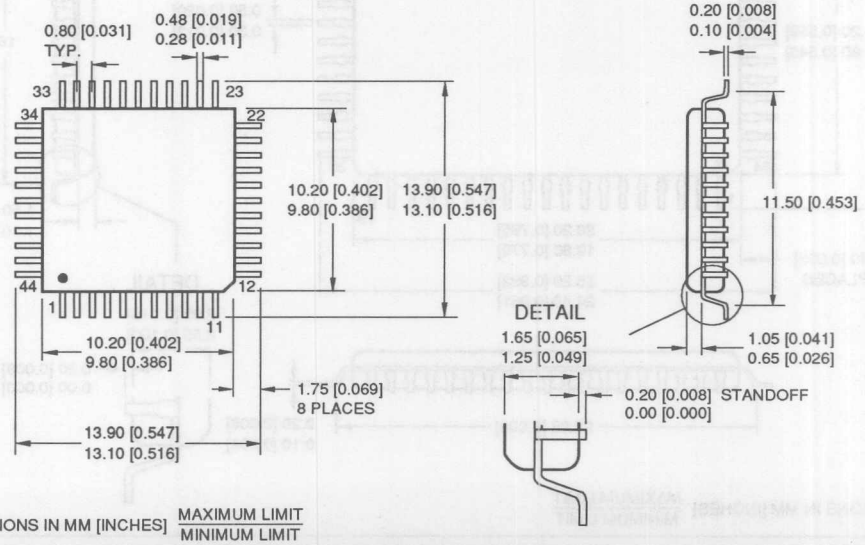
48TSOP (TSOP48-P-1218)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

48TSOP

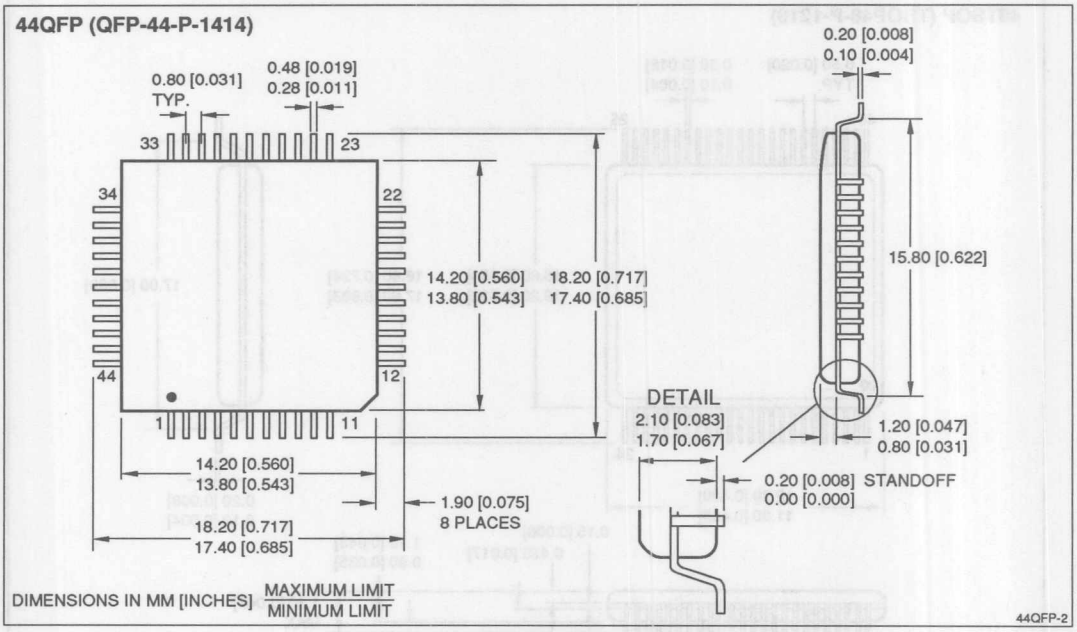
44QFP (QFP-44-P-1010)



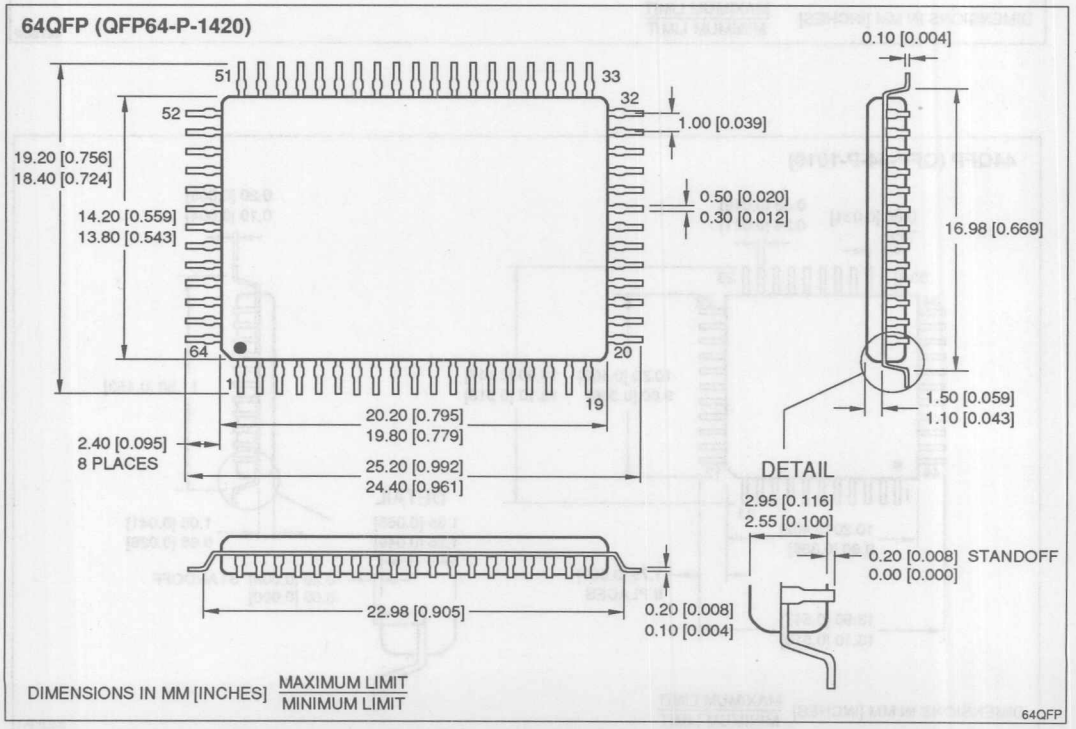
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

44QFP-1

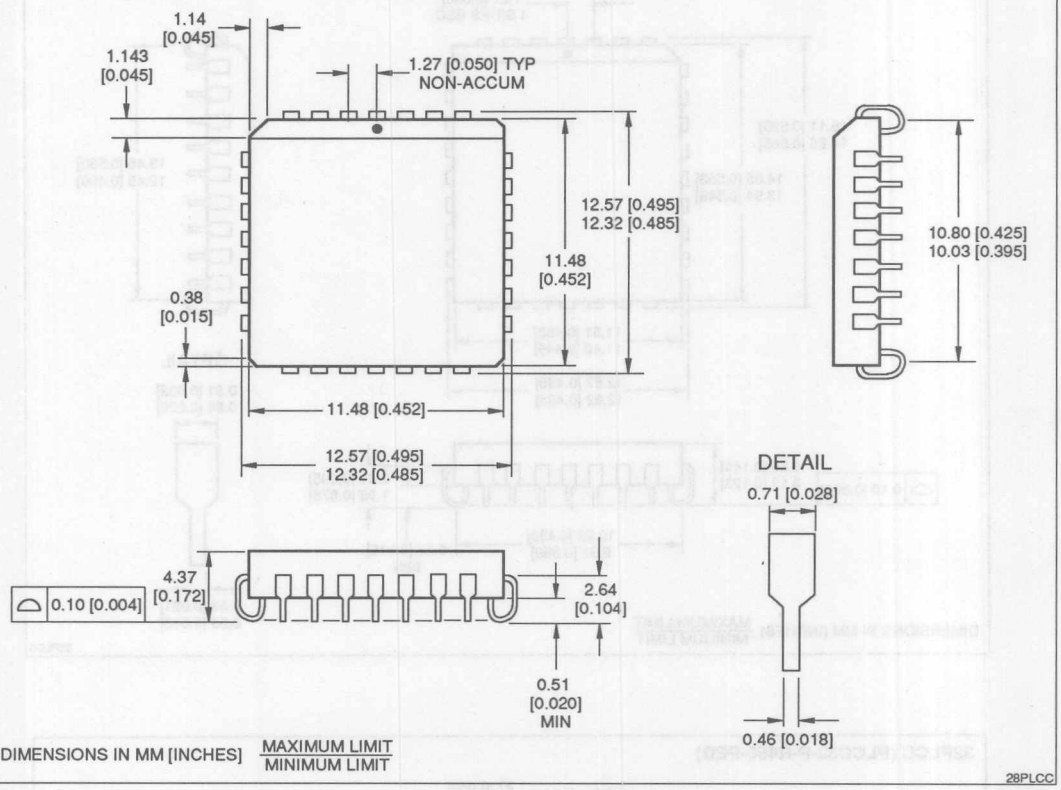
44QFP (QFP-44-P-1414)



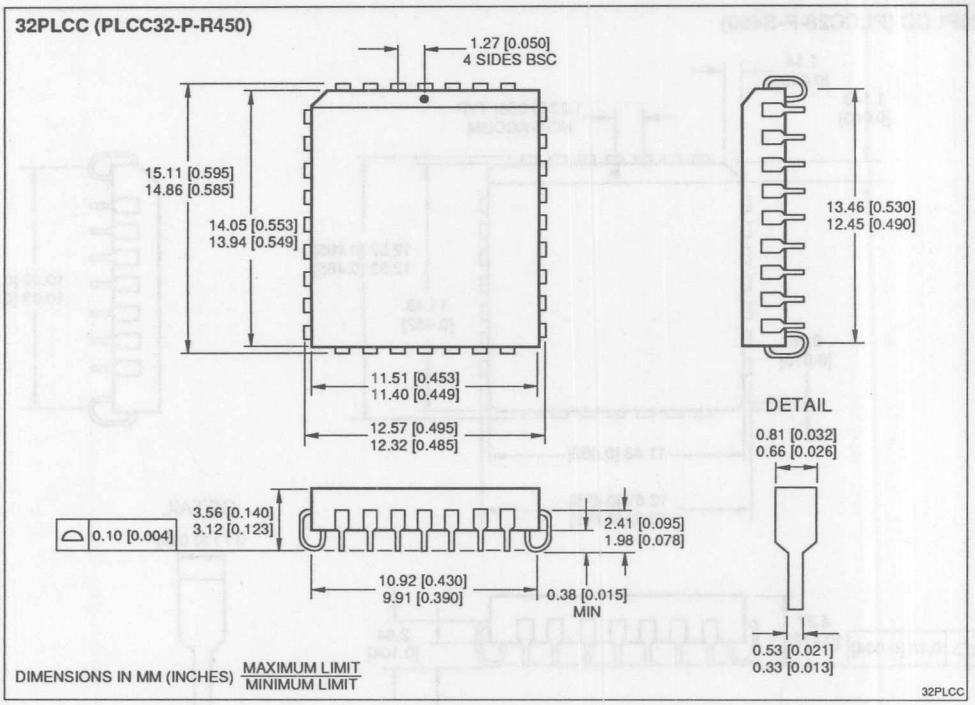
64QFP (QFP64-P-1420)



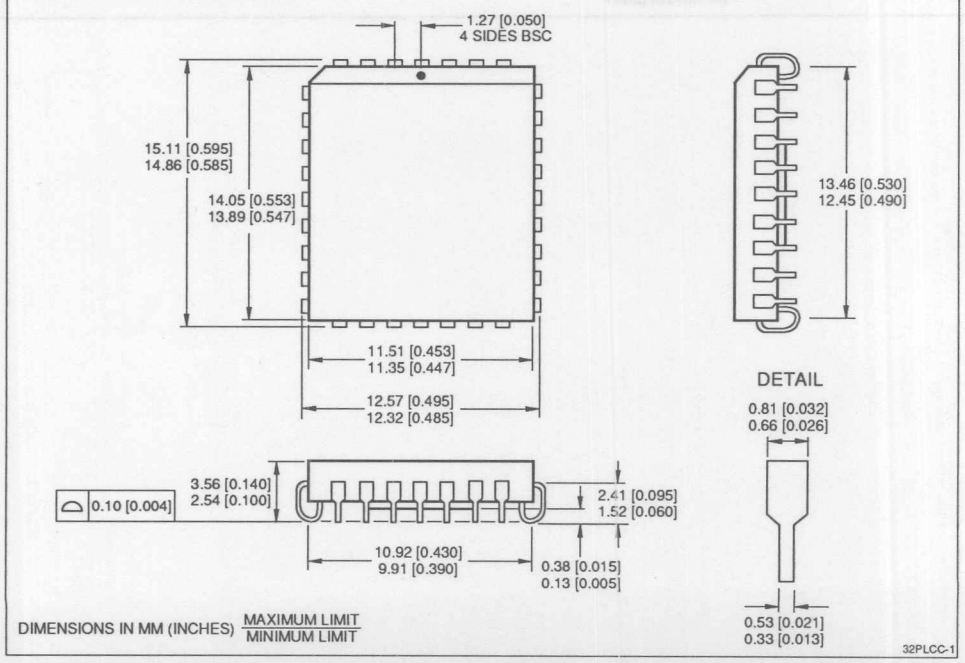
28PLCC (PLCC28-P-S450)



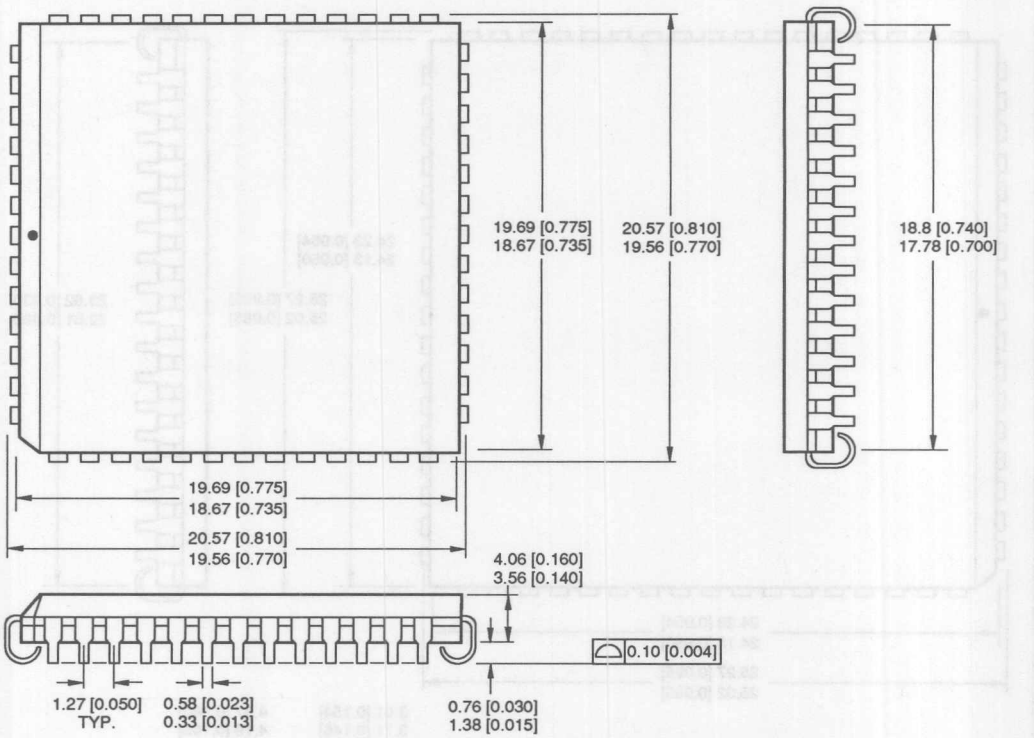
32PLCC (PLCC32-P-R450)



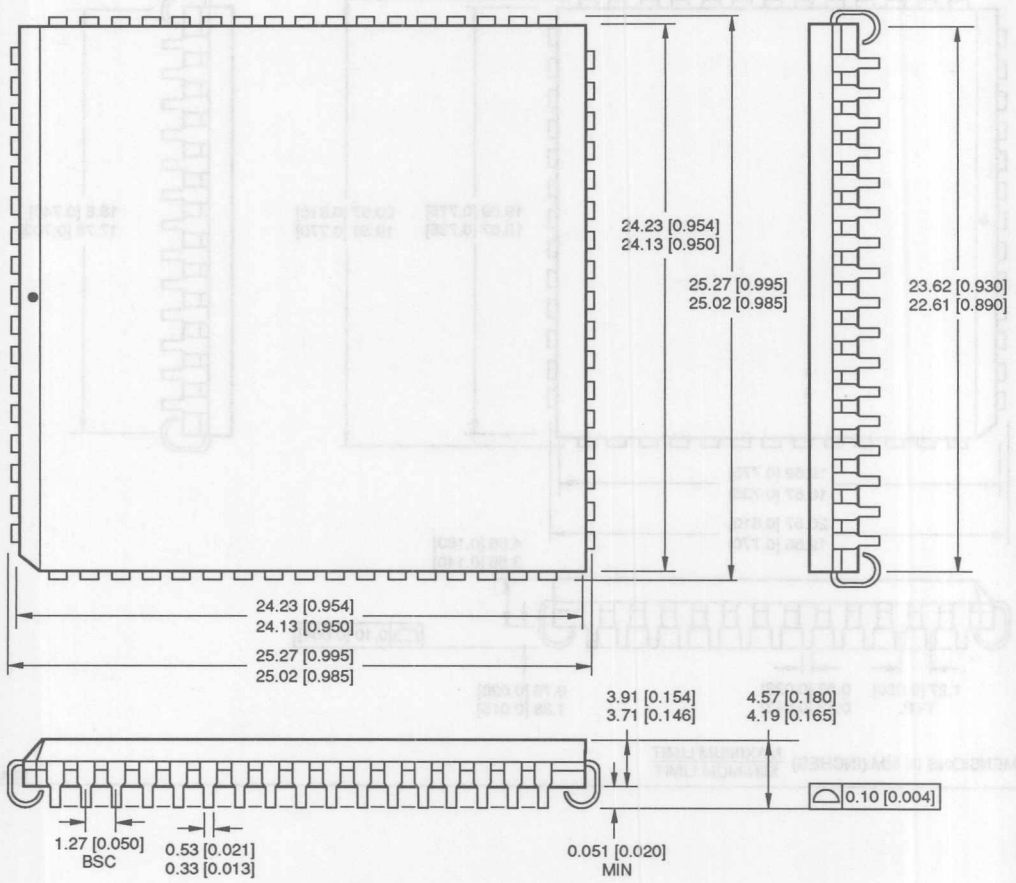
32PLCC (PLCC32-P-R450-PED)



52PLCC (PLCC52-P-750)



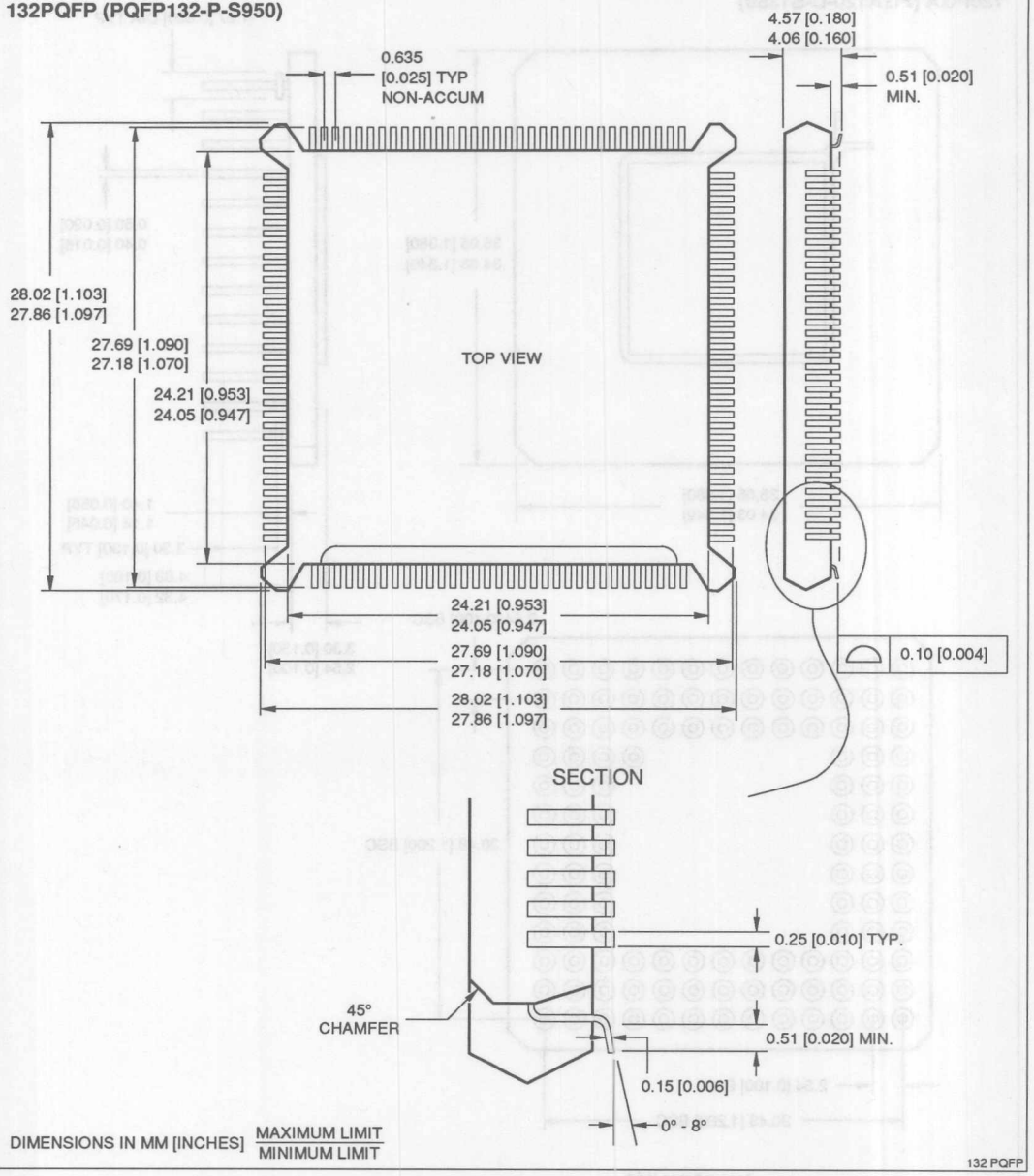
68PLCC (PLCC68-P-950)



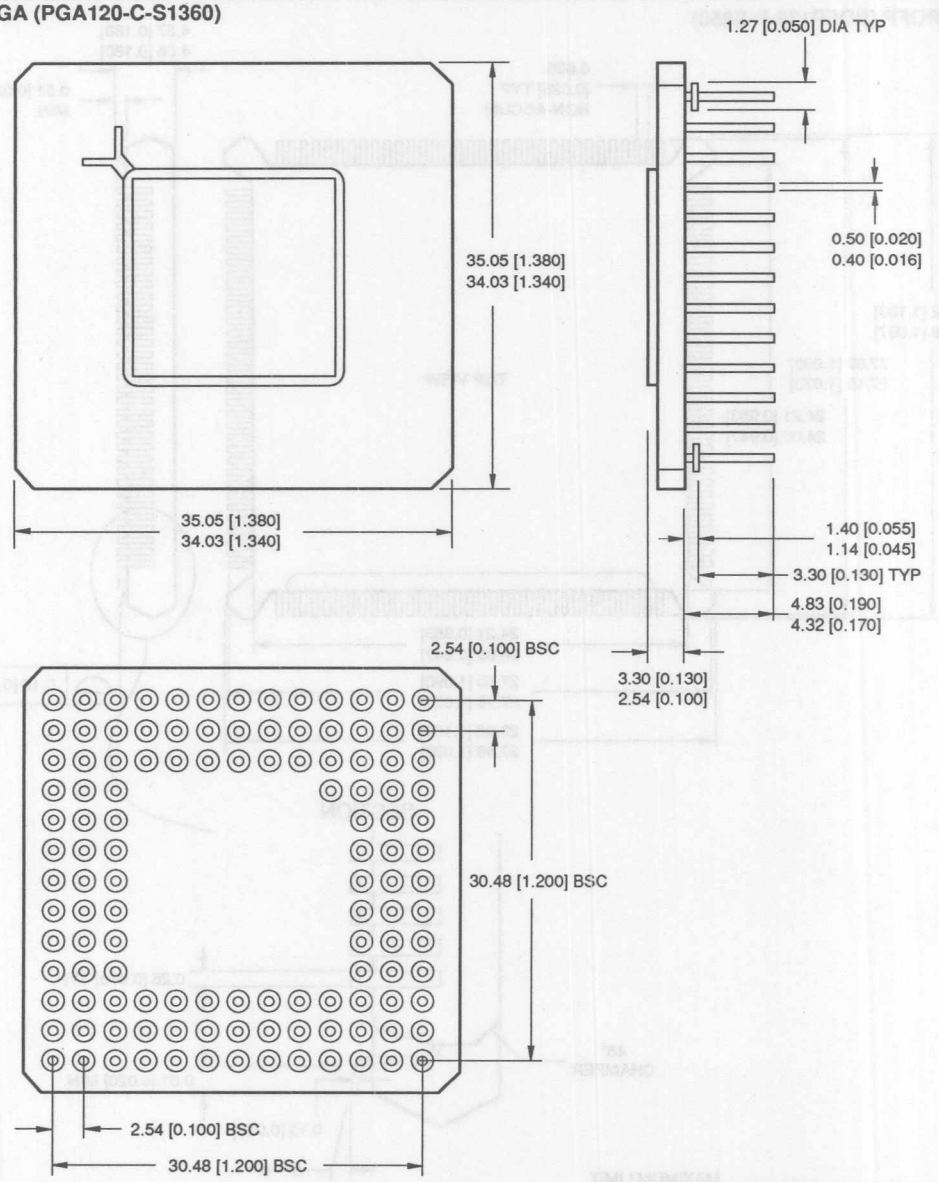
DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

68PLCC-1

132PQFP (PQFP132-P-S950)



120PGA (PGA120-C-S1360)



DIMENSIONS IN MM [INCHES] MAXIMUM LIMIT / MINIMUM LIMIT

120PGA